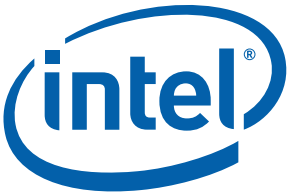

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Platform Design Guide (PDG)

September 2017

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Date	Revision	Description

September 2017	2.1	Updated the following:
		• Chapter 3
		  • Updated Table 3-10, "DBxxxxZL Reference Clock Topology - DBxxxxZL to PCIe Connector."
		  • Updated Figure 3-15, "Add Two GND Vias For CLK_X1 and CLK_X2 Signals."
		  • Updated Section 3.4, "Flex Clock Output Design Guide."
		• Chapter 4
		  • Updated note following Table 4-2, "DDR4 DQ/ECC to DQS Grouping."
		  • Updated Section 4.4.5, "SODIMM Special Design Guide."
		  • Added Section 4.4.6, "SODIMM Ground Plane Voiding for DQ and DQS."
		  • Added Section 4.6, "DIMM SPD Addressing Requirements."
		  • Added Section 4.7, "DDR4 Low Speed Signals."
		• Chapter 6
		  • Updated Table 6-13, "SMBUS Point-to-Point Clock, Data, and Alert to a Device Down and to a Connector (SMB_LAN_CLK, SMB_LAN_DATA, and SMB_LAN_ALRT_N) Layout Recommendations."
		  • Deleted row from Table 6-17, "NC-SI Transmit (NCSI_TXD0, NCSI_TXD1, NCSI_TX_EN) Layout Recommendations."
		  • Updated Table 6-21, "MDC (LAN_MDC) Point-to-Point to Device Down and the MDC (LAN_MDC) Point-to-Point to a Connector Layout Recommendations."
		  • Updated Table 6-23, "MDIO (LAN_MDIO) Point-to-Point to a Device Down and for a MDIO (LAN_MDIO) Point-to-Point to a Connector Layout Recommendations."
		• Chapter 9
		  • Updated Table 9-6, "Dual Devices STAR Routing Guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]."
		  • Updated Table 9-7, "Dual Devices DAISY CHAIN routing guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]."
		  • Updated Table 9-9, "Dual Devices STAR Routing Guidelines for SPI_CLK."
		  • Updated Table 9-10, "Dual Devices DAISY CHAIN routing guidelines for SPI_CLK."
		• Chapter 10
		  • Updated Table 10-2, "EMMC_CLK Routing Guidelines To A Down Device."
		  • Updated Table 10-4, "EMMC_STROBE (RCLK) Routing Guidelines To A Down Device."
		  • Updated Table 10-6, "EMMC_CMD and EMMC_D Routing Guidelines To A Down Device."
		  • Updated Table 10-8, "EMMC_CLK Routing Guidelines To A Connector."
		  • Updated Table 10-10, "EMMC_STROBE (RCLK) Routing Guidelines To A Connector."
		  • Updated Table 10-12, "EMMC_CMD and EMMC_D Routing Guidelines To A Connector."
		• Chapter 11
		  • Updated Table 11-2, "SMBus Layout Recommendations (for all SoC SMBus signals SMBCLK, SMBDATA, and SMBALERT#)."
		  • Updated Table 11-7, "Legacy SMBus - Voltage Translator to DIMM Layout Recommendations."
		  • Updated Table 11-8, "Legacy SMBus - Voltage Translator to DIMM Layout Recommendations."
		• Chapter 12
		  • Updated Figure 12-3, "Harcuvar and Cormorant Lake RTC and RTC Well Signals."

Date	Revision	Description

September 2017	2.1	• Chapter 13
		  • Updated Table 13-16, "SVID_CLK Layout Recommendations."
		  • Updated Table 13-18, "SVID_DATA Layout Recommendations."
		  • Updated Table 13-20, "SVID_ALERT_N Layout Recommendations."
		  • Updated Table 13-29, "LPC_CLK Layout Recommendations: LPC_CLKOUT[1:0]."
		  • Updated Table 13-31, "LPC_AD[3:0]: Star Layout Recommendations."
		  • Updated Table 13-33, "LPC_AD[3:0]: Daisy Chain Layout Recommendations."
		  • Updated Table 13-35, "LPC_FRAME_N: Star Layout Recommendations."
		  • Updated Table 13-37, "LPC_FRAME_N: Daisy Chain Layout Recommendations."
		  • Updated Table 13-39, "LPC_SERIRQ Layout Recommendations: SoC IO CMOS Point-to-Point."
		  • Updated Table 13-56, "UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS SoC Star_OD Input Layout Recommendations."
		  • Updated Table 13-57, "UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS SoC Daisy Chain OD Input Layout Recommendations."
		  • Updated Table 13-59, "UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Layout Recommendations: SoC CMOS Output."
		  • Updated Table 13-61, "UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS SoC Star CMOS Output Layout Recommendations."
		  • Updated Table 13-63, "UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS SoC Daisy Chain CMOS Output Layout Recommendations."
		  • Updated Table 13-65, "FAN_TACH[3:0] Layout Recommendations: SoC CMOS Input."
		  • Updated Table 13-67, "FAN_PWM [3:0] Interface Layout Recommendations."
		• Appendix C
		  • Removed Previously titled Appendix C, DDR4 SODIMM Memory for 10 Layer Boards and incorporated applicable content into Chapter 4, "DDR4 Memory."

Date	Revision	Description

August 2017	2.0	Updated the following:
		• Chapter 2
		  • Updated Chapter 2, "Platform Stack-up and General Design Considerations."
		  • Combined the previously listed Chapter 3 into Chapter 2.
		• Chapter 4
		  • Updated Figure 4-36, "DDR4 VREFCA Daisy Chain, Single Channel Configuration."
		  • Updated Table 4-29, "DDR4 VREFCA Routing Guidelines."
		• Chapter 5
		  • Added Table 5-1, "Signal Names and Descriptions."
		• Chapter 6
		  • Updated Table 6-1, "Supported System Configurations."
		  • Updated Table 6-3, "Supported SFP+ Modules/Cables."
		  • Updated Table 6-6, "PLCC-B GbE Topologies."
		  • Updated Figure 6-7, "PLCC-B Platform - GbE Ethernet Configuration Block Diagram Overview."
		  • Updated Table 6-31, "SDP Assignment during Ethernet Mode of Operation."
		• Chapter 7
		  • Updated Section 7.5, "Miscellaneous Signals."
		  • Updated Section 7.7, "SATA Interface Re-driver."
		• Chapter 8
		  • Combined previous USB 2.0 and USB 3.0 chapters.
		  • Updated Section 8, "USB Interfaces."
		  • Updated Table 8-1, "Signal Names and Descriptions."
		  • Updated Section 8.6, "Terminating Unused USB Interfaces."
		• Chapter 9
		  • Updated Section 9.1, "Serial Peripheral Interface (SPI) General Introduction."
		  • Updated Section 9.3, "Serial Peripheral Interface (SPI) Topology Guidelines."
		  • Updated Section 9.4, "TPM Support."
		• Chapter 10
		  • Updated Figure 10-4, "EMMC_CMD and EMMC_D to Down Device Topology."
		  • Updated Figure 10-5, "EMMC_CLK Topology To A Connector."
		  • Updated Figure 10-7, "EMMC_CMD and EMMC_D Topology To A Connector."
		• Chapter 11
		  • Updated Section 11, "System Management Bus Interfaces."
		  • Added Table 11-1, "Signal Names."
		  • Updated Section 11.1.1, "Legacy SMBus Connections To DDR4."
		• Chapter 12
		  • Updated Table 12-1, "RTC Signals."
		  • Updated Section 12.1, "RTC Layout Considerations."
		  • Updated Section 12.3, "RTC External Battery Connection."
		  • Added note to Section 12.4, "Clearing Battery-Backed RTC RAM."
		  • Updated Section 12.5, "Real Time Clock (RTC) Design Without Battery."
		• Chapter 13
		  • Added Section 13.1.1, "High Speed I/O."
		  • Added Table 13-28, "Signal Names and Descriptions."
		• Appendix D
		  • Updated Figure C-14, "SoC KR Connections to *Inphi Quad Port SFP+ PHY (CS4223)."

Date	Revision	Description

March 2017	1.7	Updated the following:
		• Chapter 1
		  • Updated Section 1.1, "Overview."
		  • Repaired references in Table 1-2, "Reference Documents."
		• Chapter 3
		  • Updated Table 3-1, "Coupling Capacitors."
		  • Updated Section 3.4.2.2, "Integrated Ethernet Controller 25 MHz Crystal Guidelines."
		  • Updated Table 3-10, "32.768 KHz Crystal Specification."
		  • Updated Figure 3-14, "Crystal Layout Guidance."
		• Chapter 4
		  • Updated Figure 4-1, "DDR4 Byte Lane Classifications."
		  • Updated Section 4.5, "Memory Down Design Guidelines."
		  • Updated Table 4-15, "Routing Topology Support Memory Down Configurations"
		  • Updated Table 4-16, "Length Matching Formulas"
		  • Updated Table 4-22, "Dual Rank DDR4 Command and Address Routing Guidelines"
		  • Updated Table 4-23, "DDR4 Point-to-Point Control Signal Routing Guidelines"
		  • Updated Table 4-24, "DDR4 Clock Signal Routing Guidelines."
		  • Added Section 4.7.4, "32 Bit Memory Down Design Guide."
		• Chapter 6
		  • Updated Section 6.1, "Integrated 10 Gb/s Ethernet Controller Overview."
		  • Updated Table 6-1, "Supported System Configurations."
		  • Added a note to Table 6-3, "Supported SFP+ Modules/Cables."
		  • Added note about NC-SI Multi Drop Configuration to Section 6.6.2.5, "NC-SI Layout Multi-drop Requirements."
		  • Updated Table 6-4, "LAN Controller LEK Image Support Model [1]."
		  • Updated Figure 6-37, "NC-SI Connection Schematic: Single-Drop Configuration."
		  • Updated 1G-BASE-T with Marvel 1512/1514 entries in Table 6-31, "SDP Assignment during Ethernet Mode of Operation."
		• Chapter 10
		  • Updated Section 9.4, "TPM Support."
		  • Updated Table 9-14, "eMMC Signals." and added a note to Figure 9-8, "eMMC Interface Topology."
		• Chapter 13
		  • Updated note after Figure 13-19, "LPC_SERIRQ Routing Illustration: SoC IO CMOS Point-to-Point."
		• Chapter 14
		  • Updated Section 14.1, "Requirements for Bringing the SoC Out of Reset" on page 465
		• Appendix D
		  • Updated Figure C-6, "SGMII to Dual 1GBASE-T."

Date	Revision	Description
October 2016	1.6	Updated the following: Incorporated the Denverton Product Family Pine Lake Comms Collateral (PLCC) Platform Design Guide (PDG) Supplement (Document Number #562827). • The dog-bone trace width has been redefined based on a signal's trace impedance specification in Table 3-9. • The DQS open field spacing has been clarified in Table 4-7 and Table 4-11. The minimum spacing, if needed, can be 4 mils. • Multiple updates were made to Table 6-1. • SATAx_SCLK, SATAx_SLD, and SATAx_SDOUT have been redefined from CMOS outputs to Open Drain Outputs in Table 7-27 and Table 7-28. • Added Figure 13-33 and Figure 13-34 plus Table 13-65, Table 13-66, Table 13-67, and Table 13-68 to define the FAN_TACH[3:0] and the FAN_PWM[3:0] signals. • Updated Table 15-1, Table 15-2, Table 15-3, and Table 15-4. • Updated Section 15.3, "CRB DC-DC Converter Designs" on page 475. • Multiple changes to figures in Appendix C.
March 2016	1.1	Updated the following: • Updated Block Diagrams in Figure 1-2 and Figure 1-3. • Updated Max values in Table 3-1. • Additions to the Oscillator Guidelines, Chapter 3. These changes are numerous: text and graphics. Note these as 25 MHz Xtal updated layout recommendations. Section 3.4 - Updated requirements for crystal signals. • Chapter 3, "Platform Clocks", Section 3.4, text updated with new figures: Section 3.4 removed. • Addition of design information for the DDRx_ALERT_N_PAR_ERR_N signals for RDIMM only, Chapter 4, Section 4.7.5.4, "DDR4 Alert signals: DDR0_ALERT_N_PAR_ERR_N and DDR1_ALERT_N_PAR_ERR_N" on page 189. Includes a new picture and updates to Table 4-27. • Updated Section 6.1, Figure 6-1, Table 6-1, and Section 6.5. - Table 6-9, the maximum channel length (surface mount) changed from 5" to 6" and the maximum channel length (SFP+ through hole mount connector) was removed. - Table 6-9, note #8 remove and note #10 updated. - Table 6-11, the No. of Via Transitions was set to 2. • Updated Section 8, Figure 8-1, Table 8-6, and Figure 8-5. • Updated Section 9.4 and Figure 9-9. • Addition of design information for the Legacy SMBus to SPD, Chapter 11, Section 11.1.1, "Legacy SMBus Connections To DDR4" on page 391. This is a new picture with new tables of design info. • Updated Figure 11-1. • Added a value for Cin, Chapter 12, Section 12.2, "External Capacitors" on page 404. Cin1 = Cin2 = 1-2 pF. • Changes to PROCHOT_N and MEMHOT_N design recommendations, Chapter 13. There may also be changes to THERMTRIP_N also. These three come up first in the chapter. There are graphic and text changes including Figure 13-2 and Figure 13-4. • Addition of the LC Filtering Table for specific applications, Chapter 15, Section 15.6, "DDR4 DIMMs Power Delivery Guidelines" on page 514. New table for applications whose LC filtering differs from the rail sections above. Updated Section 15.1. Updated Figure 15-1, Figure 15-2, and Figure 15-3. • Addition of Appendix C, "SoC to LAN Common Connections".
October 2015	1.01	Updated Table 6-1. • Removed 1000BASE-T row • Added Marvell 88E1512 to third party PHYs/switches Section 6.6.5 • Updated first paragraph • Removed note
September 2015	1.0	Multiple changes made throughout the document. • Changes from the initial release will be marked with change bars. • Detailed change descriptions will be utilized after Revision 1.0.
July 2015	0.96	Multiple changes made throughout the document. • Changes from the initial release will be marked with change bars. • Detailed change descriptions will be utilized after Revision 1.0.

Date	Revision	Description
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February 2015	0.9	Multiple changes made throughout the document. • Changes from the initial release will be marked with change bars. • Detailed change descriptions will be utilized after Revision 1.0.
December 2014	0.8	Multiple changes made throughout the document. • Changes from the initial release will be marked with change bars. • Detailed change descriptions will be utilized after Revision 1.0.
September 2014	0.7	Initial release

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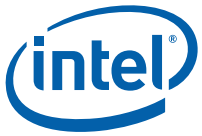

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1 Introduction

This Platform Design Guide (PDG) is used with the Intel® Atom™ Processor C3000 Product Family is the next generation System-On-Chip (SoC). These products address the growing needs for the emerging markets: microserver, cloud storage, and communications infrastructure. In addition to board design recommendations, such as layout and routing guidelines, this document also addresses other system design issues such as power delivery. The design rules are verified by Intel once the SoC System Validation (SV) board and the Customer Reference Board Schematic (CRB) are laid-out, built, powered-on, and validated. Until that time, the information in this PDG is preliminary and is subject to change. Even so, not all of the guidance situations are verified by Intel.

See Table 1-1 for the Intel code names.

Table 1-1. Intel Code Names and CRB Applications

Intel Component	Intel® Atom™ Processor C3000 Product Family System-On-Chip (SoC) (codenamed Denverton / Denverton-NS)
Associated Platform	Harrisonville
uServer single-node	Aspen Cove
Storage	Cormorant Lake
Communications	Harcuvar
Communications	Pine Lake

In this document, the terms SoC and processor refer to the Intel® Atom™ Processor C3000 Product Family System-On-Chip component.

Note: Intel advises designers to follow the recommended design information provided in this document. These design guidelines are developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. The guidelines recommended are based on experience and preliminary simulation work done at Intel while developing systems based on the SoC platform with the SoC. This work is ongoing. The recommendations are subject to change.

Caution: If the guidelines listed in this document are not followed, Intel recommends designers to perform thorough signal integrity and timing simulations. Any deviation from the guidelines needs to be simulated. Even when following these guidelines, Intel recommends that the critical signals be simulated to ensure proper signal integrity and flight time.

The associated Intel schematics are used as a reference. While the schematics cover a specific design implementation, the core schematics remain the same for most boards. The schematic set provides a reference for the common design elements regardless of the application. Additional flexibility is possible through other permutations of these options and components.

1.1 Overview

The SoC manages the flow of information between the following interfaces:

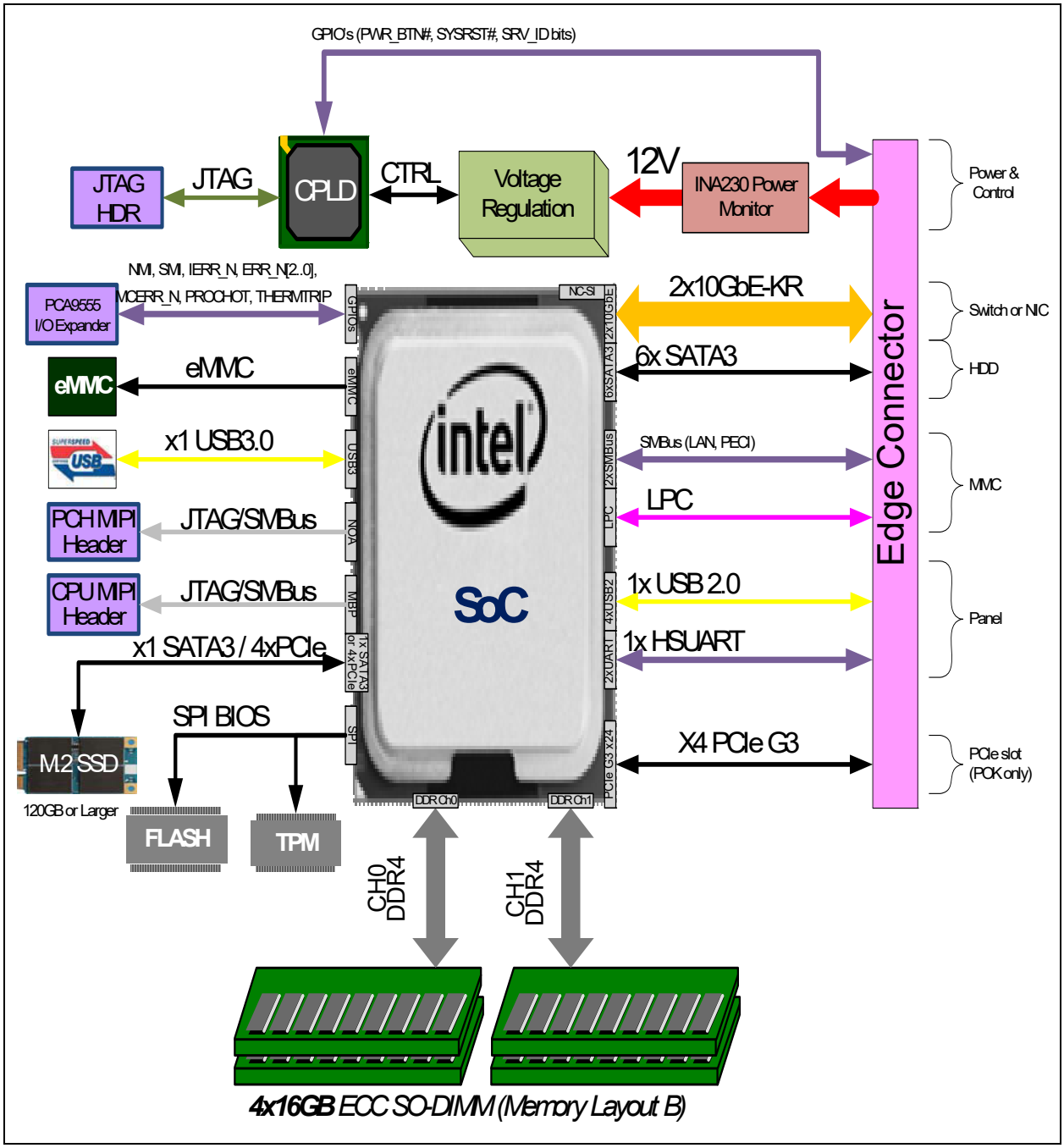
- DDR4 system memory (platform dependent)
- 10GBASE-KR, SFI, 2500BASE-X, 1000BASE-KX with no external PHY required
- SGMII 1 GbE and 10/100 Mb (Full Duplex only) are supported
- PCI Express* Gen 3
- USB 3.0 (also named USB 3.1 SS1 5 Gb/s per the USB-IF organization)
- USB 2.0
- SATA 3.1 (6 Gb/s, up to 16 ports with Flexible I/O)
- SPI for boot Flash
- eMMC (embedded Multi-Media Card). Supports eMMC 5.0
- Low Pin Count (LPC)
- High Speed Universal Asynchronous Receive/Transmit (HSUART)
- Power and thermal management through the SMBus and I^2C interfaces
- Reset and error reporting

The SoC supports up to two channels of DDR4 with up to two DIMMs per channel. It also supports up to sixteen lanes of PCI Express Gen3, up to four USB 3.0 ports, up to sixteen SATA 3 ports or a combination of all three sharing up to 20 High Speed I/O lanes (SKU dependent) as set by the Flexible I/O Adapter. For details, refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*, Chapter 10, "Flexible I/O Adapter (FIA) Overview".

The SoC makes available up to four ports of 10Gb-KR Ethernet (SKU dependent) from the SoC for high throughput communication. System management (control and status reporting) is done through the SMBus interface. Low level hardware control and status reporting occurs through the power / thermal management and reset / error reporting signals.

See Figures Figure 1-1, Figure 1-2, and Figure 1-3 for the block diagrams of the board examples.

Figure 1-1. Aspen Cove CRB Block Diagram (uServer, Single Node)



Note: The package drawing above is not the true aspect ratio for the SoC. It is drawn elongated to allow for the full list of interfaces.

Figure 1-2. Cormorant Lake CRB (Storage)

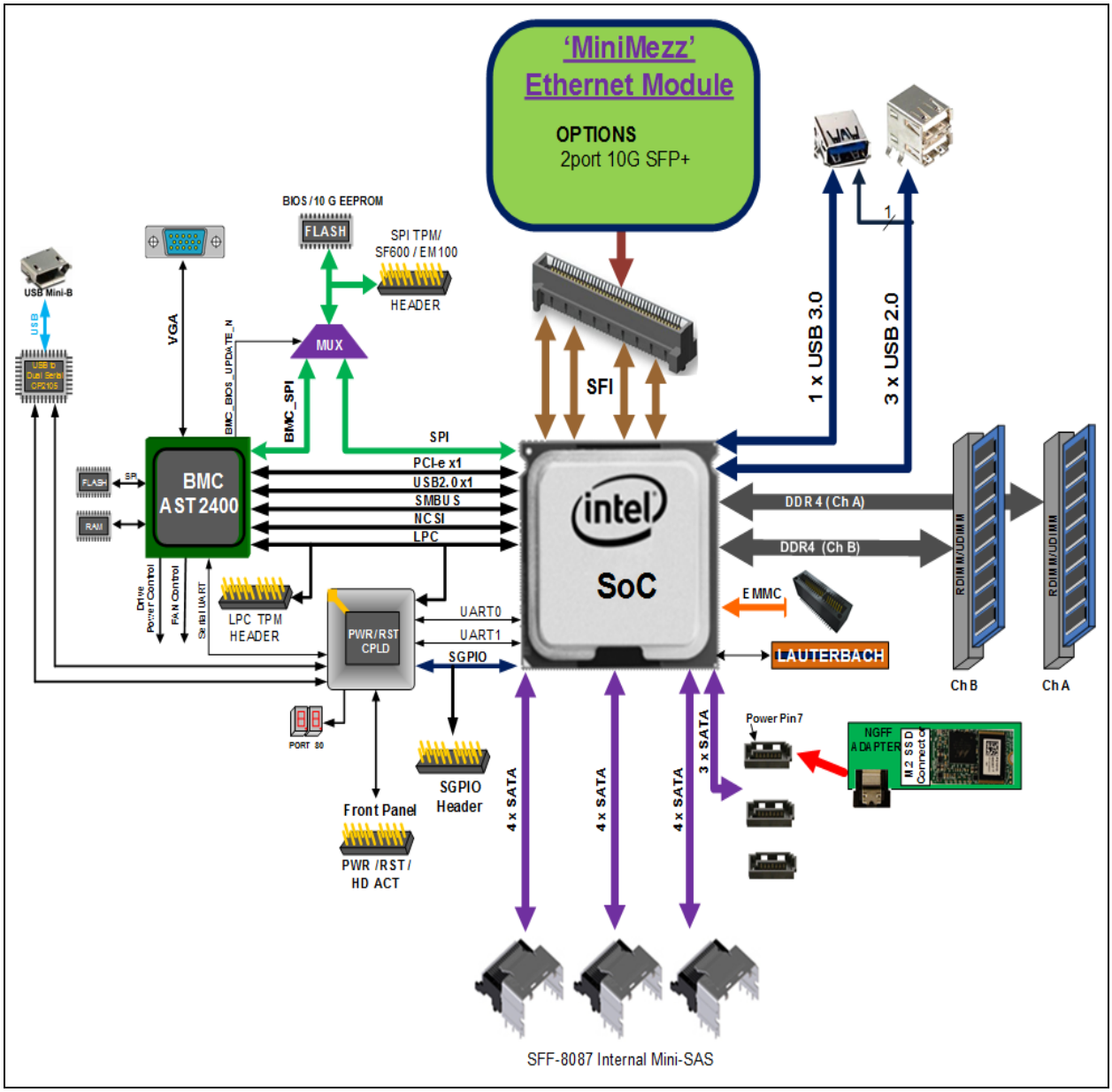
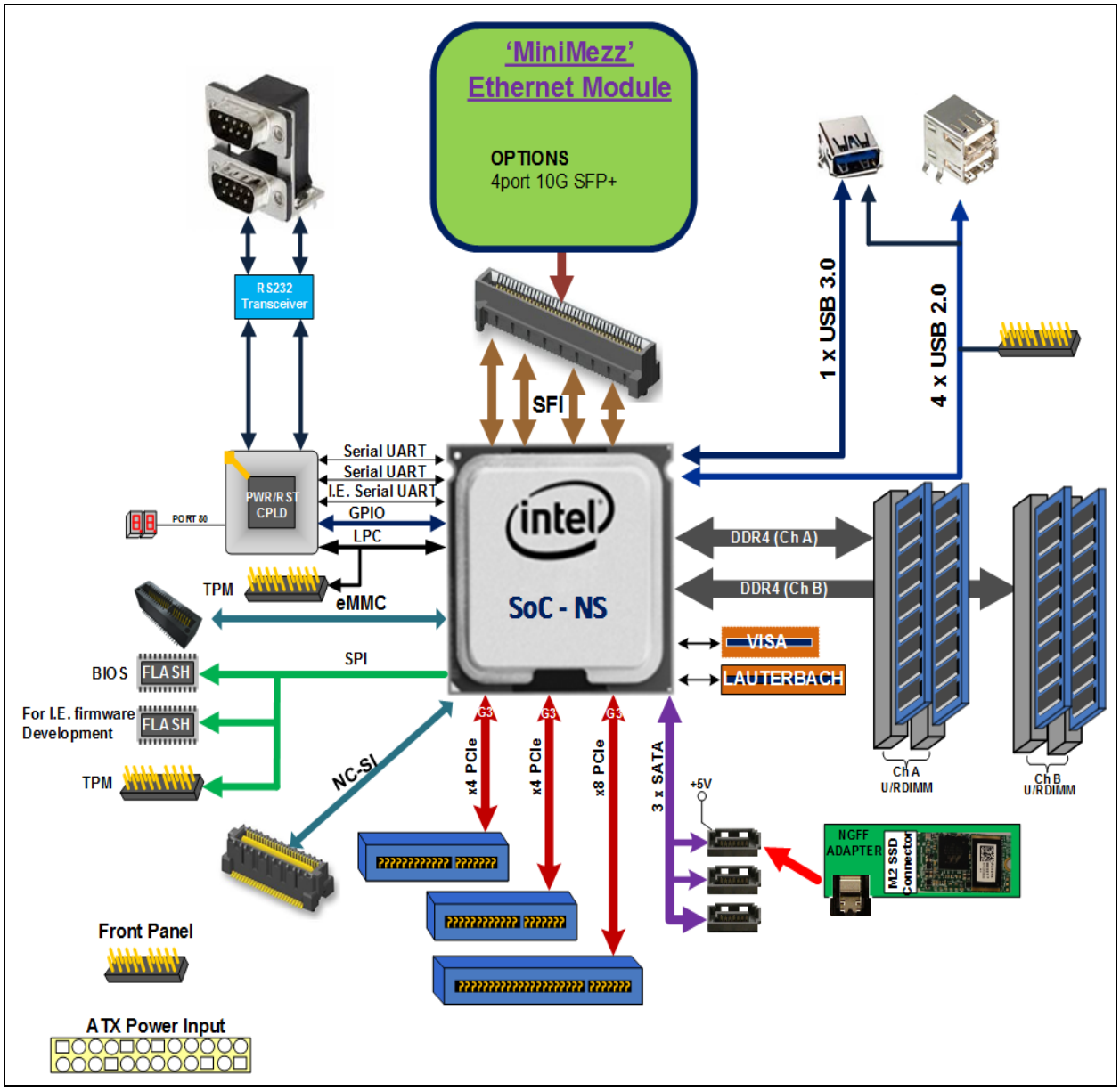


Figure 1-3. Harcuvar CRB (Communications using the -NS version of the SoC)



1.2 Pine Lake Reference Design

Pine Lake is a Proof of Design (PoD) based on the SoC to implement an IA-based compute module that demonstrates design attributes common in comms/microserver/ storage designs.

Pine Lake demonstrates an optimized low BOM cost design for the SoC Family. The platform can be scaled to support 2- and 4-core SoCs, up to 15W SKUs, and the platform can support a fanless solution.

This document includes design considerations for an optimized form factor with a 6-layer stack-up and a simplified power delivery solution with the system either ON or OFF; no sustain power delivery is required. The design is cost optimized to reduce the number of required Voltage Regulators (VR).

The design of the platform supports two types of memory form factors: memory down devices, and SO-DIMM. The design implementation demonstrates memory down devices and SO-DIMM to allow for future expansion without a redesign. The memory down designed in this platform design guide provides both designs in x8 or x16 device configuration.

The design of the platform supports up to 12 High Speed I/O (HSIO) lanes which included multiple PCIe* slots, SATA ports, and USB 3.0 ports. The platform utilizes the SoC integrated 10 Gigabit Ethernet controller (GbE controller) in the design connected to 10GbE, 1GbE and Ethernet switch interface.

Note: The Platform Design Guide is intended to provide maximum flexibility for the board designer while reducing the risk of board design related issues. The design guide is based on an Intel simulation and board implementation. The design guideline has some design limitations and constraints based on six layers of PCB routing:

- Power delivery and distribution support up to 15W, 2- or 4-core SKUs
- DDR4 memory down and SO-DIMM supports x8 and x16 up to 2133 MT/s, single and dual rank, ECC

The design recommendation must be followed as stated in this document to meet timing and signal quality goals, any deviations from the recommended guidelines in terms of topology, layout, and configuration can cause system instability. If any deviations from this design guide occur, Intel recommends that designers conduct extensive modeling, simulation, and validation.

The design provides the following additional features:

- Industry standard mini-ITX FF compact design
- Off the shelf mini-ITX chassis with external PCIe slot
- Optimized form factor to meet thermal profiles for fanless 2-core and high performance 4-core thermal solution
- Single power source (12V), on/off power delivery, and power sequencing to reduce the number of VRs; simpler power sequencing design with no sustain power delivery required.
- An all-in-one system allows operation as a standalone platform; it has a built-in eMMC and mSATA with a fully enclosed system, ready to operate.
- Two types of memory topologies with ECC are supported: memory down (CH0) -up to dual rank DDR4-2133 and SO-DIMM (CH1) - 1DPC DDR4-2133.
- Connected to multiple GbE ports: one single 10GbE port, two single GbE PHY ports, and eight ports 1GbE Ethernet switch.
- External USB 3.0 and USB2.0 ports
- RTC design support with and without battery

Figure 1-4 shows the Pine Lake Reference Design.

Figure 1-4. PLCC-A Block Diagram with x8 Memory Down and 10GbE Switch

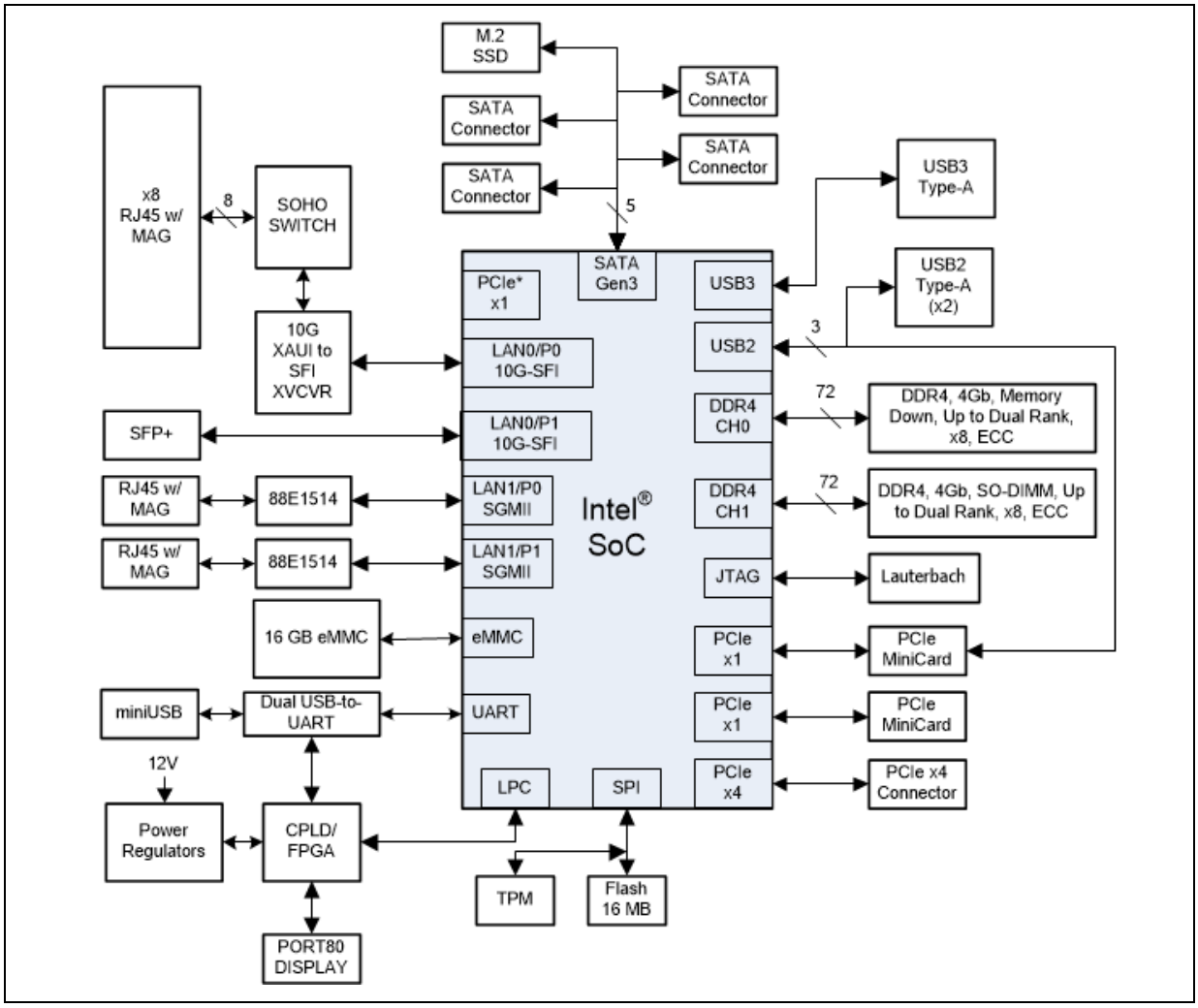


Figure 1-5. PLCC-B Block Diagram with x16 Memory Down and 2.5GbE Switch

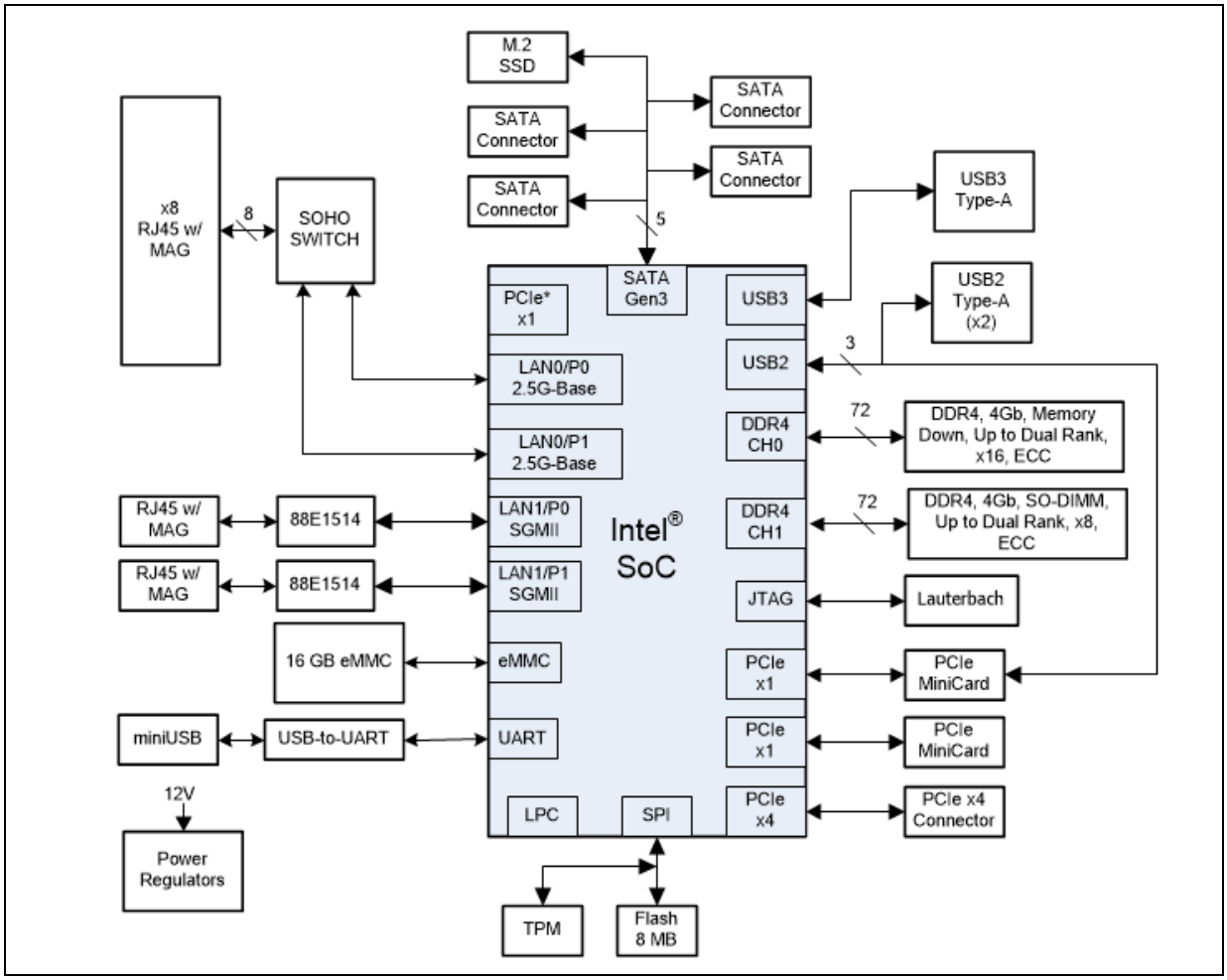
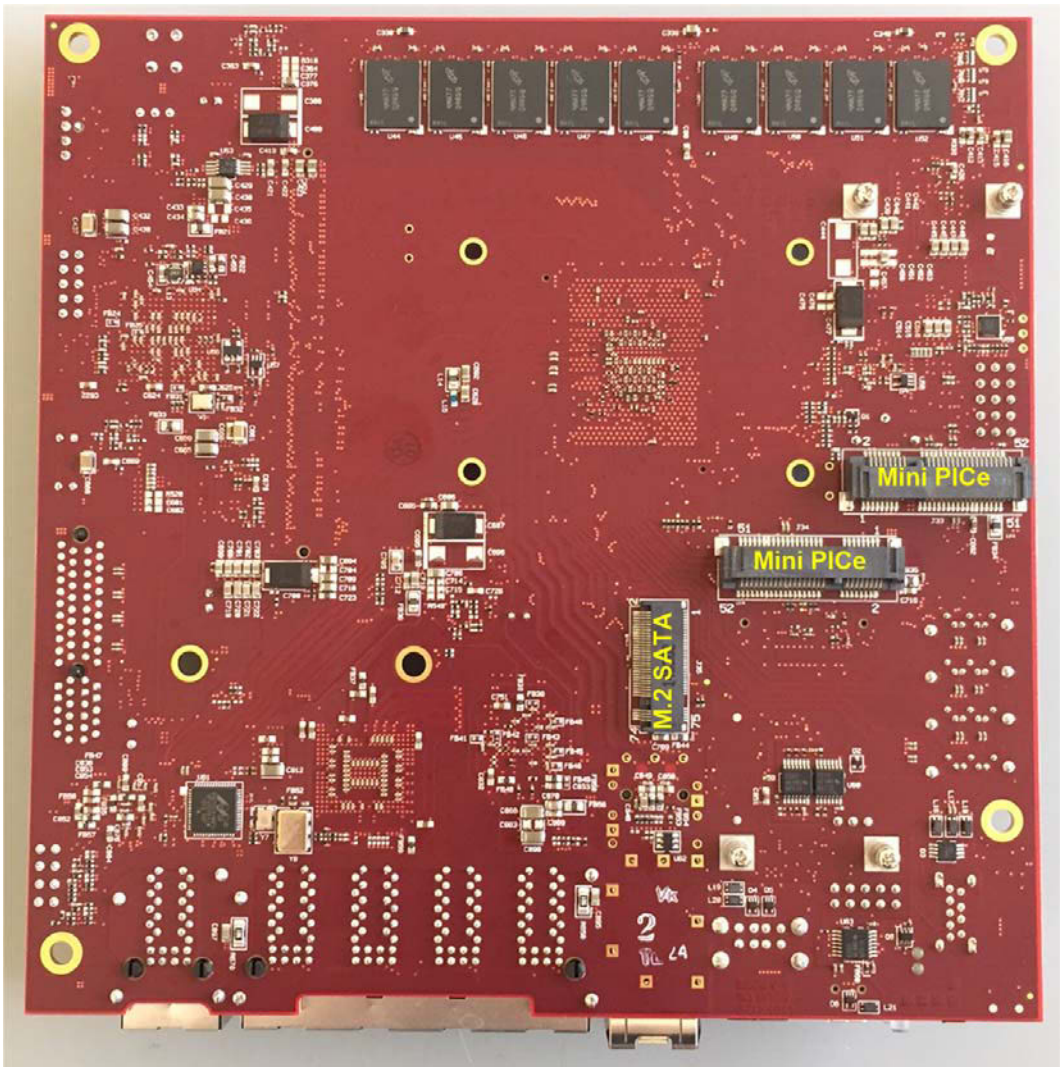


Figure 1-6 and Figure 1-7 are the photographs of the Pine Lake Reference Design.

Figure 1-6. Pine Lake-A Top View

Figure 1-7. Pine Lake-A Bottom View



1.3 Reference Documentation

The following documents are referenced in various sections of this design guide.

Table 1-2. Reference Documents (Sheet 1 of 4)

Document	Document Number/ Source
Product References	
Harrisonville Platform DDR4 HSPICE Signal Integrity Model User Guide [MUG]*	557297
Harrisonville Platform PCI Express Signal Integrity Model User Guide [MUG]*	553621
Harrisonville Platform USB3 HSPICE Signal Integrity Model User Guide [MUG]*	552496
Harrisonville Platform SATA3 HSPICE Signal Integrity Model User Guide [MUG]*	553620
Intel® Denverton DDR4 Interface Trace Length Calculator [TLC]	558800
Denverton and Denverton-NS SoC 60-Pin Debug Port Specification Design Guide	556262
Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4	558579
Denverton and Denverton-NS SoC Thermal/Mechanical Specification and Design Guide [TMSDG]	558591
Denverton SoC Product Family BIOS Writer's Guide [BWG]	566888
Intel® Atom™ Processor C3000 Product Family Specification Update - NDA	572409
Intel Atom Processor Denverton Product Family [Aspen Cove] Customer Reference Board [CRB] SODIMM PDF Schematics	556064
Intel Atom Processor Denverton Product Family [Aspen Cove] Customer Reference Board [CRB] RDIMM PDF Schematics	566116
Intel Atom Processor Denverton Product Family [Cormorant Lake] Customer Reference Board [CRB] PDF Schematics	565190
Intel Atom Processor Denverton Product Family [Harcuvar] Customer Reference Board [CRB] PDF Schematics	556067
Intel Atom Processor Denverton Product Family Pine Lake PLCC-B Proof of Design Platform for BOM Cost Optimization Design Collateral Beta 1 Release	568258
Intel Network Connections 20.7 PV, Intel Pre-boot BIOS Image Utility BootUtil, LAN Software Tools 8-Feb-2016	387754
Intel Ethernet Network Connection X553 [Denverton] Schematic Checklist	551166
Intel Ethernet Connection X553 Denverton Layout Checklist	563945
Reason for Trace Routing at 85 Ohms in High Speed Differential Design	569488

Table 1-2. Reference Documents (Sheet 2 of 4)

Document	Document Number/ Source
Other References	
Advanced Configuration and Power Interface Specification 5.0a *Advanced Configuration and Power Interface Specification 4.0*	http://www.acpi.info/spec.htm
Alert Standard Format (ASF) Specification, Version 2.0	http://www.dmtf.org/standards/documents/ASF/DSP0136.pdf
INCITS 361-2002 (1410D): AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
DDR4 SDRAM Standard JESD79-4A	http://www.jedec.org
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://www.intel.com/content/dam/www/public/us/en/documents/technical-specifications/ehci-specification-for-usb.pdf
Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies White Paper	406926
Front Panel I/O Connectivity Design Guide (Look for I/O Connectivity in formfactors.org)	http://www.formfactors.org/developer/specs/A2928604-005.pdf
Graft Cadence Allegro PCB Editor SKILL Utility for Adding Tabbed Routing, Revision 2.5	567091
IEEE 802.3 Fast Ethernet	http://standards.ieee.org
IEEE Standard 802.3, 2000 Edition	http://standards.ieee.org
IEEE Standard 1149.1, 2001 Edition (JTAG)	http://standards.ieee.org
Innovation Engine Developers Guide Volumes 1 through 3 - Rev. 2.0	558866
Intel Annex 69B Ethernet Board Channel Executable Simulation Kit 21-Apr-2016	550875
Intel Ethernet Switch FM5000/FM6000 [Alta] Series User Guide Rev. 2.1	491052
Intel® Ethernet Switch FM6000 [Alta] Series – Layout Checklist – Rev. 0.8	540069
Intel® FM5000/FM6000 Ethernet Switch Datasheet, Rev. 3.3	526654
Intel® Interconnect Model Analyzer and Domain Converter (Intel® IMADC) Software, Rev. 1.3.1 • *Intel Interconnect Model Analyzer and Domain Converter [Intel IMADC] Users Guide Revision 1.3*	551538 (569227)
Low Pin Count (LPC) Interface Specification, Revision 1.1	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress
PCI Express Card Electromechanical Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress

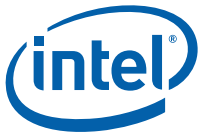


Table 1-2. Reference Documents (Sheet 3 of 4)

Document	Document Number/ Source
PCI Express 3.0 438-Pin Riser Card Edge Connector Specification*	329988 http://www.intel.com/content/dam/www/public/us/en/documents/technical-specifications/pcie-3-438-pin-riser-card-edge-connector-spec.pdf
PCI Bus Power Management Interface Specification Revision 1.2	http://www.pcisig.com/specifications/conventional/pci_bus_power_management_interface/
PICMG 3.1 R2.0 Ethernet/Fibre Channel for AdvancedTCA® Systems	https://www.picmg.org/product/ethernetfibre-channel-advancedtca-systems/
Quartz Crystal Theory of Operation and Design Notes	Fox Electronics http://www.foxonline.com
Repeater Assessment Methodology for Intel® Server Platforms Specification	507578
Serial ATA Revision 3.3 Specification	http://www.sata-io.org/
Serial-GMII Specification, Revision 1.8	Cisco Systems* http://www.cisco.com/ ENG-46158
Serial VID (SVID) Protocol Specification, Rev 1.7	456098
SFP+ 10 Gb/s and Low Speed Electrical Interface (SFF-8431)	ftp://ftp.seagate.com/sff/SFF-8431.PDF
SSI Micro Server Specification Rev 1.1.0	http://ssiforum.org/
System Management Bus Specification (SMBus), Version 2.0	http://www.smbus.org/specs/
Tabbed Routing Design Parameter Conversion Tool for Skylake Server (Purley)	554932
Tabbed Transmission Line Design Basics, Rev. 1.0	563771

Table 1-2. Reference Documents (Sheet 4 of 4)

Document	Document Number/ Source
Universal Serial Bus (USB) Specification, Rev 3.0 *Universal Serial Bus (USB) Specification, Rev 2.0*	http://www.usb.org/home
USB 3.0 Internal Connector and Cable Specification	http://www.intel.com/content/www/us/en/io/universal-serial-bus/usb3-internal-connector-cable-specification.html
USB 3.0 Radio Frequency Interference Impact on 2.4 GHz Wireless Devices White Paper*	http://www.intel.com/content/www/us/en/io/universal-serial-bus/usb3-frequency-interference-paper.html?wapkw=interference http://www.usb.org/developers/docs/whitepapers/

1.4 Terminology

This section defines the conventions and terminology that are used throughout the design guide.

Note: The SoC EDS shows the active-low signal names that end with "N". Customers may also find the "_B," and "#." The PDG may show some of the same signals ending with the "#" designation.

Table 1-3. Terminology (Sheet 1 of 2)

Term	Description
ACPI	Advanced Configuration and Power Interface
Aggressor	A network that transmits a coupled signal to another network.
anti-etch	An anti-etch is any plane-split, void, or cutout in a Vcc or GND plane.
ASF	Alert Standard Format
BGA	Ball Grid Array
BMC	Baseboard Management Controller
CMC	Common Mode Choke
CMM	Chassis Management Micro-controller. An embedded controller that manages the chassis and communicating with the compute nodes that are installed into it to deliver and provide access to the chassis management functions.
crosstalk	The reception on a victim network of a signal imposed by the aggressor networks through inductive and capacitive coupling between the networks. Backward Crosstalk – Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor signal. Forward Crosstalk – Coupling that creates a signal in a victim network that travels in the same direction as the aggressor signal. Even Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction the victim is switching. Odd Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction the victim is switching.
Df	Dissipation Factor
Dk	Dielectric Constant
EHCI	Enhanced Host Controller Interface
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
flight time	A term in the timing equation that includes the signal propagation delay, any effects the system has on the TCO of the driver, plus any adjustments to the signal at the receiver that is needed to guarantee the setup time of the receiver. More precisely, flight time is defined as: The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacture conditions required for the AC timing specifications, i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver AC timings. Maximum and Minimum Flight Time – Flight time variations are caused by many different parameters. The more obvious causes include the variation of the board dielectric constant, changes in the load condition, crosstalk, power noise, variation in the termination resistance, and differences in the I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include the effects of Simultaneous Switching Output (SSO) and packaging effects. Maximum flight time is the largest acceptable flight time a network experiences under all conditions. Minimum flight time is the smallest acceptable flight time a network experiences under all conditions.
HR	Humidity Ratio
land	The contact point of a processor in the BGA package.
LPC	Low Pin Count
LS	Low-speed. Refers to trace length.

Table 1-3. Terminology (Sheet 2 of 2)

Term	Description
MMC	Module Management Controller. A manageability complex that consists of a BMC and the corresponding support logic for managing two or more nodes on a module.
overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to Vcc observability.
pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
PECI	Platform Environmental Control Interface
pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings are measured at the pin.
Power Good	Power Good or PWRGOOD (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD goes active at a predetermined time after the system voltages are stable and goes inactive as soon as any of these voltages fail their specifications.
PFT	Press-fit type
PTH	Plated-though hole
ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback is caused by reflections, driver oscillations, or other transmission line phenomena.
RTC	Real-time clock
SATA	Serial ATA.
SISTAI	Signal Integrity Simulation Tools for Advanced Interfaces. A suite of Intel proprietary web-based SerDes tools necessary to design and optimize next-generation platforms containing the latest high-speed signal interfaces.
SMBus	System Management Bus
1SPC or 2SPC	One or two slots per channel
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SSO	The simultaneous Switching Output (SSO) effects are the differences in electrical timing parameters and the degradation in signal quality caused by the multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of the multiple outputs creates higher current swings that cause additional propagation delay (push-out) or a decrease in propagation delay (pull-in). These SSO effects impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets include a margin for SSO effects.
stub	The branch from the bus trunk terminating at the pad of an agent.
TCO	Total cost of ownership.
TDR	Time Domain Reflectometry
TDT	Time Domain Transmissometry
trunk	The main connection, excluding interconnect branches, from one end-agent pad to the other end-agent pad.
undershoot	The minimum voltage extending below V_{SS} observed for a signal at the device pad.
USB	Universal Serial Bus
USB-IF	USB Implementers Forum, Inc
VCC_CORE	The core power rail for the processor.
victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VRD	The Voltage Regulator Down (a down on the board solution) for the processor. This is a DC-DC converter module that supplies the required voltage and current to a single processor.
xHCI	eXtensible Host Controller Interface for Universal Serial Bus Specification Rev 1.1.

§ §

2 Platform Stack-up and General Design Considerations

2.1 Platform Stack-up

Stack-ups are shown in Appendix B with trace geometries (width and spacing) to meet different impedance requirements for the interfaces. These are accurate for an ideal board. Board vendors may change the geometries with minor deviation following their own process, but the proper geometries must be taken to meet the target impedance and tolerances shown in the tables.

Refer to Appendix B to view the details on the stack-up for each CRB.

To achieve the stack-up described in this chapter, it is recommended that board designer work closely with their PCB vendor in order to get the best combination of material/thickness.

2.2 General Signal Design Considerations

The simulations and reference platform presented in this design guide is based on the PCB technology described in this section. Intel recommends adherence to these guidelines for a plat-form based on the SoC.

Though each platform is different, similar design constraints result in boards with a similar stackup or composition. All board layout recommendations presented in this document assume a nominal stackup similar to those showing in Appendix B, "CRB 8L Stack-Up Details". If a particular design results in parameters (including manufacturing variances) fall outside of the boundaries shown, the designer must perform additional simulations to ensure proper signal integrity and specification compliance.

Variations in the stackup of a board, such as changes in the dielectric height, trace widths, and spacing, impact the impedance, loss, and jitter characteristics of all the interfaces. Such changes may be intentional or the result of variations encountered during the PCB manufacturing process. These variations must be handled properly when designing interconnects.

The Harrisonville platform boards were designed using heavy copper for power planes. Designing the power planes with less copper has not been tested and is not recommended by Intel. The customers who design boards with less copper in the power planes are responsible for simulations, analysis, and validation of the power distribution design. Refer to Appendix B for stack-up details.

2.2.1 General Routing Guidelines

The nominal stackups show respective thickness and assume following rules:

- Component placement is double-sided. Top and Bottom layers must be used to optimize DDR4 memory operations.
- Signals are routed as microstrip (outside layer) or stripline (inside layer). Both interconnect types are subject to impedance target, loss impacts etc.

Note: Specific trace width are spacing targets for various interconnects can be found in respective chapters of this document, as the compromise between impedance target, loss impacts, crosstalk immunity, and routing flexibility has to be met.

In general, stripline trace-routing is desirable. With stripline, the routed signal is sandwiched between two power (voltage and/or return) layers of the PCB. In some situations, microstrip routing (routed on the top or bottom signal layer) is unavoidable or required.

The generic microstrip geometries defined in Appendix B are implemented independent of the overall layer count of motherboard. In addition, the following general stackup recommendations are followed:

- Microstrip layers are assumed to be built from 0.5 oz foil then plated to an additional nominal 1 oz. Significant process variance around this nominal value is allowed.
- All high-speed signals should reference solid planes and do not cross plane splits. Ground referencing is preferred.
- The reference plane stitching vias must be used in conjunction with the high-speed signal-layer transitions that include a reference plane change.

2.2.2 Core Thickness and Material Considerations

Intel recommends using at least a 4.0-mil core for the baseboard used for the SoC based platform. This ensures the overall board thickness supports the thermal and mechanical validation assumptions. Pay close attention to the core material thickness used to ensure the overall board thickness meets the manufacturing design specifications. Deviating from this recommendation requires a new thermal/mechanical solution and reliability testing.

The stackup parameter ranges cover both the halogenated and halogen-free PCB materials. If the design falls within the material properties, the routing guidelines in this document are valid for both halogenated and halogen-free designs.

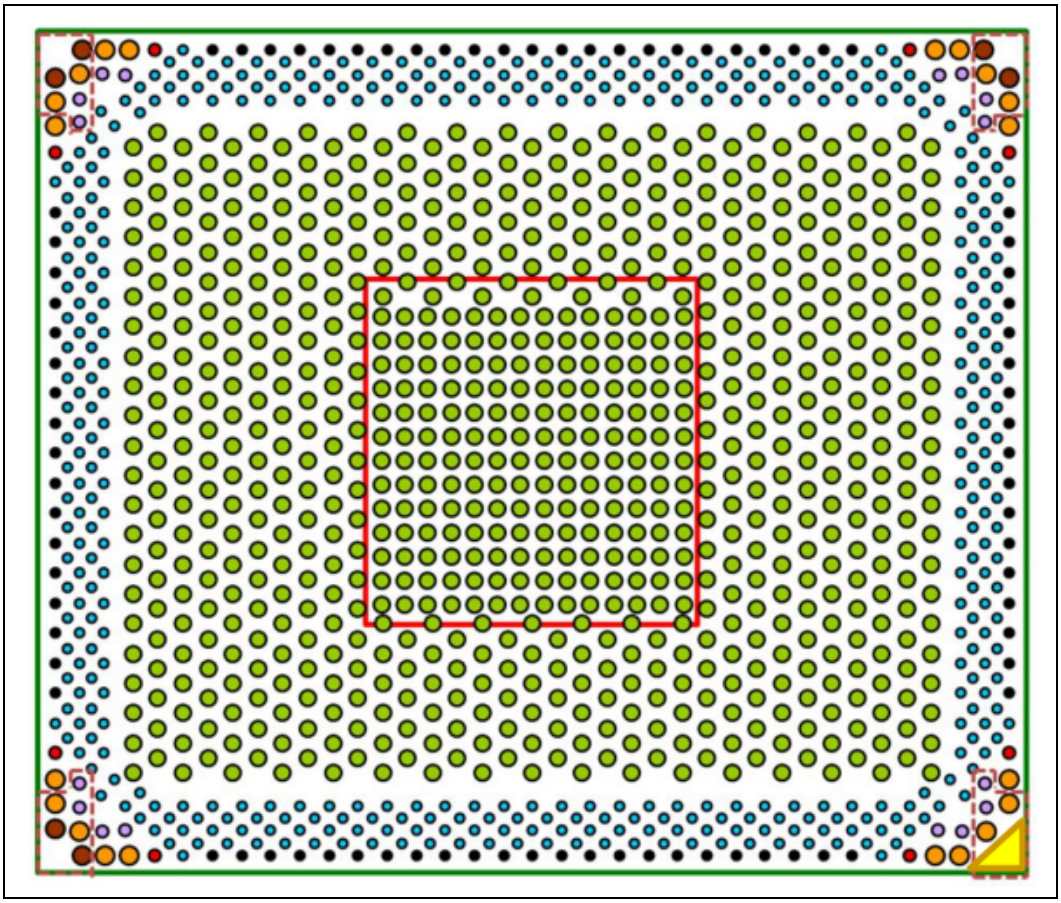
Intel recommends PCB vendors use a 1080 prepreg material or any International Electronics Manufacturing Initiative (INEMI) recommended halogen-free PCB material. A PCB stackup that uses a 1080 prepreg or the recommended halogen-free material allows for a decreased signal to reference plane height. This results in reduced crosstalk on the high-speed buses. This stackup also allows for lower trace impedances due to the thinner dielectric and lower ε_r which helps improve the flight and rise times.

Note: Other prepreg materials are available but are used only if they meet the dielectric heights and impedance requirements. If the physical parameters or impedance targets deviate from those listed in this design guide, simulations must be performed to ensure timing and voltage margins to be met.

2.2.3 SoC Footprint Considerations

The SoC is housed in a 1310 Flip Chip Ball Grid Array (FCBGA) as shown in Figure 2-1. This section details layout requirements for reliable connection and operation of the device.

Figure 2-1. SoC Footprint (View from Top)



Intel currently recommends non-soldermask defined pads (metal defined pads) for the SoC to improve solder-joint reliability. The designer needs to refer to the Denverton and Denverton-NS SoC Th*ermal/Mechanical Specification and Design Guide [TMSDG]* for detailed solder-mask guidance. Certain pad types are not allowed under the die shadow of the package.

The solder mask opening and the registration accuracy of that opening relative to the pad is critical to ensure good solder joints and minimize shorting. If the opening is too large, misregistration uncovers a nearby trace increasing the possibility of a short occurring. Regardless of opening size, misregistration causes the solder mask material to cover part or the entire pad, yielding a joint with a poor cross section (a reliability issue), or a complete open.

- Inconsistent solder mask coverage between the via and pad leads to the top and bottom side capping to avoid accidental wicking of the solder ball into the via hole. This creates an open or unreliable joint. Tenting both sides traps contaminates and moisture in the via during reflow causing severe solder mask damage as it vents. One solution is to ensure that the raw printed circuit boards are dry. An alternative is to allow for a small topside vent hole (pin hole) in the tenting.
- The solder mask requires a cap on the vias on the bottom side of the board to minimize heat transfer to the solder joints during the solder wave.

The area under the SoC outlined in red in Figure 2-1 must be free of board-mounted components. All traces must be covered in soldermask. All vias must be covered in soldermask ("tented" or "capped" vias).

The keep-out area is defined by the set of coordinates in Table 2-1.

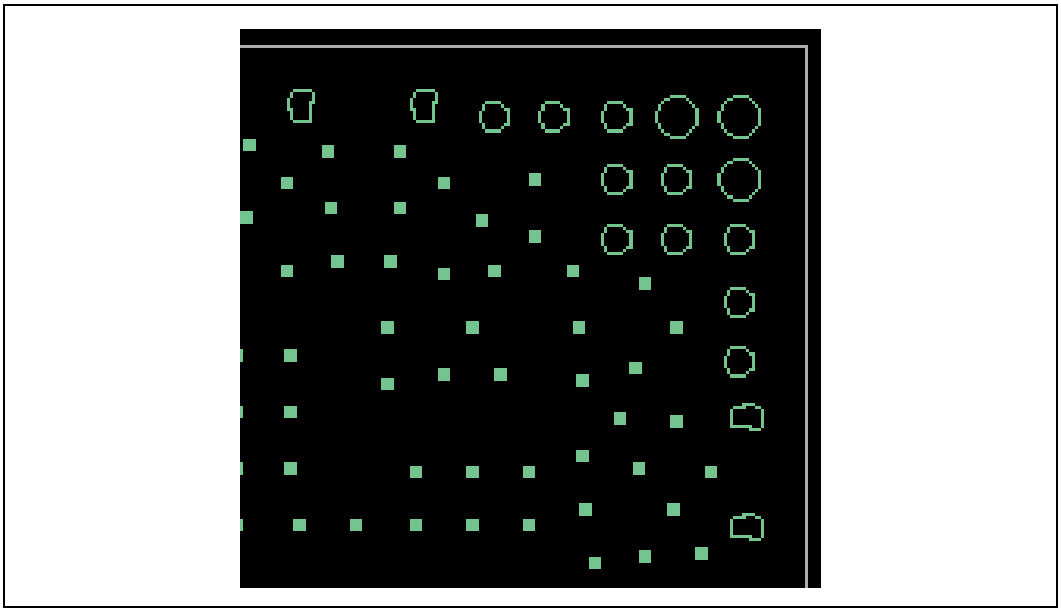
Table 2-1. SoC Keepout Zone Vertices

-6.334, 7.443	3.491, -7.458
0.300, 7.443	-4.743, -7.458
0.300, -2.046	-4.743, 3.304
3.491, -2.046	-6.334, 3.304
mm, relative to package origin	

The information shown in Figure 2-1 and Table 2-1 may not be up-to-date. To get the accurate recommended SoC footprint pad dimensions and locations, refer to the Customer Reference Board (CRB) documents. Intel provides designers an SoC logic symbol and layout footprint file to use as a reference. The pad files are also provided in case the designer has to alter them to meet specific design-house rules. The files are from the PCB design software from Cadence Design Systems, Inc*. Contact an Intel representative for details.

Figure 2-2 shows the pad detail on the package edges for round pads.

Figure 2-2. SoC Package Edge Close-Up with Round Pads



The smaller pads for the top-layer breakout are used. PCB vendors are encouraged to validate the process and equipment capabilities prior to implementation on the platform.

Note: The top-layer breakout trace routing and spacing for the SoC on the Aspen Cove Customer Reference Board support the pad sizes used: 12-mils, 14-mils, and 16-mils round pads. The minimum via-to-pad spacing will be 4.5 mils for round pads.

2.3 High-Speed Signal Trace Insertion Loss

With high speed signals, excessively high-insertion loss can dramatically attenuate the signal in long channels, reducing eye height and increasing jitter.

Excessively low insertion loss can create problems for the short, reflective channels, since the reflections are not sufficiently damped. Measuring and controlling the PCB insertion loss is critical to a successful platform design. As noted below, selecting low-loss dielectric materials is not sufficient to control loss, nor is it the most cost-effective solution to the loss problem.

High-Speed Differential (HSD) buses (excluding 10 Gb Ethernet) trace insertion loss per unit length should not exceed the profile (assumed linear) defined by the following points:

- -0.75 dB/inch at 4 GHz for stripline routing
- -0.79 dB/inch at 4 GHz for microstrip routing
- -1.50 dB/inch at 8 GHz for stripline routing
- -1.58 dB/inch at 8 GHz for microstrip routing

The insertion loss magnitude should be at least -0.55 dB/inch at 4 GHz (excluding 10 Gb Ethernet).

1. This value assumes the mixed-mode measurements of a differential response from a differential stimulus.
2. This limit is the maximum loss at ordinary lab measurement conditions as defined in IPC-TM-650 Method 2.5.5.12A (23°C ± 2C [73.4°F ± 3.6F] and 40%RH ± 5%). The design rules in this document accommodate the additional loss incurred by the laboratory environments or the final platform operating environments that are near the worst-case American Society of Heating, Refrigerating, and Air-Conditioning Engineers (ASHRAE) temperature and humidity. The ASHRAE temperature and humidity limits are described in Section 2.3.2, “Humidity Impact on Loss” on page 55.
3. This limit applies only to the PCB traces, not to any other components or to the system as a whole (in other words, this limit does not take into account vias, connectors, or any non-PCB interconnect).
4. Meeting the loss requirement does not mean that the link can meet SI performance requirements. There are many other factors such as number of via, routing layers, type of connectors, etc, that determines the SI performance together with a PCB loss target.

2.3.1 Insertion Loss and Measurement

Specifying a PCB material loss tangent or solely considering PCB material as a basis for verifying compliance with the provided loss targets is no longer sufficient. The dielectric loss tangent (*tan δ*) and the dielectric permittivity (ε_s, also expressed as dielectric constant $\varepsilon_r=\varepsilon_s/\varepsilon_0$) describe the dielectric medium's ability to convey an electromagnetic field. Historically, specifying the loss tangent of the PCB material was considered adequate to control the PCB trace insertion loss. However, at the HSD signal frequencies of this platform, several additional factors besides the loss tangent affect the insertion loss and become critical to the overall understanding of loss.

The design elements that have the largest effect on insertion loss magnitude are:

- **Loss Tangent of the Dielectric Material (also known as dissipation factor or Df):** The materials with a lower-loss tangent may or may not involve an additional expense when compared with the most common dielectric materials.
- **Glass-to-Resin Ratio:** The typical PCB materials are made from some form of woven glass fiber impregnated with various types of resin. Core and prepreg materials can vary in their glass-to-resin ratio. Resin has a higher loss than glass, so a given material that is resin rich will have a higher loss than material that is glass rich.
- **Conductor Geometry:** Copper conductors experience a skin effect at high frequencies. Electrons in the conductor tend to travel closer to the surface of a conductor within a calculable boundary called the Skin Depth that decreases with frequency. As the skin depth decreases and the electrons are forced closer to the copper surface and conductive resistance (loss) increases. Wider, thicker traces with more surface area have less loss than thin, narrow traces.
- **Conductor Material:** While copper is used extensively for the base material and its properties are consistent, plating with additional materials can have a significant effect on the insertion loss.
- **Conductor Texture:** The texture of the copper has historically intentionally been roughened to increase the peel strength and improve board strength and reliability. At current microwave frequencies, rough copper increases the insertion loss significantly. Where possible, techniques should be employed to minimize copper surface roughness while maintaining the reliability of manufacturing the PCB.
- **Manufacturing Process:** Material data sheets only document the properties of the materials used as inputs to the PCB manufacturing process. Board processing, heating, handling and other aspects of the assembly of the board components into a finished PCB can result in variations in loss.
- **Temperature and Humidity:** Water absorption increases insertion loss. Observing the ASHRAE requirements, as shown in Section 2.3.2, "Humidity Impact on Loss" on page 55, is recommended for both manufacturing of the PCBs and the operation of the final system.

Note: Although many of these elements are fixed in the platform design rules and guidelines, vendors are usually given some flexibility to modify the design slightly according to their products and processes. Attention should be paid to vendor modifications as alterations to any or all of the above elements may have a significant effect on the PCB losses measured. Further, the tolerances on all the above should be taken into account when attempting to limit the total loss of a design.

2.3.2 Humidity Impact on Loss

The dielectric loss tangent and therefore the dielectric loss increases with the humidity of the environment. The operating conditions for servers are specified by the ASHRAE document, *Thermal Guidelines for Data Centers and Other Data Processing Environments* (2004) according to whether the server application is considered mission critical (Class 1) or merely important (Class 2). All guidelines specified in this document presume that the operating environment of the server will be within the appropriate bounds specified by ASHRAE.

The electrical design guidelines in this PDG are meant for ASHRAE Class 1 and 2 machines operating within the environmental boundaries shown in Figure 2-3.

Figure 2-3. ASHRAE Class 1 and 2 Allowable Boundaries

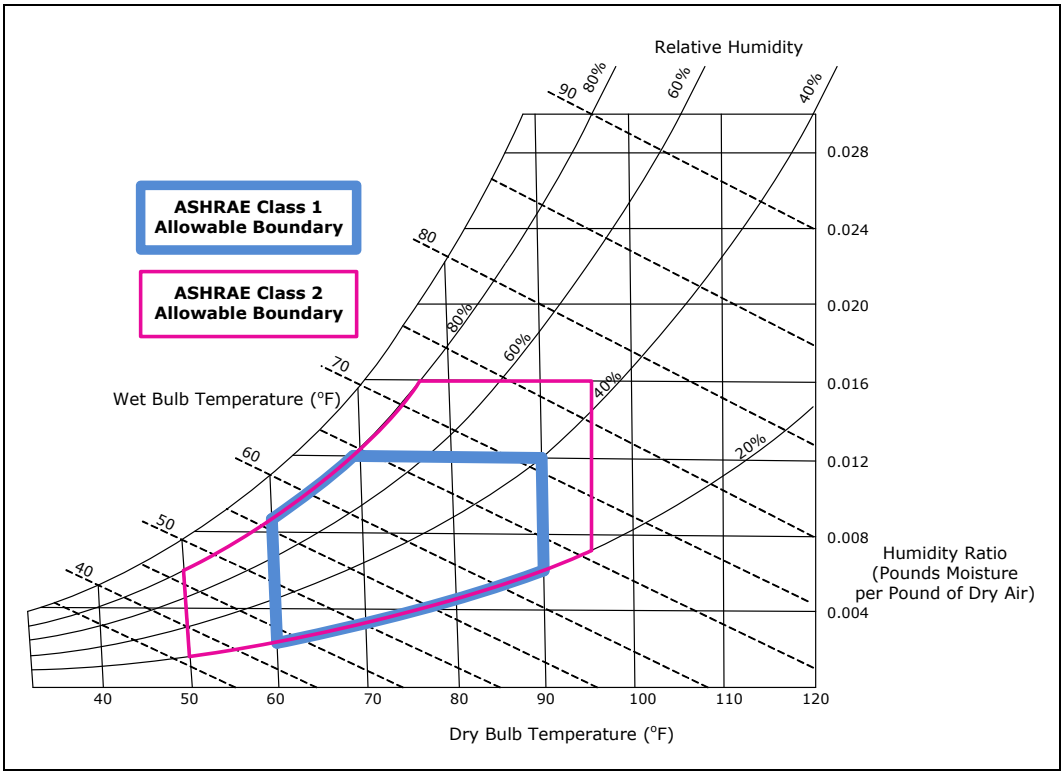


Table 2-2. Environmental Operational Boundaries

Parameter	Class 1 Range	Class 2Range	Units
Ambient Temperature	60<T<90	50<T<95	°F
Humidity Ratio	HR<0.012	HR<0.016	
Relative Humidity	20%<RH<80%	20%<RH<80%	

Board designers are advised to evaluate the dielectric materials under the worst-case environment specified by ASHRAE environmental classes, so that the loss tangent value does not exceed the simulation assumptions.

2.4 General High-Speed Signal Guidelines

This chapter contains general routing guidelines that are applicable to multiple buses presented throughout this document.

2.4.1 AC Coupling and Layout Requirements

For those interfaces requiring coupling capacitors, Table 2-3 shows the recommended values.

Table 2-3. Coupling Capacitors

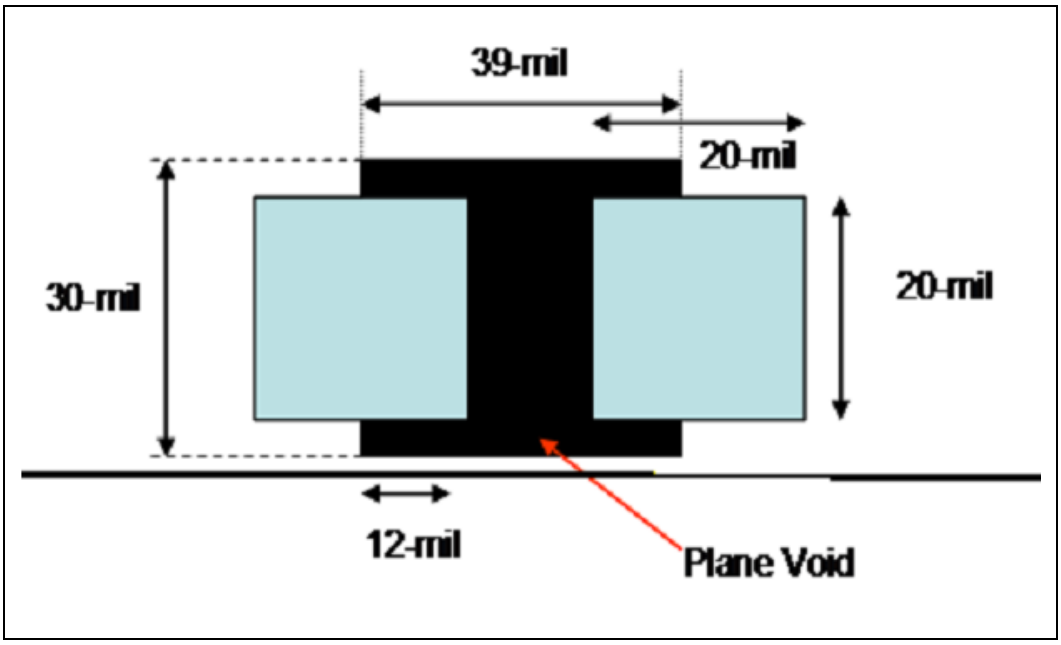
Bus	Target	Min	Max
PCIe 3.0	220 nF	75 nF	265 nF
GbE-KX, 2.5G-X, 10G-KR	100 nF	90 nF	110 nF
SATA 2.0	10 nF	9.0 nF	12.0 nF
SATA 3.0	10 nF	9.0 nF	12.0 nF
USB 3.0	100 nF	75 nF	200 nF

AC Capacitor Layout Requirement

The rectangular reference plane void shown in the Figure 2-4 is required for the AC capacitor. The voiding is only required on the adjacent reference plane. Intel recommends to use 0402-size capacitors.

- SATA 3 (6Gbps) and USB 3.0 should have the rectangular reference plane void shown in Figure 2-4 for the AC capacitor.
- PCIe (8Gbps) must have the rectangular reference plane void shown in Figure 2-4 for the AC capacitor.

Figure 2-4. AC Capacitor Layout



2.4.2 Length Matching Requirements

Table 2-4. Intra-Pair Length Matching - Segment Matching (1)

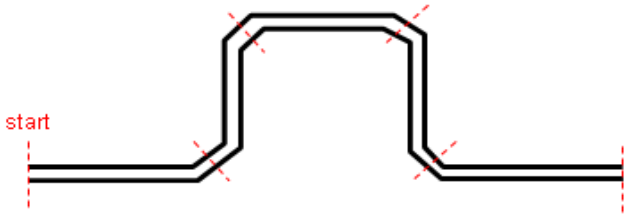
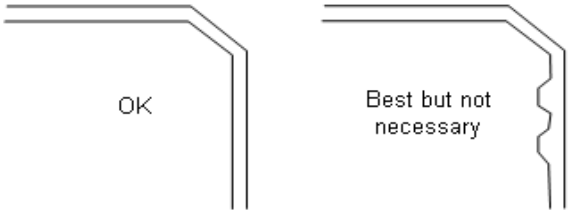
Criteria	Description
Guideline	Keep track of the intra pair running skew between D+ and D-. The recommendation is to keep the running skew less than 25 mil. In most cases, a 25-mil running skew allows for two 45° routing bends.  Definition of running skew: Traverse the differential pair from pin to pin configuration (as shown in red dashed line above), and measure the skew between the pair starting from the beginning of pin routing 
Applicable Buses	All HSD and CLKs
Purpose	Keep the symmetry of the differential pair and avoid the differential-to-common mode conversion.
Significance	Medium. A violation of the rule results in a larger common mode conversion.
Implementation	No need for segment length matching for a routing of two 45° bends as shown on the right.
Cost	Added routing complexity
Validation Tech	Visual inspection

Table 2-5. Intra-Pair Length Matching - Segment Matching (2)

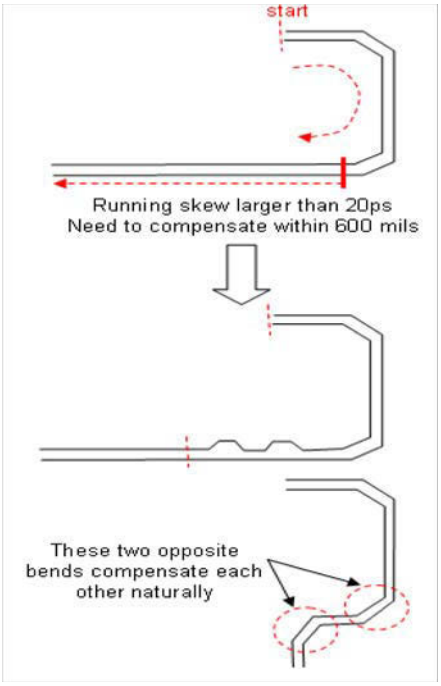
Criteria	Description
Guideline	For a skew larger than 25 mils, the mismatch needs to be compensated within 600 mils. The compensation is done using a bend in the opposite direction or adding serpentine bumps (wiggles) to the shorter one of the pair. Once the above guideline is met, further reduction in the length mismatch of the signals within a differential pair, less than 5 mils, is done at any location along the routing of the signals. 
Applicable Buses	HSD and CLKs
Purpose	Keep the symmetry of the differential pair and avoid the differential-to-common mode conversion.
Significance	Medium. A violation of the rule may result in a larger common mode conversion.
Implementation	
Cost	Added routing complexity
Validation Tech	

Table 2-6. Intra-Pair Length Matching - Segment Matching (3)

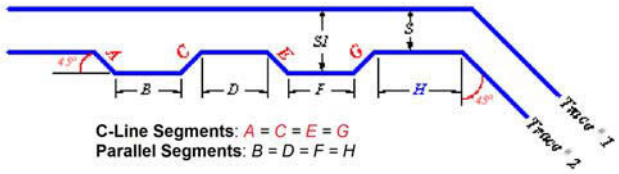
Criteria	Description
Guideline	The Figure below shows the recommended length matching serpentines. Rule: *S1 < 4S, B = D = F = H = 3w*, 45° bend, where w is the trace width. 
Applicable Buses	HSD and CLKs
Purpose	Provide a reference for length matching using serpentines.
Significance	Low to Medium. The serpentines can be slightly tweaked (e.g., *D = 4w*).
Implementation	
Cost	Added routing complexity
Validation Tech	

Table 2-7. Intra-Pair Length Matching - Segment Matching (4)

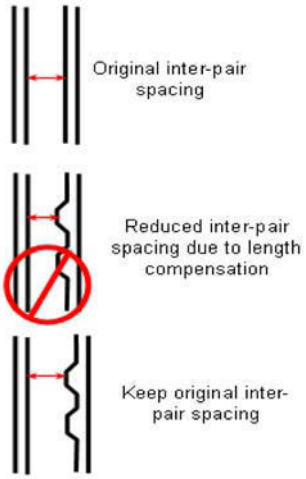
Criteria	Description
Guideline	The length mismatch compensation techniques do not reduce the interpair spacing. 
Applicable Buses	HSD and CLKs
Purpose	Reduce crosstalk from adjacent traces.
Significance	Medium to High. A violation of the rule results in a larger crosstalk coupled from nearby traces.
Implementation	
Cost	Added routing complexity
Validation Tech	

Table 2-8. Intra-Pair Length Matching - No Phase Matching Required Cases

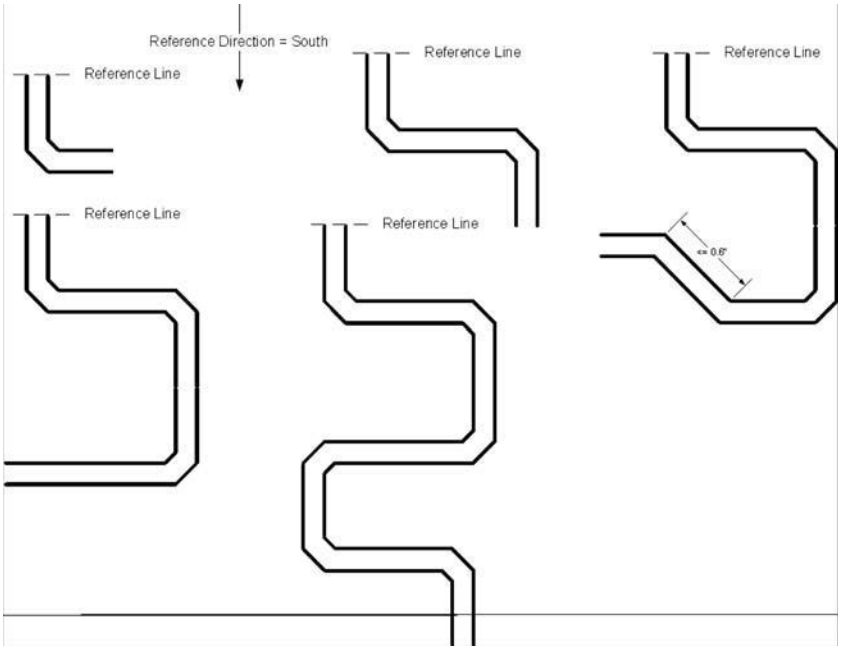
Criteria	Description
Guideline	As long as the routing angle does not exceed 90° from the reference direction for 600 mils, no phase matching is required. 
Applicable Buses	HSD
Purpose	Keep the symmetry of the differential pair and avoid the differential-to-common mode conversion.
Significance	Medium. A violation of the rule results in a larger common mode conversion.
Implementation	No need for segment length matching for a routing of two 45° bends as shown above.
Cost	Added routing complexity
Validation Tech	Visual inspection

Table 2-9. Intra-Pair Length Matching - Phase Matching Required Cases

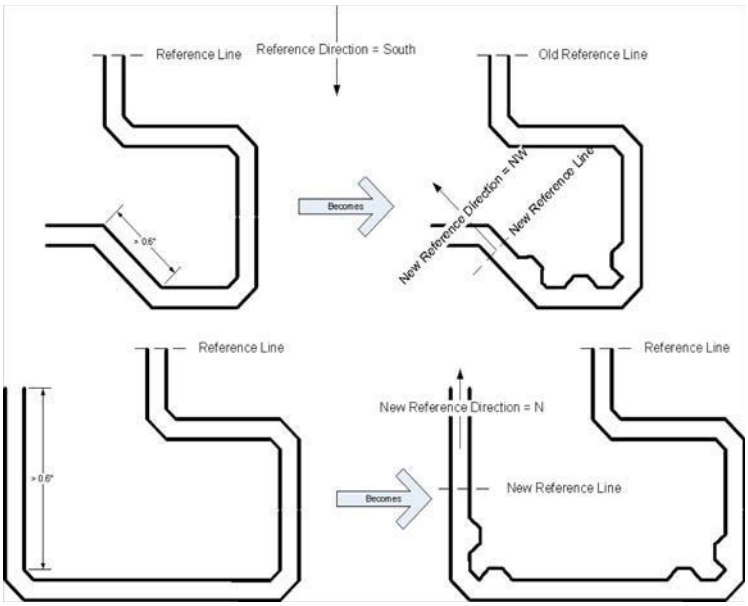
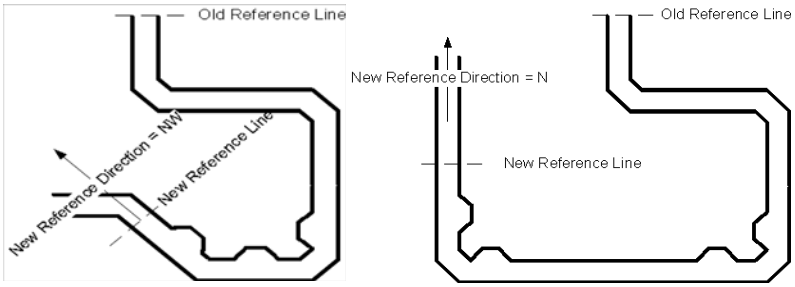
Criteria	Description
Guideline	If the routing angle exceeds 90° from the reference direction for 600 mils, phase matching is required.  Follow the same guideline after setting the new reference direction. 
Applicable Buses	HSD
Purpose	Keep the symmetry of the differential pair and avoid the differential-to-common mode conversion.
Significance	Medium to High. A violation of the rule results in a larger common mode conversion.
Implementation	No need for segment length matching for a routing of two 45° bends as shown on the right.
Cost	Added routing complexity
Validation Tech	Visual inspection

Table 2-10. Serpentine Routing Rule

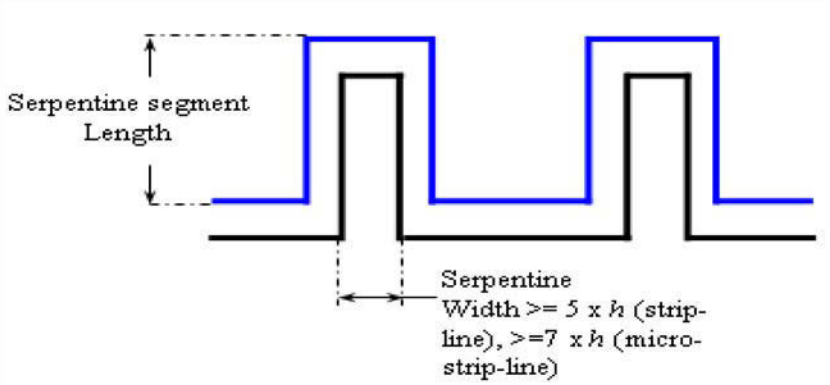
Criteria	Description
Guideline	Follow the spacing rules defined in the topology tables, or if none are provided use these general rules - Spacing: ≥ 5*h* for stripline, ≥ 7*h* for micro stripline. If the spacing rules are followed, then the serpentine segment length does not require constraining. 
Applicable Buses	All HSD, CLKs, and DDR4
Purpose	Avoid self-coupling between the different segments of the serpentine.
Significance	High. A violation of the rule results in self-coupling between a different segment of the routing and a distortion of the signal at the end of the routing. A violation of the rule also results in a slight change of the trace impedance.
Implementation	
Cost	
Validation Tech	

Table 2-11. Dog-Bone Breakout Routing Rule

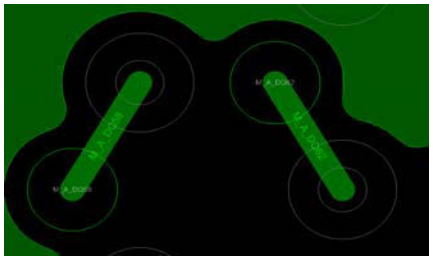
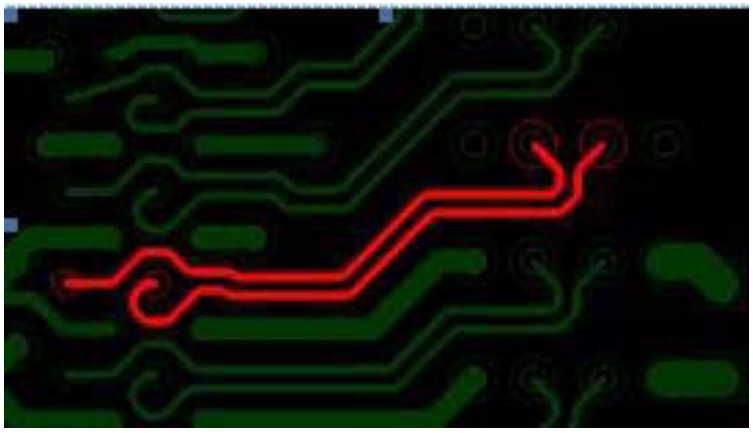
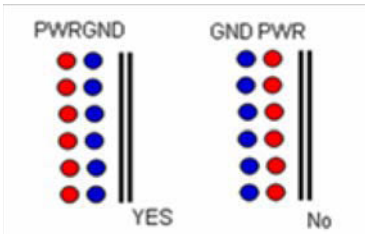
Criteria	Description
Guideline	The following rule describes the required breakout used to route between the component pad (SoC) and an inner layer transition. This is commonly referred to as the dog-bone connection. • The length of the dog-bone can vary between 15 to 30 mils (maximum). • The width of the dog-bone must follow the impedance specification for the signal. The stack-up determines the impedance for any given width. A dog-bone width, for example, for a memory data bit in a 1SPC application would be 4.25 mils if 4.25 mils gives a 50 ohm impedance value.  Dog-bone is not needed for microstrip escape as shown below. 
Applicable Buses	All HSD signals which require a transition from the top later of a component to an inner layer.
Purpose	Provide specific guidance to minimize impedance discontinuity and to provide the dog-bone breakout with min/max length checking tools.
Significance	Medium to High. A different dog-bone structure needs careful signal integrity analysis to assess the risk.
Implementation	
Cost	
Validation Tech	

Table 2-12. Routing Clearance from Antipad

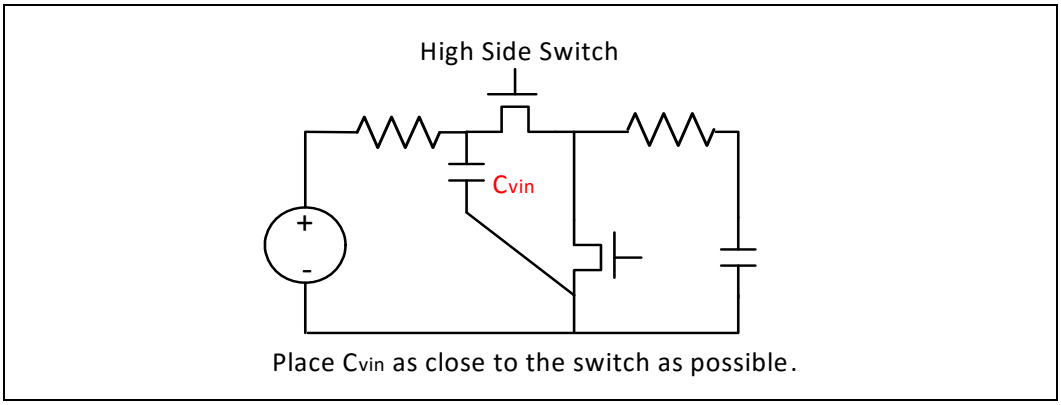
Criteria	Description
Guideline	Recommendations for minimum signaling impact are: • 5*h* for fast-switching power signals (>1 A/ns) Violations - two (maximum) allowed at > 3*h*, if and only if, the signal is not routed at worst case conditions (i.e., maximum length, longest via stub, etc.). • 3*h* for other high-speed signals Violations - two (maximum) allowed at > 0*h*. • 2*h* for static, low-current signals or same type of signal – Rx or Tx Violations - four (maximum) allowed at > 0*h*. • > 0*h* for mounting hole antipads. If the signal has violations in several or all cases above, then the maximum count is not applicable and the situation requires review by the signal integrity expert. Other guidelines: The power supply vias have Vss vias in proximity (≤ 50 mils). Intel does not recommend a route through a via field (power or other type of signals) except the escape routing from Tx and Rx. If many power supply vias (more than five) are placed as a via field, then the Vss vias are paired to the Vcc vias and the Vss vias are placed between the signal traces and the power supply via field. 
Applicable Buses	HSD, PCIe*, USB 2.0
Purpose	To minimize the impedance discontinuity and ensure the signal integrity of the routing trace.
Significance	High. Impact on the trace impedance discontinuity and crosstalk.
Implementation	
Cost	Added routing complexity and congestion.
Validation Tech	

2.4.3 Controlling Voltage Regulator (VR) Noise

The routing of nets or vias near the voltage regulator (VR) may result in a high amount of noise coupled onto critical signal traces or vias, causing significant signal integrity problems. This section provides recommendations for controlling such noise sources or limiting such noise induced by fast switching (high *dv/dt* or high *di/dt*) VR nodes onto all neighboring or adjacent data, control, analog traces, and vias of the PCI Express*, DDR4, clock, and other miscellaneous signals. The preference is to avoid routing signal traces or vias in the proximity of the VR area. In addition, the following guidelines need to be followed:

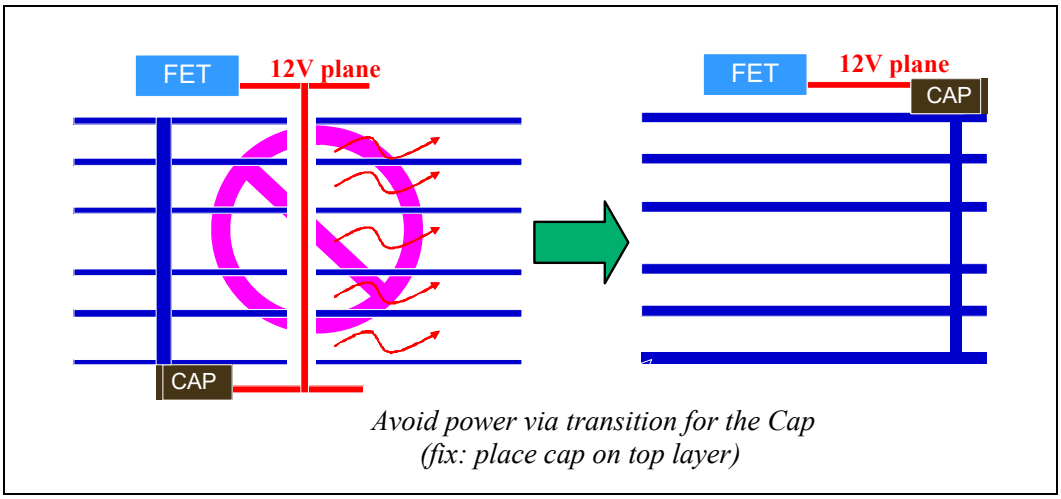
- Place decoupling capacitors (C_{VIN}) for the 12V or 5V planes as close to the high-side and low-side switches to minimize ground bounce caused by the current loop change. This is shown in Figure 2-5.

Figure 2-5. Decoupling Capacitor Placement at the VR



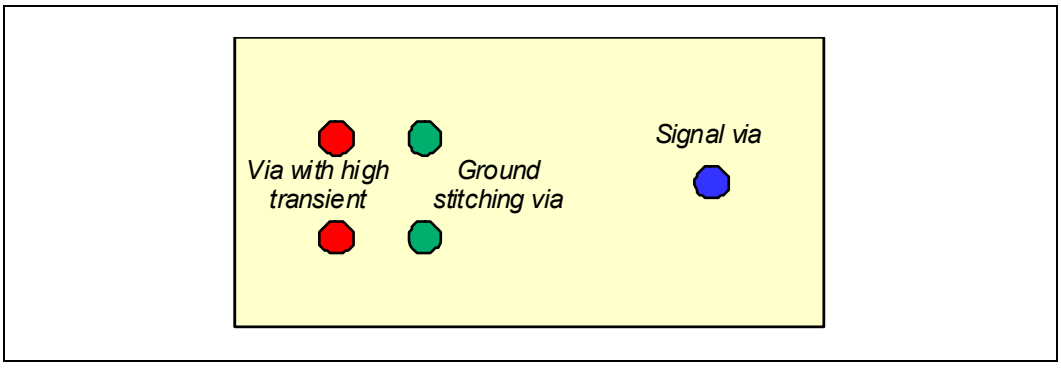
- Avoid via transition for pins with high *dv/dt* or *di/dt* transients. Extra care must be taken on the decoupling capacitor power vias. Although the voltage is held constant or under low fluctuations, these vias carry extremely high *di/dt* transients during switching events and inductively couple a significant portion of the noise to the adjacent or closest signal vias. See Figure 2-6.

Figure 2-6. Avoiding Via Transitions of High-Switching Current Nets



- If the via transitions are not avoided, the ground-stitching vias must be placed next to the aggressor vias as shown in Figure 2-7.

Figure 2-7. Placing Ground-Stitching Vias as Shields

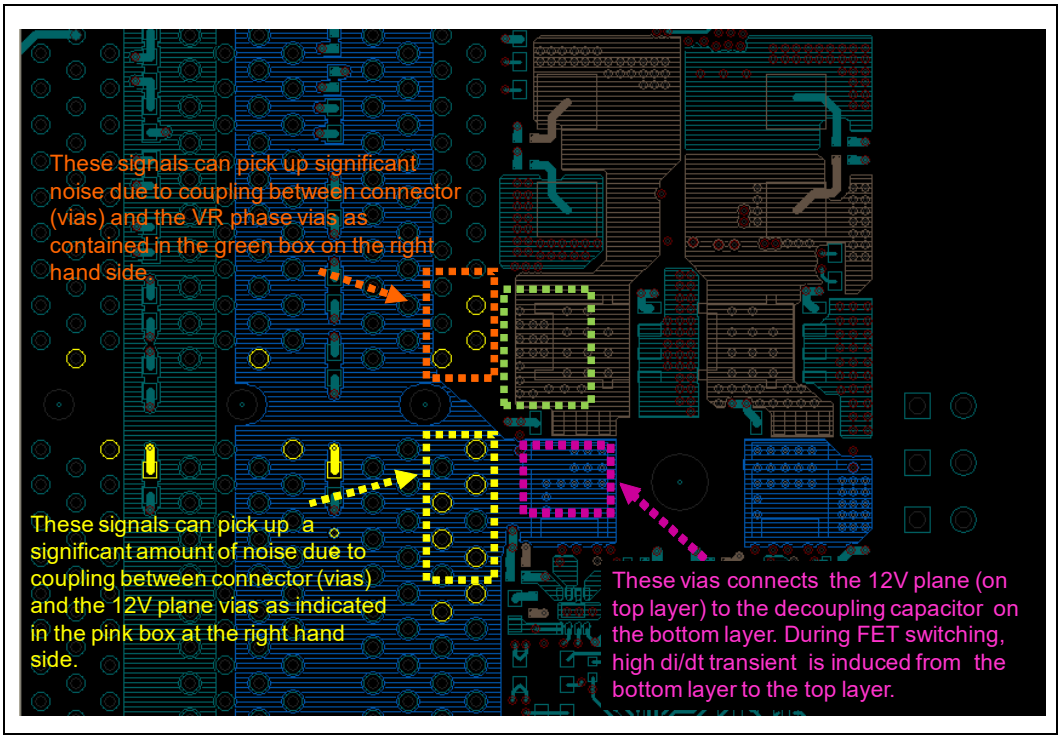


Further attention needs to be paid to the routing of Ugate, Lgate, and Phase nodes/ traces of the VRs due to significantly high *di/dt* values. The width needs to be as wide as possible and the length as short as possible to reduce the overall impedance and inductance. Try to avoid a transition between the layers with vias, but if required, use multiple vias and strictly follow the other design guides as suggested. Route each channel Phase and Ugate trace as close to each other as feasible.

2.4.4 Layout Pitfalls Examples

The layout of a problematic design is shown in Figure 2-8. The 12V plane (not shown here) is on the top layer. The decoupling capacitors for the 12V plane are placed under the bottom layer, and the connections have to be made through vias as shown in the purple rectangular box in Figure 2-8. During FET switching events, the current is charged/discharged from the capacitors at the bottom layer and transitions through these vias. These high *di/dt* vias do couple noise to the signal vias nearby. In this case, the reference design platform has DIMM connectors placed in proximity, and the connector critical signal vias pick up a significant amount of this noise, thereby causing signal integrity problems to these signals.

Figure 2-8. Problematic Customer Reference Design Illustration



The noise coupling is reduced or eliminated by removing the via transition (have to place decoupling capacitors on the top layer) as shown in Figure 2-5 and Figure 2-6, or adding ground-stitching vias next to the aggressor vias as mentioned in Figure 2-7.

Table 2-13. Routing Clearance from VR Vias

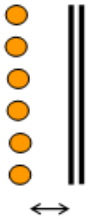
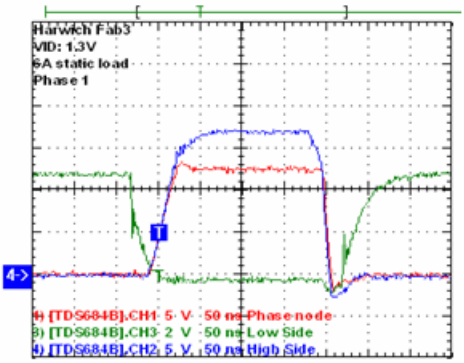
Criteria	Description
Guideline	The high-speed differential traces are routed 10*h* away from the VR vias that have high *dv/dt* switching noise (typically phase nodes in the VR). The high-speed, single-ended traces should be routed >100 mils away from the VRM vias that have high *dv/dt* switching noise. ***Note:*** (*h* is the dielectric height between the signal and ground plane.)  At lease 10h away from edge of anti-pad for phase node vias (with High dv/dt switching noise)  *Example of the phase node voltage waveform*
Applicable Buses	HSD/DDR/Clocks
Purpose	To minimize the discontinuity of the routing trace and ensure the signal integrity of the routing trace.
Significance	High. Violation of the rule results in noise coupling from the VRM via switching noises.
Comments	Added routing complexity and congestion.

Table 2-14. Power Noise Coupling to Signal Traces

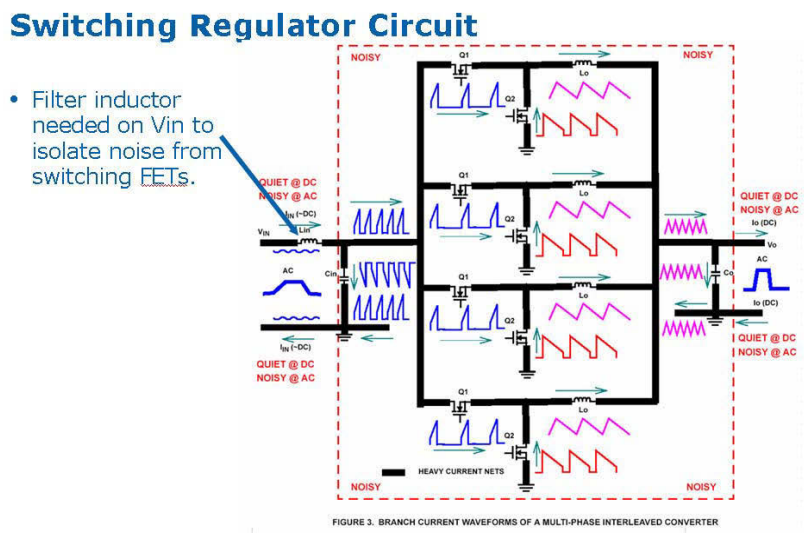
Criteria	Description
Guideline	First Option (most recommended): • A LC filter on input for any switching VR using 12V • A low-pass LC filter between the switching FETs and the 12V voltage plane to eliminate *dV/dt* • Avoid VR FETs switching nodes >50 mils Second Option: • Avoid critical nets under the 12V plane - eliminates noise coupling path Final Option (**risk mitigation strategy, not full solution, to be avoided**): • Capacitor decoupling around the critical net crossings • Distributed low-pass filtering • A high-frequency capacitor every 1 - 2 in^2 • Route critical nets away from the >1000-mils VR footprint (area with FETs) • A GND plane close to a 12V plane (PWR/GND sandwich) • Signal integrity validation under full loading conditions, OS testing • No 100% mitigation, just risk reduction • Challenging for IBIST/REUT validation  FIGURE 3. BRANCH CURRENT WAVEFORMS OF A MULTI-PHASE INTERLEAVED CONVERTER
Applicable Buses	HSD/DDR/Clocks
Purpose	To prevent a 12V VR switching noise from coupling onto the signaling lines on the adjacent layers
Significance	High. Single-ended or common-mode noise coupling results. Expect a >10% noise coupling when the nets are routed under the 12V plane.

Table 2-15. Reference Plane Clearance

Criteria	Description
Guideline	The preference is to use GND reference only. The PWR/GND dual reference is used with care: • Keep a complete GND plane. • Avoid routing over the split PWR plane. • Need to keep *S* ≥ *20h* from the edge of the plane to the edge of the trace for long signal traces routed in parallel to the edge of the planes (or partial planes). ***Note:*** (h is the dielectric height between the signal and ground plane.) 
Applicable Buses	HSD/DDR/Clocks
Purpose	To reduce the system noise on the power bus.
Significance	High. Violation of the rule results in a larger noise on the power bus, or a coupling of the power bus noise to the signal traces.

Table 2-16. Routing over Split Power Plane

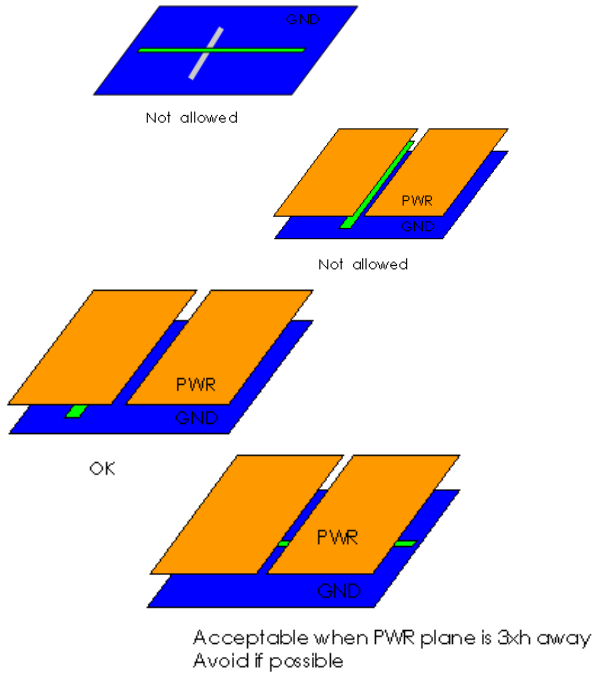
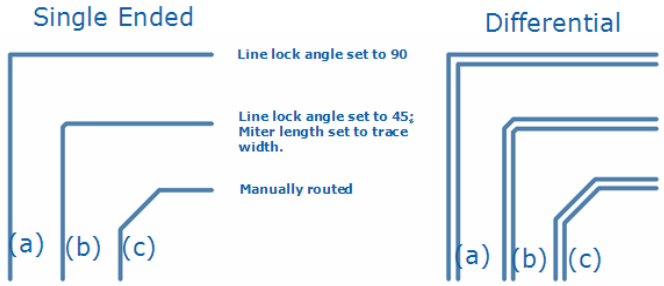
Criteria	Description
Guideline	1. (Required for signaling.) The signal is not routed over a split ground plane. 2. (Suggestion is to mitigate EMI.) The signal is not routed along the edge of a split power plane. The 5*h* spacing (minimum) from the signal to the edge of a split (20*h* recommended). ***Note:*** (*h* is the dielectric height between the signal and ground plane.) 3. (Required for signaling.) The signal is routed over a split power plane if there is already a complete ground reference plane, and the power plane is 3*h* away. **Warning** - The 3*h* far-reference rule does not protect against a 12V power plane referencing, since the AC noise on the 12V plane is large enough to cause significant crosstalk even at 3*h* spacing. Avoid the 12V power plane as far-reference. 4. (Suggestion is to mitigate EMI.) Limit the signal length in a plane split to 20 mils or less. (Avoid this scenario.) As stated above, do not have the signal dwell by the plane edge or route along the edge for any amount of distance. 
Applicable Buses	HSD/DDR/CLKs
Purpose	To ensure the signal integrity of the routing trace (1 and 3 above). To reduce the system noise on the power bus (3 above). To reduce EMI of the system (2, 3, and 4 above).
Significance	High. A violation of the rule results in larger noise on the power bus, an EMI failure, or a coupling of the power bus noise to the signal traces.

Table 2-17. Trace Corners

Criteria	Description
Guideline	Below are the three common options for routing 90° corners: • Right-angle routing is done with no change in trace width. This adds a small excess capacitance to the trace. This technique is acceptable (and is required in some instances such as in pin fields), but options (b) or (c) shown in the Figure below are preferred for best signal integrity. • A slight miter or chamfer is added to reduce or eliminate the excess capacitance. This is automatically performed by most routers with simple option settings. The drawback to this approach, compared to (c), is adding length to the bus. • Manually routing to transact the orthogonal traces at 45° eliminates the excess capacitance and also minimizes the trace length. • Option (c) is preferred for minimizing routing length. Option (b) is acceptable if the length is not an issue (for faster routing). Option (a) is acceptable where neither (b) nor (c) is used. 
Applicable Buses	HSD/PCIe*
Purpose	Reduce length mismatch and discontinuity.
Significance	Medium. Large numbers of bends as shown in (a) cause accumulated common mode noise effects. Option (c) is preferred for best signal integrity performance.

2.4.5 Escape Routing Guides

Table 2-18. Trace Necking

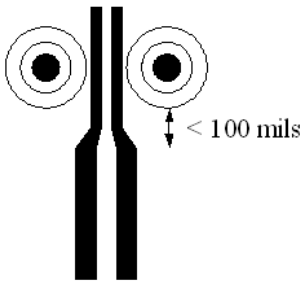
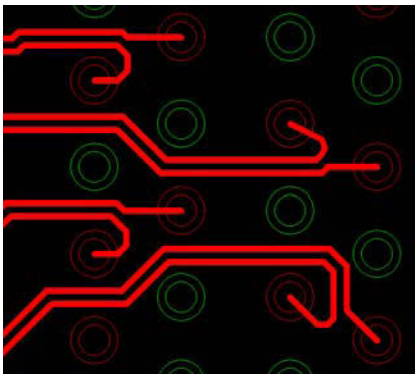
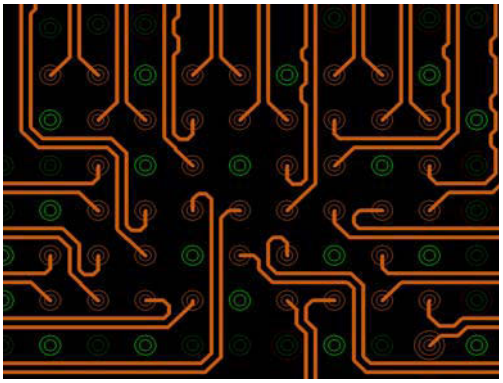
Criteria	Description
Guideline	When a differential pair escapes the pin field area with narrow traces, it needs to fan-out symmetrically to a wider trace within 100 mils from the edge-of-pin field. If the escape versus the main route trace width is large (> 2 mils), then a ≤ 45°-angle-taper segment between is recommended. 
Applicable Buses	All HSD and CLKs
Purpose	To reduce impedance discontinuity and trace loss.
Significance	Medium to High. Fan-out within 100 mils helps to reduce the overall trace loss since a narrow trace typically has higher conductor loss. Low. A taper segment helps to reduce impedance discontinuity.

Table 2-19. Uncoupled Length

Criteria	Description
Guideline	Symmetric routing for differential signals is preferred. When a differential pair, however, is assigned diagonally at a package pin or escapes from a connector, one trace of differential traces possesses a longer uncoupled line. Maintain ≤ 70 mils (35 mils typical) for an uncoupled line length for the pin field escape and ≤ 100 mils (70 mils typical) for a connector escape (measured from the edge of the pad). This rule is overruled when an L-compensation is implemented. The escape from the pin possesses short routes over the antipads and is the same length between D+ and D-. Connector example: 
	Ball Grid Array (BGA) escape example: 
Applicable Buses	All HSD and CLKs
Purpose	To reduce impedance discontinuity and trace loss.
Significance	Medium to High. A violation of the rule results in a larger common mode noise which impacts the overall system signal integrity and EMI performance.
Comments	Reference Generic High-Speed Routing Guidelines Matching – Segment Matching (2)

2.4.6 Routing Through or Escaping a Pin Field

Table 2-20. Pin Field Escaping

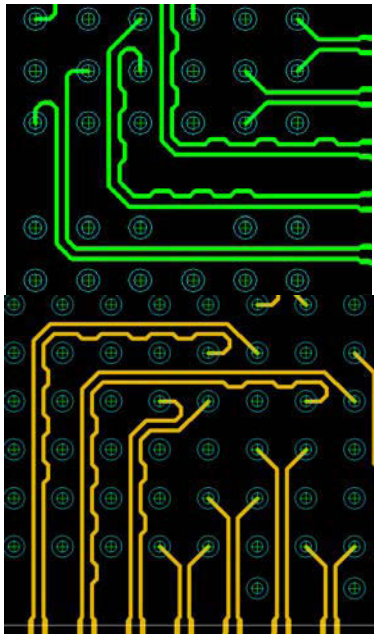
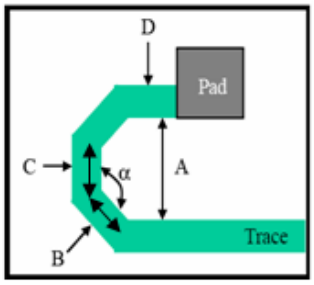
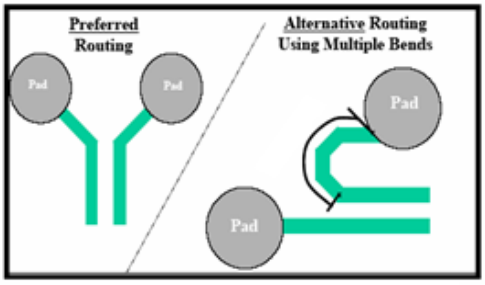
Criteria	Description
Guideline	Symmetric escapes are preferred. The Figures below show several types of escapes. 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the mode conversion (from differential model to common mode).
Significance	Medium to High. A violation of the rule results in larger common mode noise which impacts the overall system signal integrity and EMI performance.
Implementation	See the Figures below for reference. For asymmetric escapes, use bends in the Figure and minimize uncoupled length. $A \geq 3h$ (dielectric height) $\alpha \geq 135°$ B, C $\geq 1.5w$ (trace width) D: minimize  
Cost	Added routing complexity
Validation Tech	
Other Comments	

Table 2-21. Routing through or escaping a Pin Field - Example A

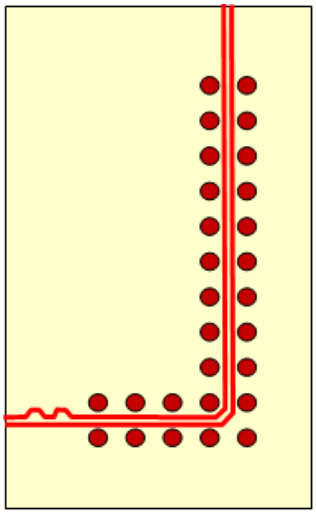
Criteria	Description
Guideline	Reduce routing length under a pin field. The drawing below shows and acceptable routing. Maximum length under a pin field varies by chip and bus. Refer to each bus section for details. Avoid routing over pin fields that have a high magnitude of transient currents (*e.g.*, power delivery pin fields). 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the amount of noise picking up from the vertical vias
Significance	High. A violation of the rule results in excessive crosstalk coupled from the vertical vias causing eye closure.
Comments	

Table 2-22. Routing through Pin Field - Example B

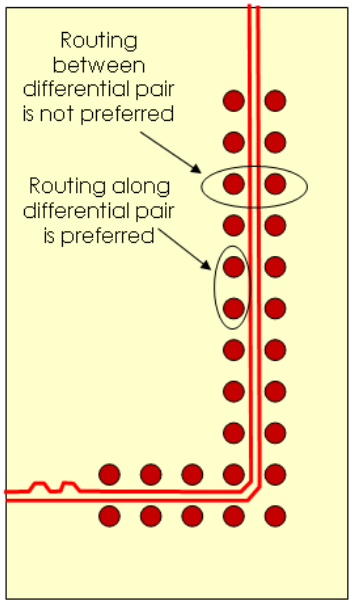
Criteria	Description
Guideline	Length matching needs to be applied when necessary to reduce the differential-to-common mode conversion. Length matching is initially done outside of the pin field to reduce crosstalk between the traces and vias. (Length matching in the pin field is generally unnecessary, unless there is not enough room for length matching outside of the pin field.) The preference is to compensate length mismatch within ≤ 400 mils from the edge-of-pin field (starting from ≤ 125 mils from the edge-of-pin field). Route a differential trace along one side of a differential via pair. 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the mode conversion (from differential model to common mode) and avoid the crosstalk between the traces and vertical vias
Significance	Medium. A violation of the rule results in larger common mode noise which impacts the overall system signal integrity and EMI performance.
Comments	

Table 2-23. Breakout Signals to Via Coupling Rules

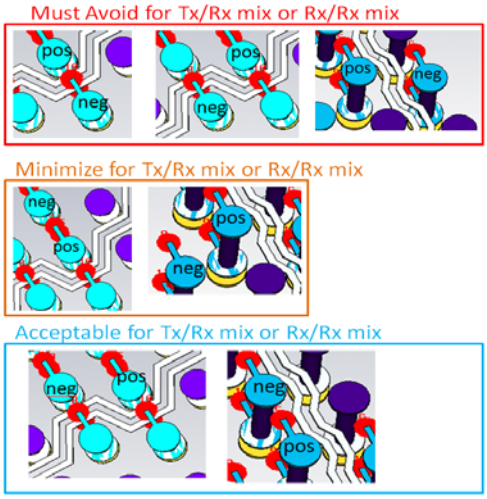
Criteria	Description
Guideline	Most Impact: • Avoid routing Rx signals through Tx P/N pairs. • Avoid routing Tx signals through Rx P/N pairs. • Avoid routing Rx signals through Rx P/N pairs (Rx of different ports/channels). • Potential impact: one Rx from the long channel and other Rx from the short channel • Each violation will accumulate to significant margin degradation. Moderate Impact: • Minimize routing Rx signals only close to one of the Tx P/N signals. • Minimize routing Tx signals only close to one of the Rx P/N signals. • Minimize routing Rx only close to one of the Rx P/N signals (Rx of different ports/channels). • Each violation will accumulate to moderate margin degradation. May be manageable, but still prefer to avoid. Desired Routing: • Route Rx signals alongside Tx P/N. • Route Tx signals alongside Rx P/N. • Route Rx signals alongside Rx P/N (Rx through Rx of different ports/channels). • No restrictions (Rx through Rx of same ports/channels). • No restrictions (Tx through Tx of same and different ports/channels). • Any combination of Tx and/or Rx, no restrictions (on bottom layer routing only). Expecting coupling to be negligible. 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the crosstalk between the differential trace routing and vertical vias
Significance	Medium. A violation of the rule results in larger crosstalk coupled from the vertical vias. A violation is determined as any instance that falls under a "most impactful" classification.
Implementation	
Cost	Added routing complexity
Validation Tech	
Other Comments	

Table 2-24. Length Matching when Routing through the Pin Field

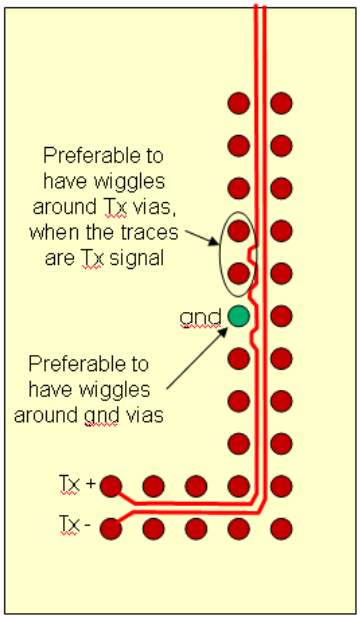
Criteria	Description
Guideline	When length matching is implemented within the pin field, place the length-matching serpentine near the ground via or similar via types (Tx via over Tx trace or Rx via over Rx trace). 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the crosstalk between the differential trace routing and vertical vias
Significance	Medium. A violation of the rule results in larger crosstalk coupled from the vertical vias.
Comments	

Table 2-25. Layer Transition and Via Stub (Sheet 1 of 2)

Criteria	Description
Guideline	Avoid a layer transition whenever possible.
Applicable Buses	All HSD and CLKs
Purpose	Reduce the discontinuities (caused by a layer transition and via stubs) along the signal path.
Significance	High

Table 2-25. Layer Transition and Via Stub (Sheet 2 of 2)

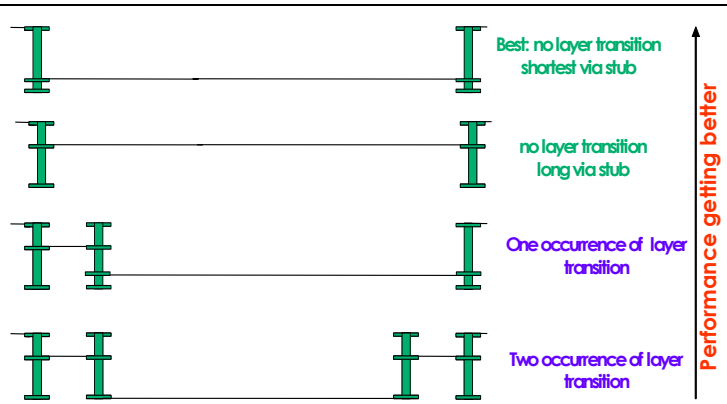
Criteria	Description
Implementation	Route the most risky signals (typically longest channel) first without a layer transition and the shortest via stub.
Comments	Refer to the other PDG chapters to determine whether the layer transitions are allowed for a particular interface signal.
Other Comments	

Table 2-26. Combining Antipad for Differential Via

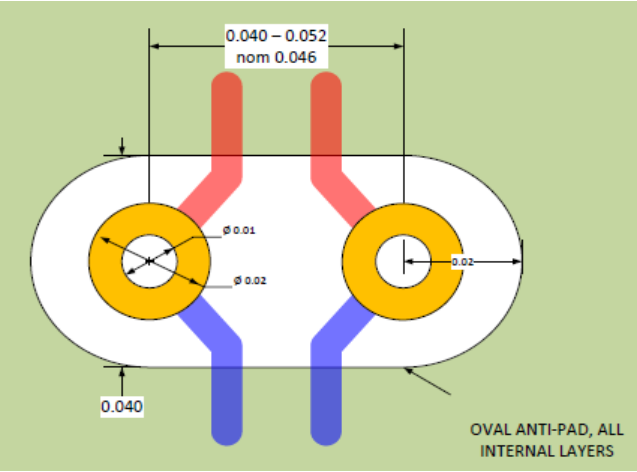
Criteria	Description
Guideline	Combining antipads together to reduce the via capacitance. 
Applicable Buses	All HSD and CLKs
Purpose	To reduce the via capacitance and improve the signal integrity performance
Significance	Low to Medium. Apply only when applicable. The benefit is expected to be small.
Implementation	Simulation is needed to determine the best combined antipad size.
Cost	
Validation Tech	
Other Comments	

Table 2-27. Via Size

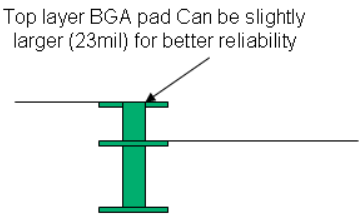
Criteria	Description
Guideline	An analysis has verified the following vias under the pin field, the layer transition, and the DC blocking capacitor connection. • (hole/pad/antipad) For a reliability reason, the top-layer Ball Grid Array (BGA) pads attached is as large as 23 mil. This has minimal impact on the signal integrity performance. The antipad design is tweaked for the best impedance matching for each particular case. 
Applicable Buses	All HSD and CLK
Purpose	A reference for the via size
Significance	Medium.
Comments	

Table 2-28. Differential Via Symmetry

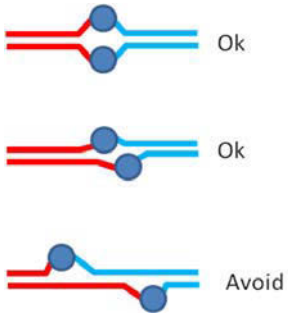
Criteria	Description
Guideline	Intel recommends symmetry when placing vias between D+ and D-. In areas where routing density is high, the two vias are slightly offset. The intra pair spacing between the two vias are kept close to each other (≤50 mil). 
Applicable Buses	HSD
Purpose	Keep the differential property of the pair for noise rejection. Keep the symmetry of the differential via to avoid differential, common mode conversion.
Significance	Medium to High. A violation of the rule results in a larger noise coupling to the signal and/ or larger common mode component of the signal.

Table 2-29. Differential Via Pitch

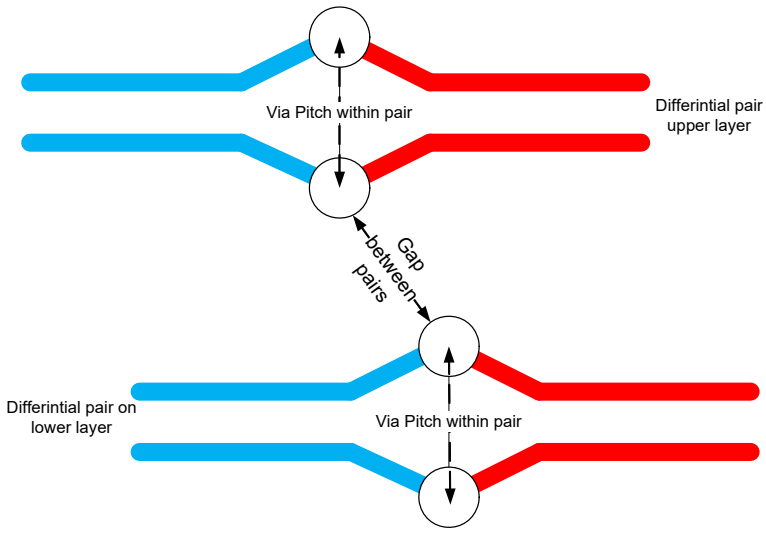
Criteria	Description
Guideline	The via pitch within a pair must be between 25 and 50 mils. The gap between the via pairs must be >50 mils. 
Applicable Buses	HSD
Purpose	Reduce the impedance discontinuity and via crosstalk at the layer changes.
Significance	Medium.
Comments	This applies to the layer changes in open field routing only. This does not apply to BGA or connector routing.

Table 2-30. GND Vias for Layer Transition

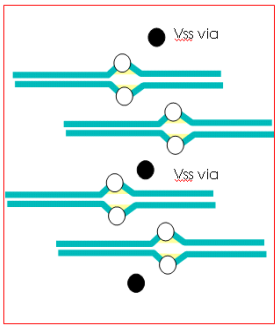
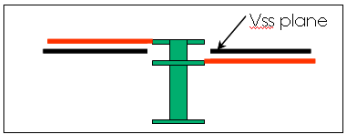
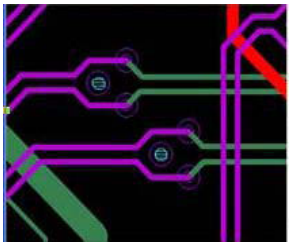
Criteria	Description
Guideline	Each high-speed signal via has a Vss via within a 50-mils gap. The spacing between the signal and ground via is larger than the intra pair via spacing so that it has little impact on the via impedance.  (a) If the layer transition keeps the same Vss plane (e.g., the layer transition from layer 1 to 3), then there is no need for the GND vias. See picture (b).  (b)
Applicable Buses	All HSD and CLKs
Purpose	Keep the return path (which is the shorting via) of the common mode signal close to the differential pairs.
Significance	Medium to High. A violation of the rule results in a larger common mode noise coupling between signals.
Comments	Consider the following layout with caution. It addresses the common mode conversion but at increased risk of pair-to-pair crosstalk. Signal integrity simulations should be run to optimize the design. 

Table 2-31. Stripped Via Pad

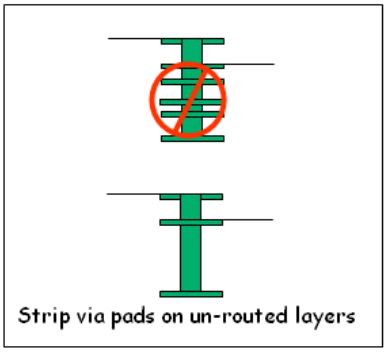
Criteria	Description
Guideline	For the best signal integrity, all via pads on un-routed layers must be removed/stripped. For board reliability, check with the particular PCB manufacturer to determine the effect of via pads on un-routed layers on the stackup. ***Note:*** The pads are not stripped in a board layout file; it is done in the Gerber file generation, or specified in a manufacturer note. 
Applicable Buses	All
Purpose	To reduce the via capacitance and improve the signal integrity performance
Significance	High. Apply whenever possible.
Comments	

Table 2-32. Via for Top-Layer (Microstrip) Routing

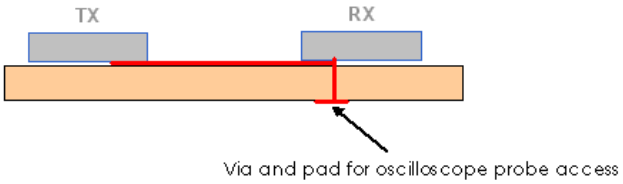
Criteria	Description
Guideline	Although no via is needed for the signal routing on the top layer, adding the via on the RX side for oscilloscope probe access may be desirable. 
Applicable Buses	All HSD and CLKs
Purpose	To improve the link observability by providing an oscilloscope accessing point.
Significance	Medium.
Implementation	The long via stub at the RX side deteriorates the link performance. This is a compromise to provide an oscilloscope probe access point.
Cost	
Validation Tech	
Other comments	

Table 2-33. Multiple Differential Via Placement

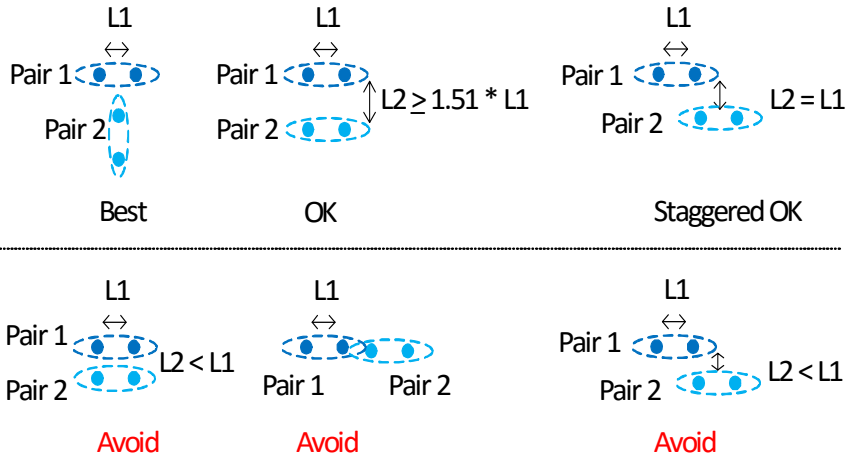
Criteria	Description
Guideline	When placing multiple differential via pairs: • Keep the intra pair spacing (L1) equal or smaller than the inter pair via spacing (L2). • Use a stagger pattern or perpendicular pattern whenever possible. • Avoid TX pairs next to RX pairs • Importance is given to the via length, data rate, and the aggressors. 
Applicable Buses	All
Purpose	Reduce the crosstalk between the differential vias.
Significance	Medium to High.
Implementation	
Cost	
Validation Tech	
Other Comments	Refer to EMI industry standards for reducing RF interference using ground stitching.

Table 2-34. Dogbone Orientation Recommendation

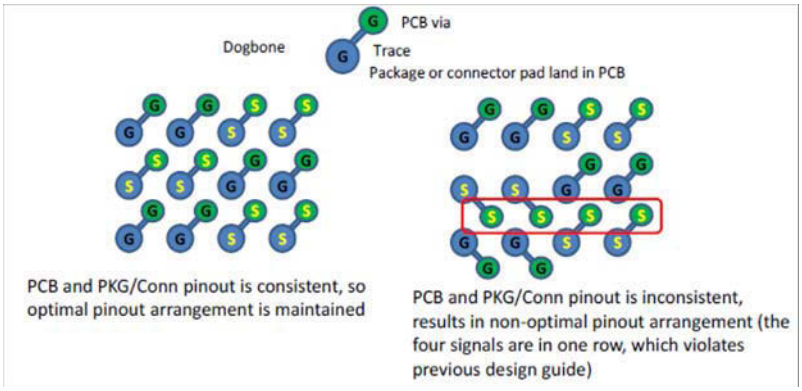
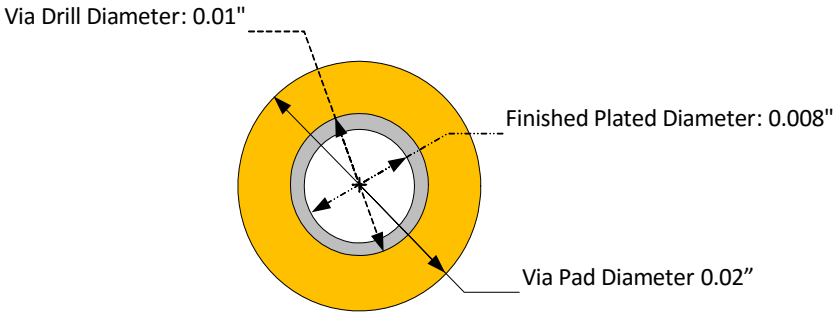
Criteria	Description
Guideline	When routing dogbone for BGA CPU/CS, or SMT connectors, following the guideline of pinout arrangement to avoid coupling violations: • Recommend to maintain the CPU/CS/connector pinout arrangement, as it should have been already optimized to avoid coupling issues • If you decide to change the pinout, ensure to not incur additional coupling to other critical signals (such as: VR switching signals, Low speed critical signals) Differential to differential pair orientation (in Table 2-33, "Multiple Differential Via Placement") must be followed.  PCB and PKG/Conn pinout is consistent, so the optimized pinout is kept PCB and PKG/Conn pinout is not consistent. Now there are two differential signal pin pairs in a row. See Table 2-33, "Multiple Differential Via Placement" for differential pair orientation violations
Applicable buses	HSIO buses
Purpose	Keep the isolation between differential, single ended and power vias.
Significance	Medium to High. Note that the coupling of the vias depends on the via length. In other words, the noise coupling is worse when the via (through portion, not including the stub) is longer.
Other comments	Refer to Table 2-33, "Multiple Differential Via Placement" for differential pair arrange allowed.

Table 2-35. Via Drill Diameter

Criteria	Description
Guideline	For best signal integrity the via drill diameter should be ≤ 10 mils. Note: This does not apply to press-fit or through-hole mount connector vias. 
Applicable Buses	All HSD and CLKs
Purpose	Reduce the via capacitance to improve signal integrity and align with PDG modeling assumptions.
Significance	High.
Implementation	All vias except those for press-fit or through-hole mount connectors.
Cost	
Validation Tech	
Other Comments	The Model User’s Guides (MUGs) contain exact assumptions for modeled via dimensions. For other via dimensions simulations or lab validation is needed to assure adequate signal integrity performance.

2.4.7 Connector Routing Guideline

Table 2-36. Ball Grid Array (BGA) and Press-Fit Type (PFT) Connector Selection and Back Drilling

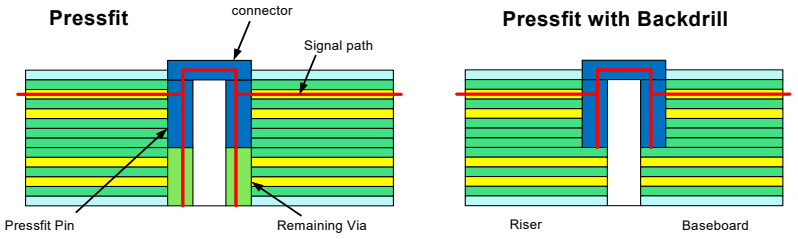
Criteria	Description
Guideline	The Ball Grid Array (BGA) connector has better performance compared to the Press-Fit Type (PFT) connector because the PFT connector has a larger pin size and capacitance. Pay special attention to the BGA pad design, a large pad increases the parasitic capacitance. Sometimes ground voiding is needed to control the excessive capacitance. For the PFT connector, back drilling improves the performance by reducing the length of the via stub. For a two-connector topology with a board thickness of > 75 mil at 6.4 Gbps or above, either the BGA connector or the PFT connector with back drilling is highly recommended.
Applicable Buses	All HSD and CLKs
Purpose	Guideline for selecting the appropriate connector type
Significance	High. Using a low-performance connector results in a large eye-opening reduction.
Implementation	The depth of the back drilling is limited because the remainder of the via needs to be at a ~60-mil range for a mechanical reason. The drill size is slightly larger than the via size, so it impacts the routing channel at the bottom layers. 
Comments	Also see the via design for the press-fit connector.

Table 2-37. Lead Length Protrusion and High-Speed Signals

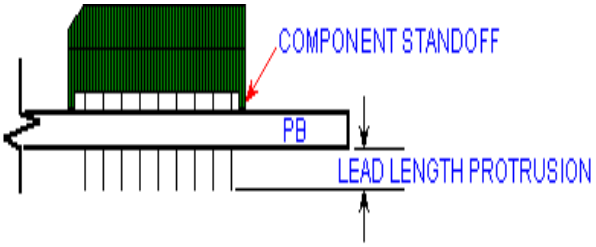
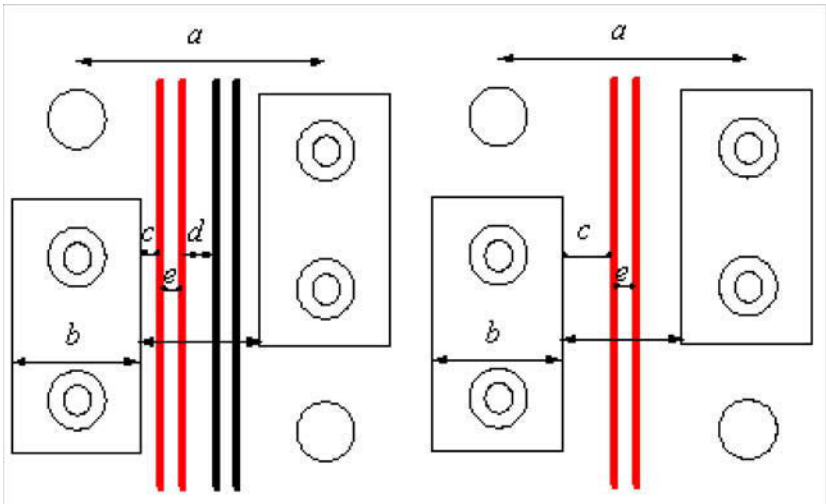
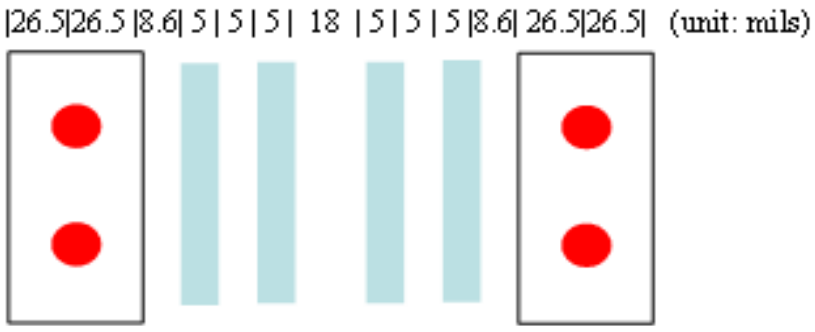
Criteria	Description
Guideline	The lead length protrusion is the lead length for the Through Hole Mount Technology (THMT) component that extends out the bottom of the board. See diagram below. Intel Designing For Excellence (DFx) rules require a minimum lead length protrusion of 0.018" and a maximum of 0.090". See *DFx 1020* http://dfx.intel.com/dfx/app/entry.asp?id=1020.  The lead length protrusion increases the capacitance on high-speed signals. Do not use a connector with lead lengths longer than necessary. The lead length or lead length protrusion is not included in the via stub length guidelines. • For 0.062" ± 6-mil stackup, the maximum connector lead length is 100 ± 10 mils (a maximum lead length protrusion of 54 mils). • For 0.072” ± 7-mil and 0.093" ± 9-mil stackups, the maximum connector lead length is 122 ± 10 mils (a maximum lead length protrusion of 67 and 48 mils respectively).
Applicable Buses	High-speed signals operating at > 5 GT/s
Purpose	The lead length protrusion increases the capacitance on high-speed signals. Do not use a connector with lead lengths longer than necessary.
Significance	Medium.
Comments	The lead length or lead length protrusion is not included in the via stub length guidelines.

Table 2-38. Backplane Connector

Criteria	Description
Guideline	For stripline routing under the 3 mm pitch connector: • Two pairs are routed; the inter pair spacing is reduced to 2.5*h*, and the spacing from the edge of the antipads is ≥1.5*h*. • Two pairs must be the same type of signals (i.e., Tx and Rx are not equally routed side-by-side in a channel). The preferred way is to route the clock signals without a neighboring pair. (Exception: the failover clock signals are satisfactory to relax the layout complexity.) *w* = trace width, *e* = diff spacing, *a* = conn pitch, *b* = conn antipad, *c* = antipad spacing, *d* = interpair spacing, e.g., for *h* = 6 mils -> *w* = 5 mils, *e* = 6 mils, *a* = 118 mils, *b* = 53 mils, *c* = 9 mils, *d* = 15 mils  For micro-stripline routing under the 3 mm pitch connector (or routing under the 2 mm pitch connector) -> only one pair is routed on a channel. (Route the traces centered between the pins with spacing from the edge of the antipads ≥3*h*, e.g., for *h* = 6 mils -> *w* = 5 mils, *e* = 6 mils, *a* = 118 to 79 mils, *b* = 53 mils, *c* = >9 mils.) ***Note:*** (*h* is the dielectric height between the signal and ground plane.)
Applicable Buses	All HSD and CLKs
Purpose	To control the crosstalk between the adjacent pairs routed under congested routing channels at the connector footprint.
Significance	High.
Implementation	An example for a two-pair routing is shown. 
Comments	

2.4.8 PCIe* General Routing Guidelines

The routing guidelines in this section apply to all the flexible I/O including PCIe *, USB 3.0, and SATA 6Gb/s design.

Table 2-39. PCIe* AC Coupling Capacitor Guide

Criteria	Description
Guideline	Locate the capacitors for the differential pair traces at the same location along the differential traces. Size 0402 capacitors are recommended. The smaller the package size, the less the inductance introduced. C-packs are not allowed for the PCI Express* AC coupling capacitor purposes. The same capacitor package size is used for each signal in a differential pair. The pad sizes for the capacitors are to be the minimum allowed. The specification requires that a value anywhere between a minimum of 75 nF and a maximum of 265 nF be used for each capacitor. **220 nF** capacitors are recommended. The tolerance values of the capacitors are irrelevant as long as the overall range of tolerances falls within the specification minimum/maximum values of 75 to 265 nF. Dielectric properties are not a major consideration for AC coupling capacitors. Any type of C0G capacitors to X7R is acceptable as long as the capacitors meet all other requirements.
Applicable Buses	PCIe*
Purpose	Maintain compatibility with the base specification.
Significance	High.
Comments	Please also consider capacitor tolerance along with temperature change while selecting the components.

Table 2-40. PCIe*, USB 3.0, and SATA 6 Gb/s Recommendations

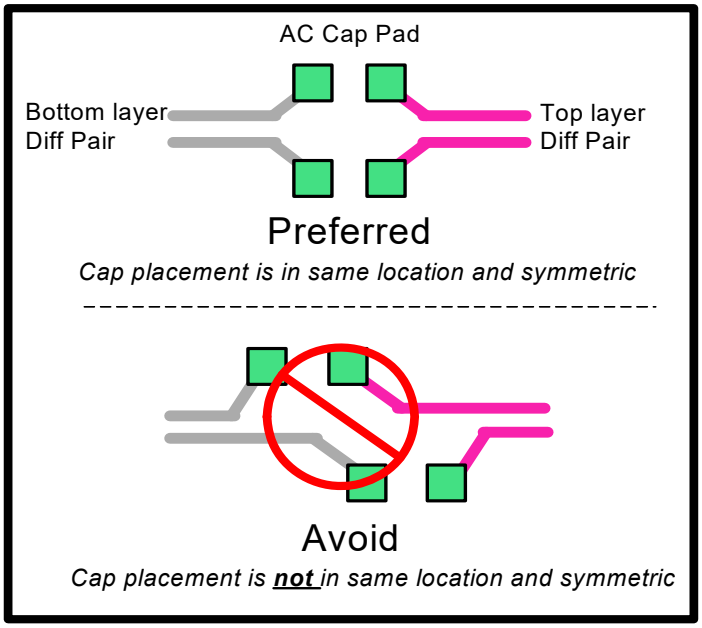
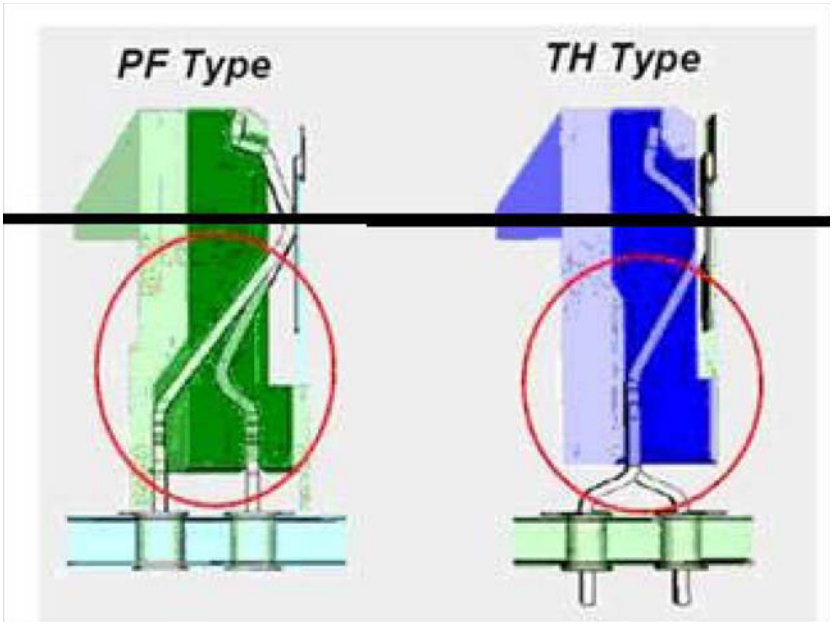
Criteria	Description
Guideline	Keep symmetry in the capacitor pad placement. 
Applicable Buses	PCIe*, USB 3.0, SATA 6Gb/s
Purpose	Keep symmetry within the differential pair to avoid the common mode conversion.
Significance	Medium to High.
Comments	

Table 2-41. Press-Fit (PFT) and Through-Hole Connectors

Criteria	Description
Guideline	Measurements have shown a significant increase in crosstalk with the press-fit connector (shown below) compared to a through-hole connector. This is due to the vertical coupling in the press-fit type connector. Through-hole connectors are recommended. When using press-fit connectors on the baseboard, validation needs to be done. On the PCIe* riser cards, PFT connectors are required for mounting on both sides. Some recent PFT connector designs have made significant improvement on the crosstalk level. 
Applicable Buses	PCIe*
Purpose	Minimizes crosstalk in the connector.
Significance	High.
Comments	The designer might need to validate the connector crosstalk to meet the design requirements.

2.4.8.1 Connector Type and Board Weave

Table 2-42. Connector Specification for Compliance to Intel® Platform PCIe* Design Guidelines (Sheet 1 of 2)

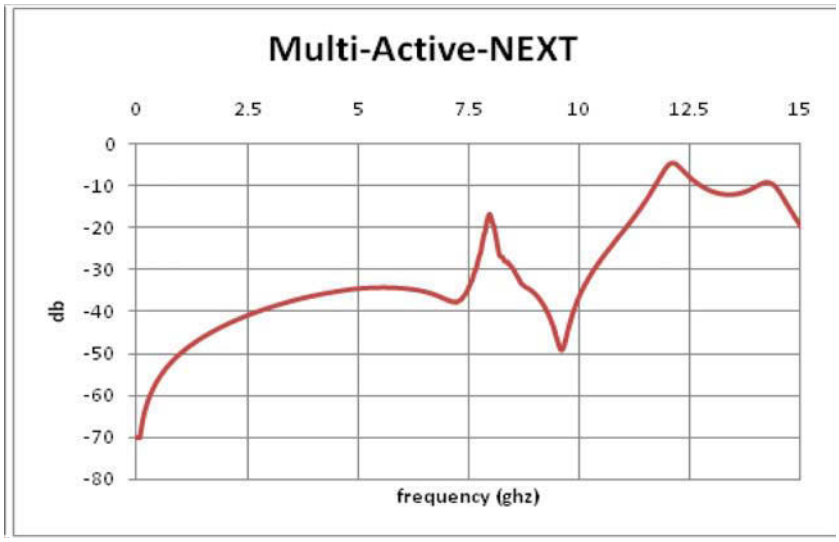
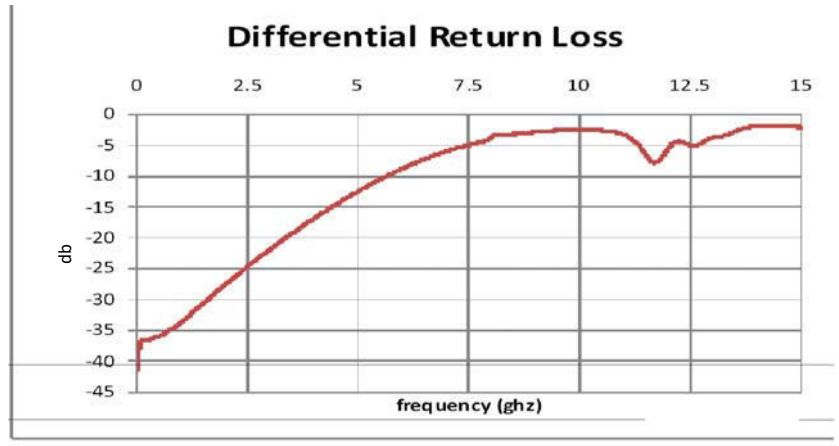
Criteria	Description
Guideline	Intel recommends using PCIe* connectors that meet the performance metrics shown below. Selecting a PCIe 1.1 compliant connector, or a lesser-performing PCIe 2.0 compliant connector, impacts the performance of the link significantly. Ensure extreme care and analysis when the connectors are not compliant with the requirements shown below, but the connectors meet the *PCI Express CEM 2.0 Specification*.
	
	

Table 2-42. Connector Specification for Compliance to Intel® Platform PCIe* Design Guidelines (Sheet 2 of 2)

Criteria	Description
	
Applicable Buses	PCIe
Purpose	These connector performance requirements ensure platforms designed to the Intel platform design guidelines satisfy the maximum platform lengths documented.
Significance	High.
Comments	The connector frequency response curves below are derived from the baseboard through the hole-mount-connector model present in the Intel® Atom™ Processor C3000 Product Family PCIe Signal Integrity Models (in accordance with the *PCI Express Connector High-Speed Electrical Test Procedure 1.0*).

Table 2-43. Insertion Loss

Criteria	Description
Guideline	The PCB trace insertion loss requirement is defined per inch for bare traces alone, without vias, connectors, or other non-trace structures. To establish whether the target platform stackup and trace geometries meet loss requirements across manufacturing variations and tolerances, use a test coupon of the design. See Section 2.2, "General Signal Design Considerations" for complete details.
Applicable Buses	High-speed signals operating at > 5 GT/s
Purpose	To identify and constrain the total PCB loss that is a significant part of the interface performance.
Significance	High.
Comments	The topologies provided in the PDG assume the PCB does not exceed the loss requirement stated in Section 2.2, "General Signal Design Considerations". PCB loss testing is intended to apply to traces only, not to complete topologies.

Table 2-44. Minimizing the effect of Fiberweave

<table>
<tr><th>Criteria</th><th>Description</th></tr>
<tr><td>Guideline</td><td>
Typical printed circuit boards, due to their basic construction consisting of woven fiberglass fabric (Er~6) strengthened and bound together with epoxy resin (Er~3.5), present a non-homogeneous medium for signal propagation of differential pairs. There are several weave types with the weave strands running horizontal and vertical relative to the board edges. For differential pairs with trace width and spacing comparable to the dimensions of the fiberglass cloth, the nonuniform dielectric PCB gives rise to substantial propagation differences between the conductors of the pair.
The table below specifies the maximum allowed routing parallel to the board edge for each transfer rate. It is given as a “Root Sum Square” (RSS, root of the sums squared) value – see note *1.
<table>
<tr><th>Transfer speed</th><th>Max RSS length (see note 1)</th></tr>
<tr><td>2.5 GT/s</td><td>10 in.</td></tr>
<tr><td>4 GT/s</td><td>6 in.</td></tr>
<tr><td>5 GT/s</td><td>5 in.</td></tr>
<tr><td>6.4 GT/s</td><td>4 in.</td></tr>
<tr><td>8 GT/s</td><td>2 in. (see note 4)</td></tr>
<tr><td>10 GT/s</td><td>2 in.</td></tr>
</table>
Max RSS length vs. Transfer Speed
Notes:
1. The lengths in the table represent total trace lengths that are aligned to the weave (i.e., parallel to the mfg. panel’s edge). Actual routing may have a significant portion of the length at angles to the edge of the board – those lengths shouldn’t be considered in this analysis.
a. The total length is the Root Sum Square of total vertical and horizontal lengths that run parallel to the weave:
$$Length = \sqrt{(H_1^{\,2} + H_2^{\,2} + H_3^{\,2} + ... + V_1^{\,2} + V_2^{\,2} + V_3^{\,2} + ...)}$$
...where H_x = length of each segment routed horizontally, and V_x = length of each segments routed vertically.
b. For multiple board topologies, the lengths on the various boards are added equally, i.e., H_1 and H_2 might represent horizontal lengths on one board, while H_3 represents a horizontal length on another.
2. This table represents an approximation only, based on simulations of a “representative” topology. The exact fiberweave effects may vary, depending on the exact topology.
3. The table assumes worst-case weave type.
4. The Max RSS length at 8GT/s can be extended to 3” for zero connector topologies for PCIe*.
</td></tr>
<tr><td>Applicable Buses</td><td>High-speed signals operating at ≥ 2.5GT/s</td></tr>
<tr><td>Purpose</td><td>Minimizes the propagation differences between the traces within a differential pair.</td></tr>
<tr><td>Significance</td><td>High.</td></tr>
<tr><td>Comments</td><td>See full discussion about Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies White Paper (#406926).</td></tr>
</table>

2.4.8.2 Recessed Ground Plane for Edge Card Connector

Table 2-45. Recessed Ground Plane for Edge Card Connector

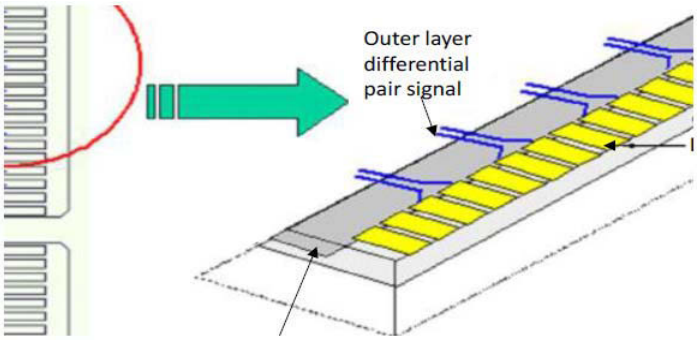
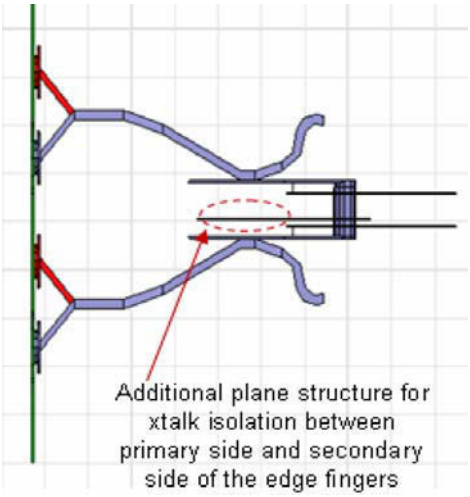
Criteria	Description
Guideline	If edge connector is used, then the ground plane underneath (layer 2 in the picture shown below as an example) should be recessed up to the tip of the edge fingers. 
Applicable Buses	PCIe*
Purpose	Recess the ground plane helps to reduce the insertion loss (S21), by reducing the excessive shunt capacitance between ground plane and the edge fingers.
Significance	High.
Comments	Recessing the ground plane can improve the signal integrity performance significantly.

Table 2-46. Cross Talk Control for Edge Card Connector

Criteria	Description
Guideline	Two approaches to control the cross talk of the edge fingers between primary side and secondary side: 1. Using the 1:1 S:G ratio pattern: Primary side: s s g g s s g g s s g g Secondary Side: g g s s g g s s g g s s 2. If 2:1 S:G ratio is used, then additional plane structures are recommended between primary side and secondary side of the edge fingers, as shown on the right. Here are two scenarios: If the two layers closest to the middle of layer stack up are power planes, then the power plane can be fully extended to the full length of the edge finger. If any of the two planes at the middle of stackup is signal plane, a small section of metal plane can be added on the same signal layer, and shorted to the ground planes by shorting vias. 
Applicable Buses	PCIe*
Purpose	To control the cross talk of the edge fingers between primary side and secondary side.
Significance	Medium to High. It is strongly recommended for ≥ 6.4 GT/s operation.
Comments	PCIe* uses 1:1 S:G ratio. HSD uses 2:1 ratio.

2.5 Audible Noise Reduction

Vibrations in power supply surface mount components that couple to the PCB can result in audible noise generation. The vibrations are caused primarily by changes in voltage (*dv/dt*) across ceramic input capacitors (MLCCs) and load current changes (*di/dt*) in the output inductor. Periodic surges in load current in the audible frequency range combined with particular components can drive board resonances loud enough to be an issue. These surges can arise, for example, from regular changes between low power sleep states to higher power run states, or from regular timer interrupts that incur higher than average processing.

Mitigations can include:

- Reduce input voltage droop: Increase input capacitance.
- Reduce output voltage droop:
  - Decrease output voltage slew rate to minimize input current. If the output voltage slews faster than needed it can worsen audible noise. A VR controller that has slew rate control with external pin is preferred for optimizing the *dv/dt* setting. Refer to the data sheet and consult with the vendor to tune this.
- Optimize input high frequency capacitance:
  - Reduce the number of MLCCs by using larger individual values.
  - Avoid Y5V type since it is much more susceptible to piezoelectric effects.
  - Use polymer chip capacitors in conjunction with MLCCs when possible.
  - Place MLCCs on either side of the regulator switching FET, not in a group on one side.
  - Place MLCCs symmetrically on top and bottom side of the board to help cancel audible noise.
- Select inductor to prevent or reduce vibration:
  - In general, ferrite is noisier than metal composite.
  - Make sure the inductor construction is rigid. The core has to be well glued together and the cavity should be filled with epoxy.

  The supplier can also provide characterization *vs*. noise given material selection and construction.

2.6 Direct Probing LAI (Logical Analysis Interface)

Table 2-47. 2 Via Structure

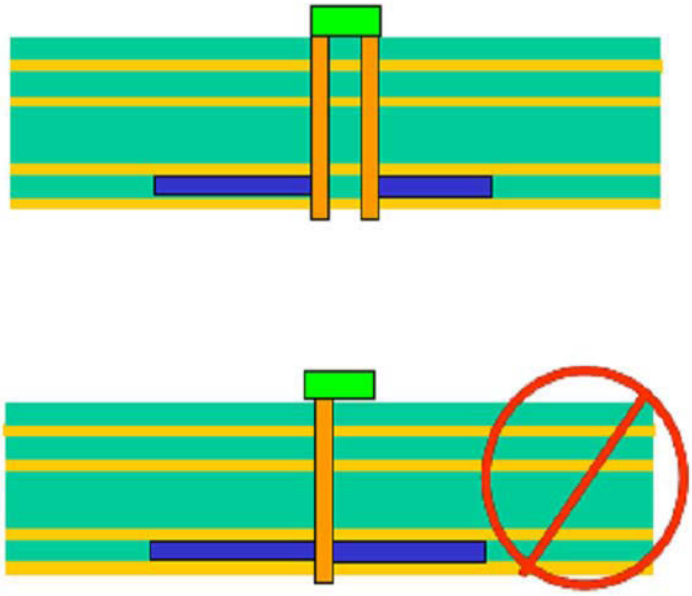
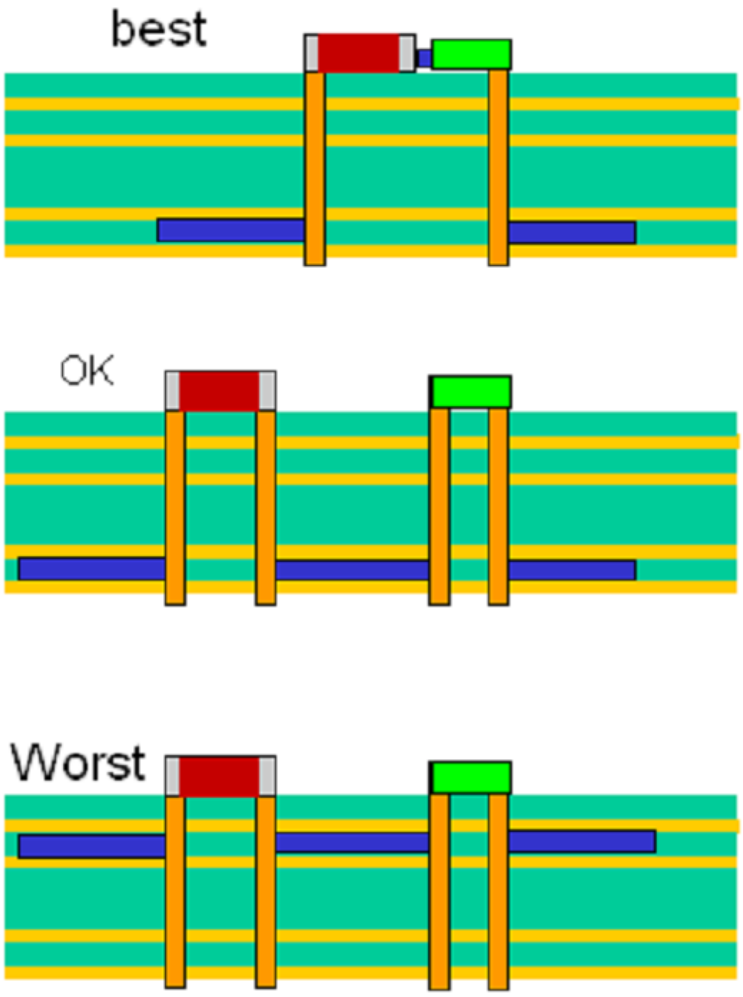
Criteria	Description
Guideline	A two-via structure is better than the one-via structure as shown on the right. The reason is that one-via structure will have big shunt capacitance, while the two-via structure has less parasitic capacitance due to the fact that the LAI pad is part of the signal path 
Applicable Buses	PCIe*
Purpose	To reduce link discontinuity and improve the eye opening at receiver.
Significance	High. Violation of the rule has significant impact on eye opening at receiver.
Comments	Must be applied.

Table 2-48. AC Capacitors With LAI

Criteria	Description
Guideline	Make the via stub as short as possible. If possible, place the AC cap as close to the LAI footprint (< 0.5 inch preferred; target 0.14 inch) to eliminate two vias. 
Applicable Buses	PCIe*
Purpose	To reduce link discontinuity and improve the eye opening at receiver.
Significance	High. Violation of the rule has significant impact on eye opening at receiver.
Implementation	Avoid the worst case scenario if possible. If due to routing constraints the worst case scenario cannot be avoided, simulation is needed to assure enough eye opening at receiver.
Comments	Must be applied.

2.7 DDR4 Tabbed Transmission Line Design

Tabbed Routing is a method of attaching small trapezoidal tabs on adjacent parallel traces to control more aggressively the mutual capacitance and inductance of the traces. This method improves the impedance of the traces and signal noise. It provides design opportunities for more compressed systems designed with high speed DDR4.

Note: Tabbed routing is not a requirement for platforms based on this SoC.

Table 2-49. Tabbed Routing Styles

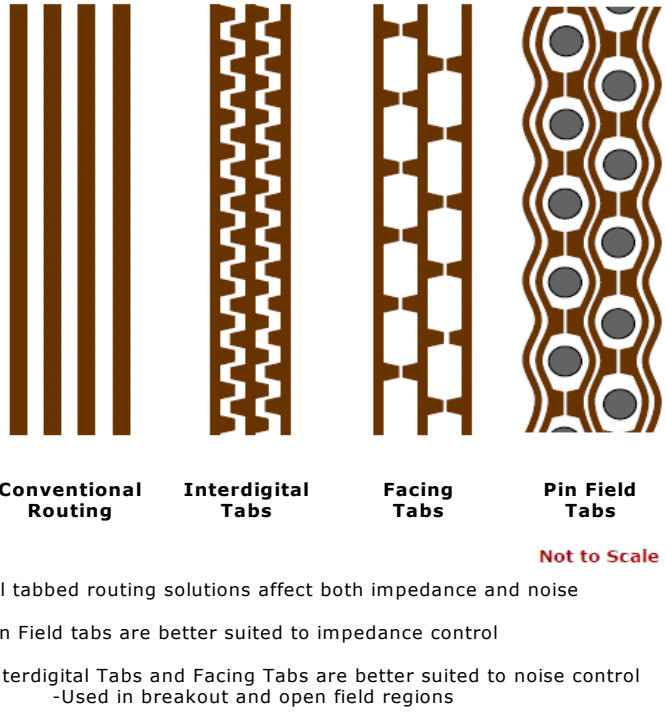
Criteria	Description
Guideline	All tabbed routing solutions affect both impedance and noise. Pin Field tabs are better suited to impedance control. Interdigital tabs and Facing tabs are better suited to noise control (used in breakout and open field regions). 
Applicable Buses	DDR4
Purpose	To optimize signal integrity with improved trace impedance to minimize noise.
Significance	High. Violation of the Tabbed Routing rules will down grade memory performance
Comments	It is recommended to achieve higher speed and higher performance on the DDR design.

Table 2-50. Pin Field Tabs

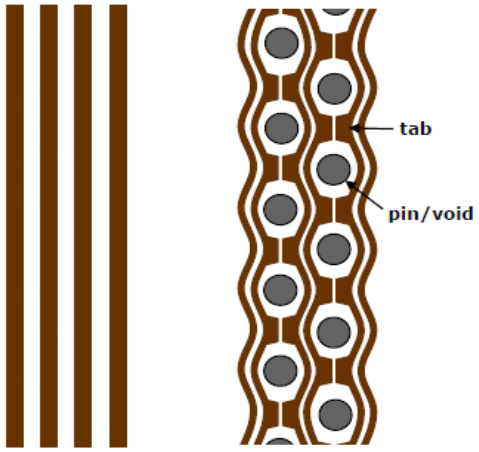
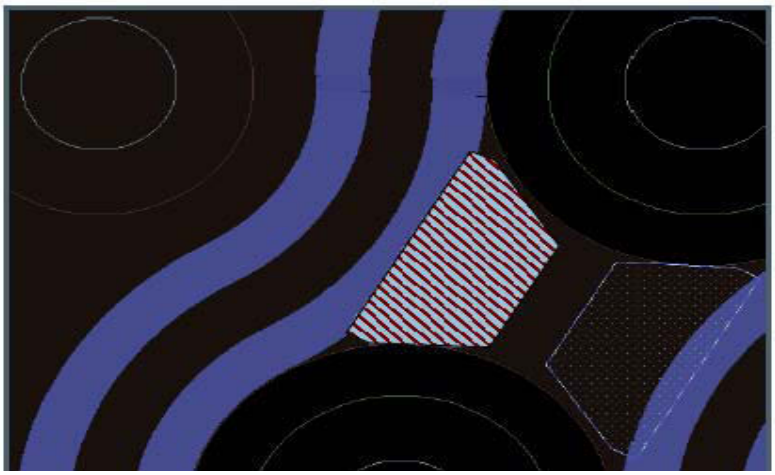
Criteria	Description
Guideline	• A Pin Field Tab refers to a wide trapezoidal tab directly opposing another such tab along two parallel traces. • Impedance control is the primary function of the pin field tab although some noise mitigation takes place. • Used in the pin field in most cases. With ground voids and narrow traces in the pin field, impedance is difficult to control. Manipulating mutual capacitance with tabs offers better impedance control. • Used on both stripline and microstrip layers in the pin field.  **Conventional Routing** **Pin Field Tabs** Not to Scale **Pin Field CAD Example.** 
Applicable Buses	DDR4
Purpose	To optimize signal integrity with improved trace impedance.
Significance	High. Violation of the Tabbed Routing rules will down grade memory performance
Comments	It is recommended to achieve higher speed and higher performance on the DDR design.

Table 2-51. Interdigital Tabs (Sheet 1 of 2)

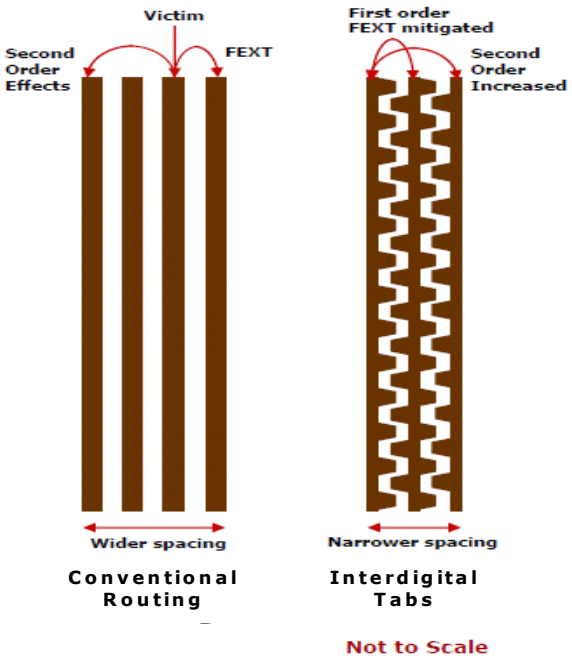
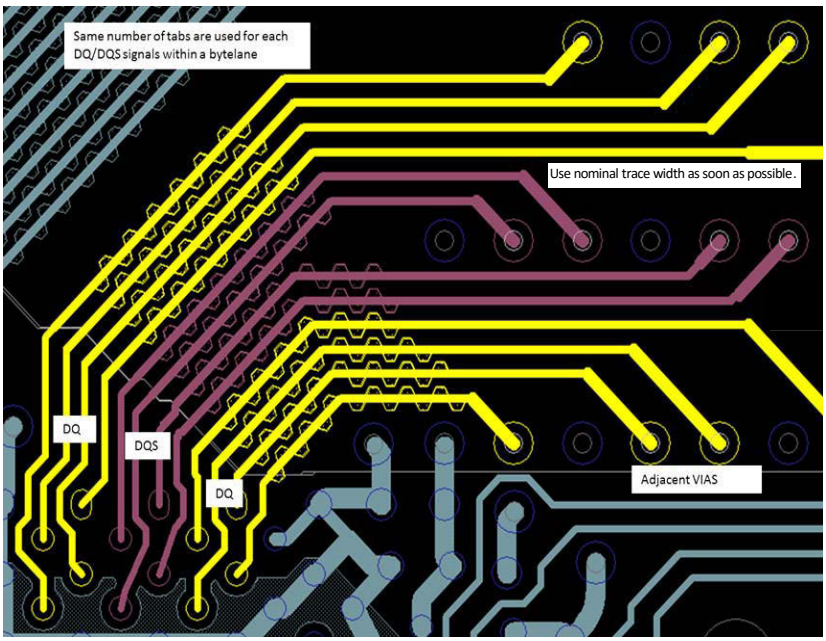
Criteria	Description
Guideline	Uses alternating trapezoidal tabs that face the gap between tabs in adjacent parallel traces. Allows for compressed routing, impedance control and FEXT (forward crosstalk) mitigation. Used mostly on microstrip layers.  Interdigital Tab Routing Example. 
Applicable Buses	DDR4

Table 2-51. Interdigital Tabs (Sheet 2 of 2)

Criteria	Description
Purpose	To optimize signal integrity with improved trace impedance to minimize first order forward crosstalk.
Significance	High. Violation of the Tabbed Routing rules will down grade memory performance
Comments	It is recommended to achieve higher speed and higher performance on the DDR design.

Table 2-52. Facing Tabs

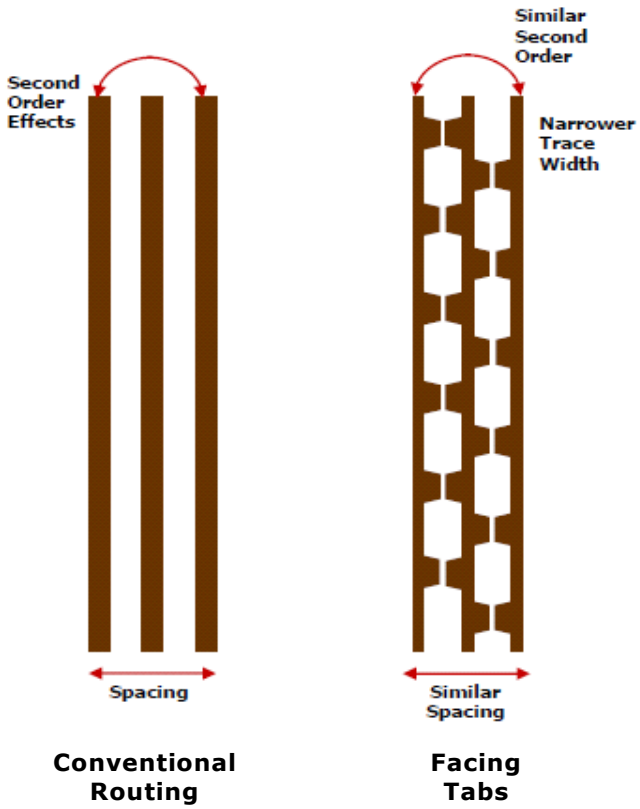
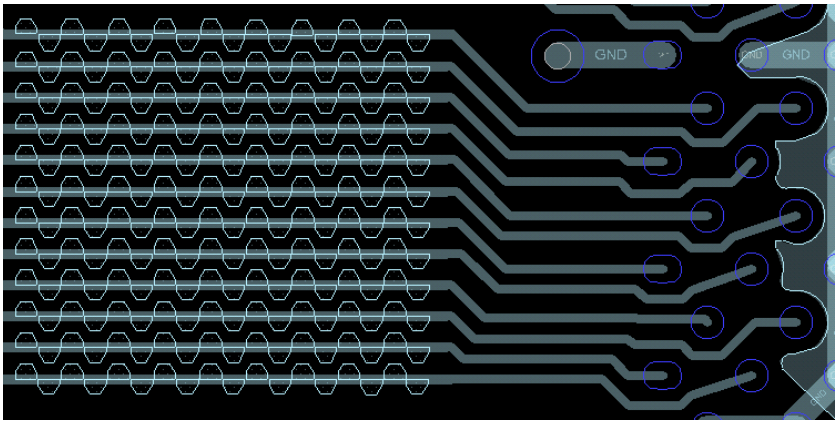
Criteria	Description
Guideline	Uses trapezoidal tabs that face the tabs in adjacent parallel traces. Allows for impedance control and FEXT (forward crosstalk) mitigation. • Two parallel traces. Impedance control is the primary function of the pin field tab although some noise mitigation takes place. • Used mostly on microstrip layers. 
Applicable Buses	DDR4
Purpose	To optimize signal integrity with improved trace impedance and first order forward crosstalk mitigation.
Significance	High. Violation of the Tabbed Routing rules will down grade memory performance.
Comments	It is recommended to achieve higher speed and higher performance on the DDR design.

Table 2-53. Tabbed Routing- Primary and Secondary Breakout

Criteria	Description
Guideline	In some cases a mix of conventional and tabbed routing will provide a solution. This is dependent on the design and the targeted performance. 
Applicable Buses	DDR4
Purpose	To improve signal integrity by controlling the trace impedance and noise mitigation.
Significance	High. Violation of the Tabbed Routing rules will down grade memory performance.
Comments	It is recommended to achieve higher speed and higher performance on the DDR design.

§ §

3 Platform Clocks

3.1 Routing Guidelines for Reference Clocks

Generic routing guidelines for system reference clocks are described in Chapter 2, "Platform Stack-up and General Design Considerations". The routing guidelines contained in this chapter assume the stackups shown in Chapter 2, "Platform Stack-up and General Design Considerations".

Note: For Dual Stripline routing, an angle of 30 degrees is required for signals routed on the inter layers. A particular trace width and spacing that is provided will meet the target impedance requirements when implemented on the reference stackup. Platform designers may have to adjust trace width and/or spacing to meet impedance and noise immunity requirements if a different stackup is used.

- Clock traces must be ground referenced to minimize dielectric and impedance variations.
- Clocks traces must not cross any plane splits on adjacent near reference planes.
- Spacing requirements for reference clock signals breaking out from the Driver buffer are reduced to minimum spacing required by Design For Manufacturing (DFM), for the first 200 mils of the clock traces.
- Do not split up the two halves of a differential clock pair between layers. Route field traces to all agents on the same physical routing layer referenced to ground.
- Typical routing assumes 1 layer transition within 500 mils (breakout) of the SoC output pins and a second layer transition within 500 mils of the destination ball (breakin).
- If a field trace layer transition cannot be avoided (this is not preferred), both clock traces of the differential clock pair must transition layers at the same length ± 100 mils.
- If an additional layer transition cannot be avoided (this is not preferred), use simulations to ensure the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces and avoid differential vias. Vias, placed in one signal of a differential-pair must be matched by a via in the complement. If unavoidable (this is not preferred), differential vias can be placed within length L1 between the clock driver and Rs to shorten length L1.

No length matching is required between different source pairs.

Stitching vias must be used when signal traces change layers from top layer to bottom or internal layer. In these cases reference GND layer associated with top signal layer has to be connected with GND-reference layer associated with bottom or internal signal layer using GND stitching via. Placing GND stitching via according current guidelines maintains optimal current return path and minimize crosstalk effect.

Stitching vias should be placed with this spacing:

- 30-mils (0.762-mm) pitch between differential clock via and closest stitching GND-via.
- Every differential clock via must have at least one GND stitching via with a maximum spacing of 30 mils (0.762 mm).

Placement of additional stitching vias, where possible, is recommended.

3.1.1 isCLK Layer Transition Rules

Layer transition on isClk sourced, output, reference clock topologies for anything other than breaking in and out of the components is not allowed. The maximum total number of vias is 2. If unavoidable (this is not preferred) an extra via transition can be added as long as total length of the topology is kept ≤ 12 inches.

Figure 3-1 details the allowable clock routing without layer transitions.

Figure 3-1. Reference Clock Routing Length Without Layer Transitions

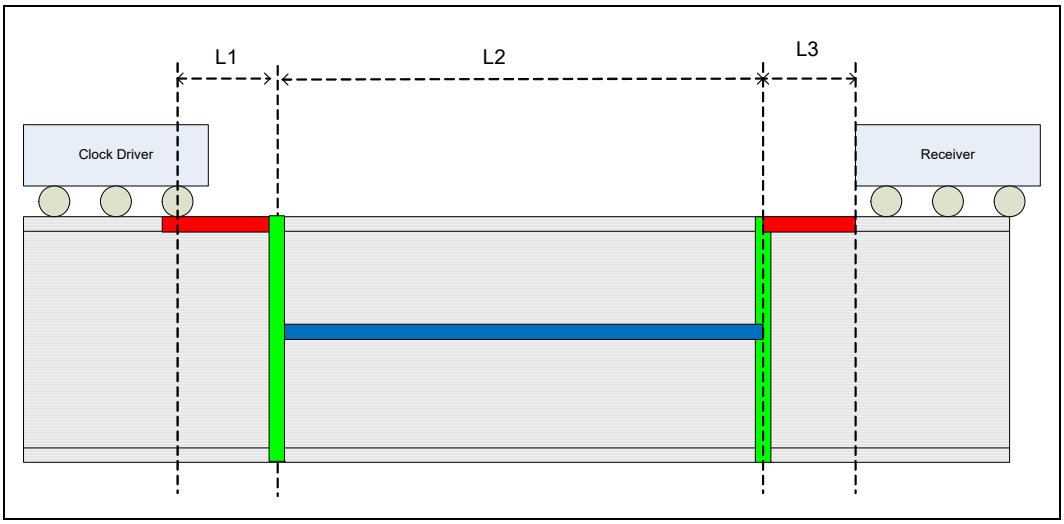
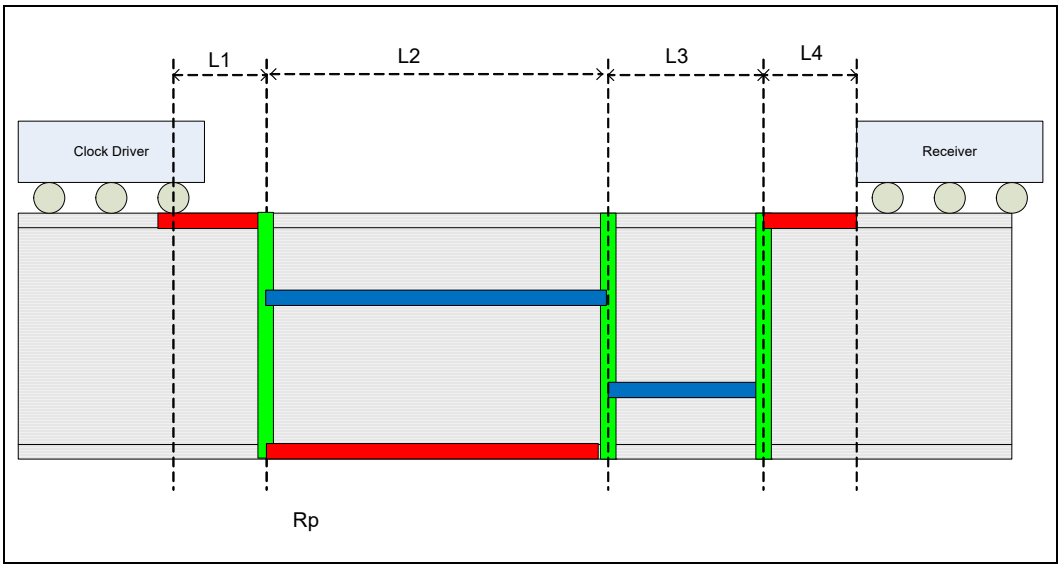


Figure 3-2 details the allowable clock routing with layer transitions.

One extra layer transition can be used in worst case scenarios, only if the reference clock topology length ≤ 12 inches i.e. L1+L2+L3+L4 ≤ 12 inches. L2 can be routed on either inner or outer layer. The total maximum number of via transitions in this case is ≤3.

Figure 3-2. Reference Clock Routing With layer Transitions Length ≤ 12 Inches

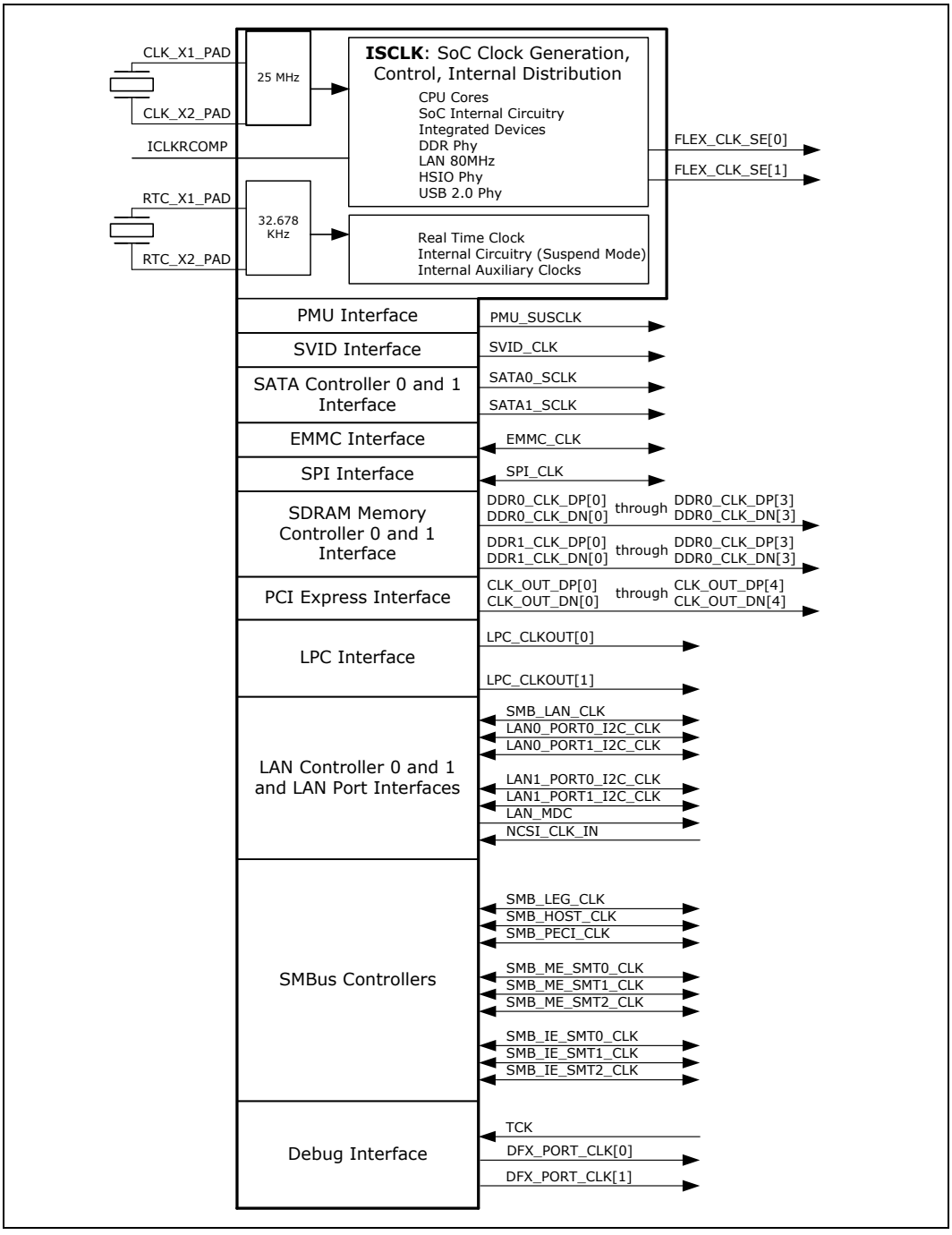


3.2 Platform Clock Topology Overview

SoC requires only two reference clocks input.

- 25 MHz clock input serves as the reference clock for the Internal System Clock (ISCLK).
- 32.768 kHz clock input serves as the reference clock for the internal Real Time Clock (RTC). All platform boards based on this SoC must have this clock input.

Figure 3-3. Platform Clock Topology Overview



The signal descriptions are shown in Table 3-1, "Signal Names and Descriptions". The Direction/Type column is interpreted as follows:

- I = Input signal. The SoC has receiver circuit.
- O = Output signal. The SoC has driver circuit.
- O-OD = Open-Drain Output. SoC output circuit uses an open-drain driver.
- Differential = Differential signal pair. Two pins: Positive; Negative.

Table 3-1. Signal Names and Descriptions (Sheet 1 of 2)

Signal Names	Direction	Shared	Notes
CLK_X1_PAD	I	No	**Clock Crystal - 25 MHz.** The SoC uses the crystal for its internal oscillators and PLLs to generate internal clocks of various speeds which are controlled and distributed throughout the SoC
CLK_X2_PAD	O	No	
ICLKRCOMP	I,O	No	**ISCLK RCOMP:** Compensation resistor for the CLK_OUT_DP[4:0], CLK_OUT_DN[4:0] differential output signals. The resistor is used by the internal ISCLK circuitry to calibrate the PCIe reference-clock driver impedance to comply with the PCIe specification for REFCLK. For 50-Ω driver impedance, ICLKRCOMP must be connected to a 200-Ω resistor to VSS on the platform board. For a 42.5- Ω driver impedance, a 169-Ω resistor must be used.
RTC_X1_PAD RTC_X2_PAD	I,O	No	**Clock Crystal - 32.768 KHz:** The SoC uses the crystal for its internal Real-Time Clock (RTC) oscillator. The clock is used internally and drives the PMU_SUSCLK output signal.
BVCCRTC_EXTPAD	I,O	No	**External Pad for RTC Power Well:** Must be connected to an external 0.1-µF capacitor on the platform board.
FLEX_CLK_SE[1:0]	O	Yes	**Flex Clock.** These single-ended output signals are general-purpose clocks that can be used by the platform board.
PMU_SUSCLK	O	Yes	
SVID_CLK	O-OD	Yes	
SATA0_SCLK SATA1_SCLK	O-OD	Yes	
EMMC_CLK	I,O	Yes	
DDR0_CLK_DP[3:0] DDR0_CLK_DN[3:0] DDR1_CLK_DP[3:0] DDR1_CLK_DN[3:0]	O, Differential	No	
CLK_OUT_DP[4:0] CLK_OUT_DN[4:0]	O, Differential	No	
LPC_CLKOUT[1:0]	O	Yes	

Table 3-1. Signal Names and Descriptions (Sheet 2 of 2)

Signal Names	Direction	Shared	Notes
SMB_LAN_CLK	I,O-OD	Yes	
LAN0_PORT0_I2C_CLK LAN0_PORT1_I2C_CLK LAN1_PORT0_I2C_CLK LAN1_PORT1_I2C_CLK	I,O-OD	Yes	
LAN_MDC	O	Yes	
NCSI_CLK_IN	I	Yes	
SPI_CLK	I,O	Yes	
SMB_LEG_CLK	I,O-OD	Yes	
SMB_HOST_CLK	I,O-OD	Yes	
SMB_PECI_CLK	I,O-OD	Yes	
SMB_ME_SMT0_CLK	I,O-OD	Yes	
SMB_ME_SMT1_CLK		Yes	
SMB_ME_SMT2_CLK		Yes	
SMB_IE_SMT0_CLK	I,O-OD	Yes	
SMB_IE_SMT1_CLK		Yes	
SMB_IE_SMT2_CLK		Yes	
TCK	I	No	
DFX_PORT_CLK[1:0]	O	Yes	

3.2.1 25 MHz Clock Input Design Consideration

These crystals are physically tuned to operate within the specified frequency range and ppm tolerance with a certain expected capacitive load present. The expected external capacitive load to be used (Ce) must compensate for the crystal capacitive load and the pin and trace capacitances. The external load capacitors are important to minimize frequency variations from the crystal by compensating for variable PCB factors related to pin and trace capacitance. Care must be exercised in the selection of the external load capacitors to present the expected capacitive load specified for the crystal in use on the platform. A balanced capacitance on both legs of the circuit is ideal.

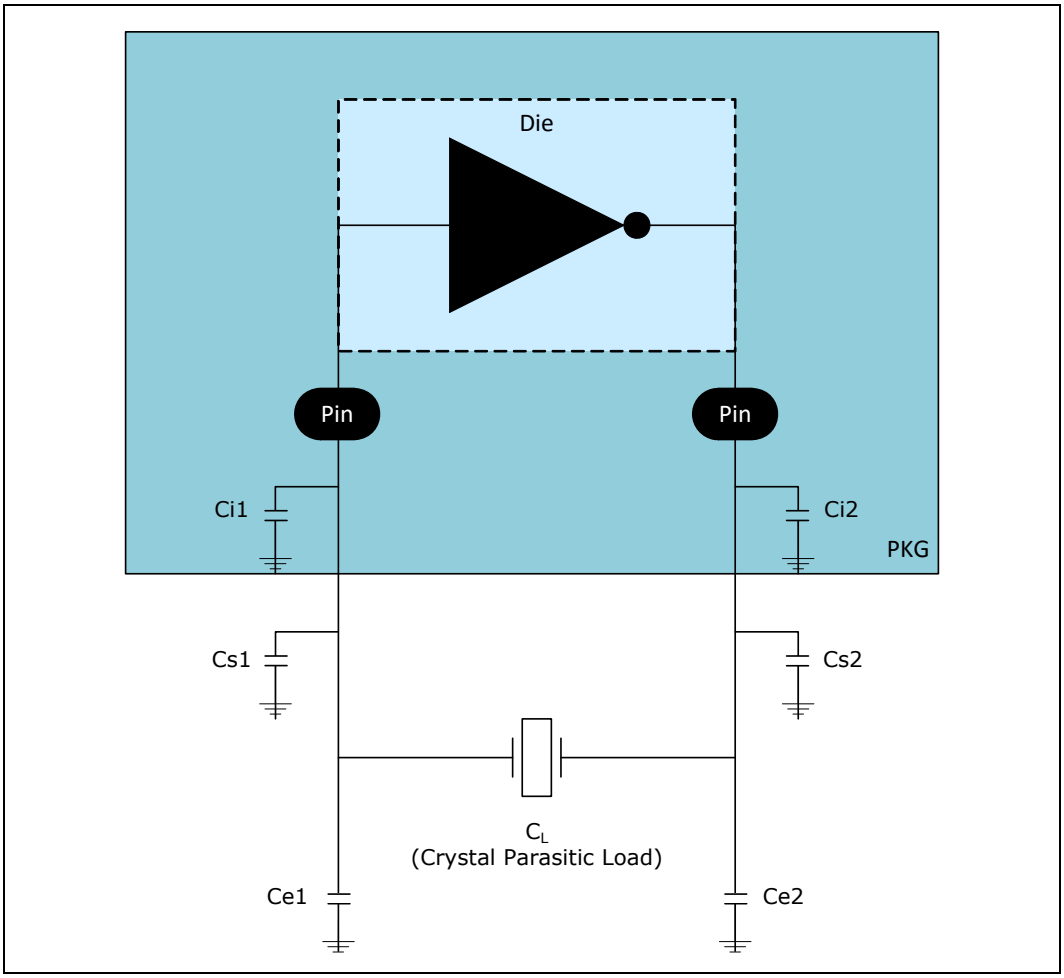
The appropriate capacitor value for the platform may be determined using the following formula:

Ce = (2CL) - (Cs + Ci), where:

- Ce = Ce1 = Ce2
- CL = crystal capacitance as specified in the datasheet
- Cs = Cs1 + Cs2, where Cs1 = Cs2 (stray capacitance of board traces and XTAL pad)
- Ci = Ci1 + Ci2, where Ci1 = Ci2 (~2 pF internal capacitance of pin and PKG traces)

Figure 3-4 shows a diagram of the crystal capacitance calculation parameters.

Figure 3-4. Example Diagram for Crystal Capacitance Calculation



Based on Ci1 = Ci2 is about 2 pF, the Ce typical value is falling in the range 27 pF ~ 36 pF.

The following table provides more details on the 25 MHz crystal specification.

Table 3-2. 25 MHz Crystal Specification

Parameter	Value	Units	Comment
Frequency	25	MHz	
Mode of vibration	1st		AT cut crystal
Motional resistance	30	Ω	Max
Load capacitance	20	pF	
Calibration Tolerance	± 20	ppm	at 25 °C
Frequency Stability	± 20	ppm	Reference Temperature 25 °C
Operating Temperature Range	-20 to 100	°C	
Operating Drive Level	300	µW	
Aging	20	ppm / 10 years	at 25 °C
Shunt Capacitance	7	pF	max
Trim Sensitivity (pullability)	10	ppm/pF	Max (can be relaxed to 12ppm/pF if aging is 10ppm/10 years)
Quality Factor	30,000		min
3rd Harmonic Motional Resistance	30	Ω	min
Physical Dimensions	3.2mm x 2.5mm x 0.7mm	x, y, z	min

The design implemented on Customer Reference Board (CRB):

- One 25 MHz crystal

Two external load capacitors C1 and C2 (typical value = 33 pF, if guidelines are followed from the Crystal Capacitance Calculation section)

When calculating load capacitance:

- The value of the capacitor should be 40pF-(trace capacitance)-(pin capacitance). Trace capacitance is about 3pF and pin capacitance is about 2-3pF.
- The exact capacitor value should be decided after measuring the crystal frequency on an actual board with a few different capacitors. The value should be selected such that the frequency is within 20 PPM to 25 MHz (as close as possible using standard capacitors).
- After capacitor value section, the crystal frequency need be tested on multiple boards to make sure the accuracy.
- Capacitor tolerance value should be ± 5% or better. Use NPO or C0G high quality capacitors.

A summary of the 25 MHz crystal routing considerations is as follows:

- Clock crystals should be placed and crystal signals laid out first, before other signals on the motherboard.
- X1 and X2 board routing length shall be < 1000 mils. X1 and X2 lengths should be matched within ± 50 mils, or capacitance should be matched within 0.5 pF.
- Route such that X2 (X_{OUT}) is next to the aggressors, instead of the more sensitive X1 (X_{IN}).
- Spacing between X1 and X2 to be kept at 7h minimum with a ground shield between the two. This distance can be reduced to 4h in the pinfield region up to 200 mils.
- Keep the breakout/pinfield routing as short as possible to avoid crosstalk (this should be kept lower than 300 mils).
- Spacing between X1/X2 to nearest aggressor signal traces should be kept at 13h with ground shields. Ground pour is required with enough return vias (one at the beginning and end of the pour and one every 0.25 inches).
- There should be a 5 mil airgap between ground pour and signal.
- Spacing between X1/X2 to nearest aggressor signal via should be 7h and must have a ground pour.
- Spacing to power rails and power vias should be very tightly controlled with a 70 mil spacing requirement.
- Solid reference ground required under the crystal, and no routing is recommended on signal layer below the crystal.
- Crystal traces are not differential.
- No more than one via per X1/X2 trace. If xtal is to be routed on the bottom layer, place xtal and caps on the bottom layer of the board. Any via transitions on X1/X2 need to have a ground return via with an airgap of 7.5 mils.
- Add ground BGA vias in the pinfield to isolate crystal pins from aggressors and other crystal pins.
- Add two GND vias in BGA field b/w X1/X2 and DQ4/5 to provide a vertical path for return current transition b/w package, board L1 and board L2.

3.2.2 RTC Design Consideration

The following table provides the 32.768 kHz crystal specification.

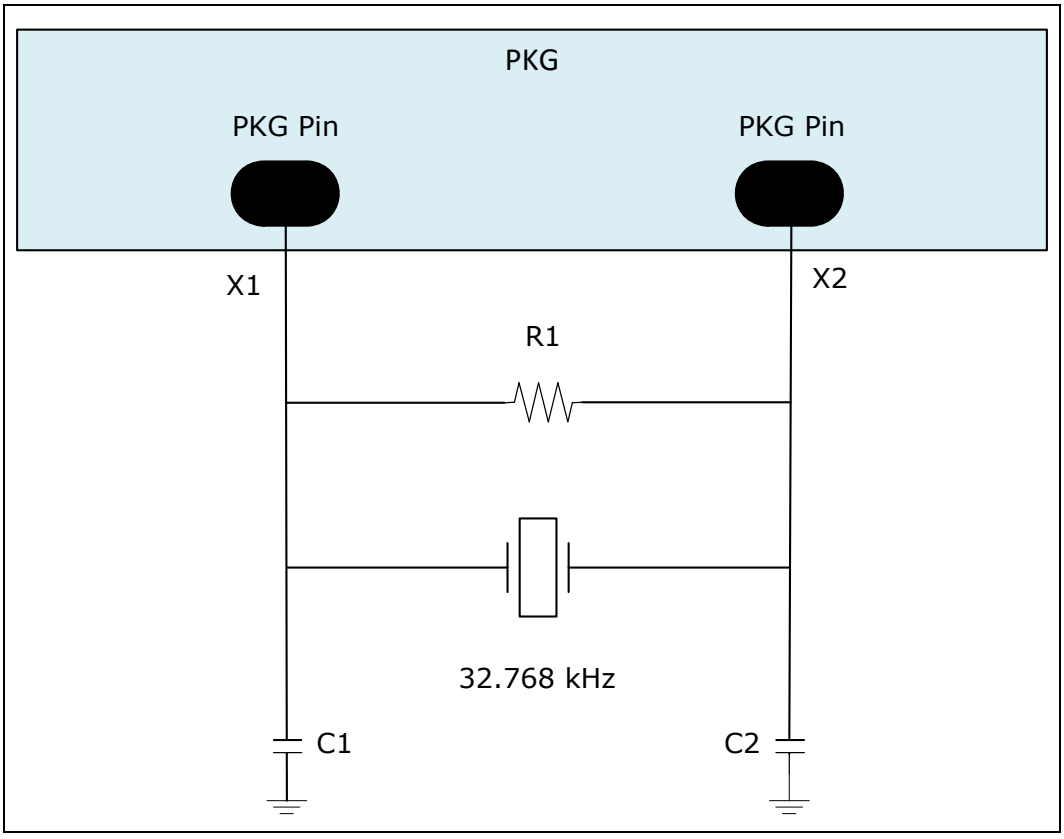
Table 3-3. 32.768 kHz Crystal Specification

Item	Specifications
Nominal Freq	32.768 kHz
Storage Temp	-55 °C to 125 °C
Operating Temp	-40 °C to 85 °C
Drive Level	0.5 uW
Freq Tolerance	± 20 ppm
Turnover Temp	+25 °C ± 5 °C
Parabolic Coefficient	- 0.04 ppm/°C^2
Load Capacitance	12.5 pF
ESR	50 kΩ (Max)
Motional Capacitance	3.4 fF (Typ)
Shunt Capacitance	1.1 pF (Typ)
Freq Aging	±3 ppm/Year (Max)
Cut	Tuning Fork
Mode of Oscillation	Fundamental

The implemented design on the Customer Reference Board (CRB) has:

- One 32.768 kHz crystal
- Two external load capacitors C1 and C2 (typical value = 18 pF, if guidelines are followed from the Section 3.2.1, "25 MHz Clock Input Design Consideration.")
- One 10 MΩ bias resistor R1

Figure 3-5. RTC Crystal Implementation Diagram



Notes:

1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.
2. Reference designators are arbitrarily assigned.
3. RTCX1(X1) is the input to the internal oscillator. RTCX1 can be driven by external clock generator to desired frequency.
4. RTCX2(X2) is the feedback for the external crystal. When single ended external clock generator is used, this pin must be left floating.

When calculating load capacitance:

- The value of the capacitor should be 25 pF-(trace capacitance)-(pin capacitance). Trace capacitance is about 4 pF and pin capacitance is about 2-3 pF.
- The exact capacitor value should be decided after measuring the crystal frequency on an actual board with a few different capacitors. The value should be selected such that the frequency is as close as possible to 32.768 kHz.

After capacitor value section, the crystal frequency needs to be tested on multiple boards to ensure accuracy.

- Capacitor value should be ± 5% or better. This implies using NPO or C0G high quality capacitors.

Because RTC is used as system clock and is required to be highly accurate, trace layout and routing must be precise.

- Reduce trace capacitance by minimizing the RTC trace length. The recommendation is a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR4, a 5-mil trace has approximately 3.3 pF per inch.
- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2.
- Using a ground guard plane is highly recommended.

Add filter on clock generator power supply.

Table 3-4. RTC Routing Guidelines

Signal Name	Impedance	Width (W)	Spacing (S)	Layer	Length	Figure	Note
RTCX1 RTCX2	50 Ω ± 15%	4 mils	15 mils	Microstrip	0-1"	External Circuitry for the RTC	1
	50 Ω ± 10%	4.5 mils	15 mils	Stripline			
Note: 1. W represents width of signal; S represents spacing to any other signal.							

3.3 PCIe Interface Clock Output Design Guide

There are 5 PCIe clock output differential signals to support on board PCIe device/ connector. There is ***no board/package termination required for differential reference clocks.***

Note: For DDR clock design guide detail, see Chapter 4, "DDR4 Memory."

Figure 3-6 and Table 3-5 show the topology and routing guidelines for a PCIe* reference clock from the SoC on the baseboard to a PCIe* slot.

Figure 3-6. PCIe Clock from SoC to PCIe Device on Add-In Card

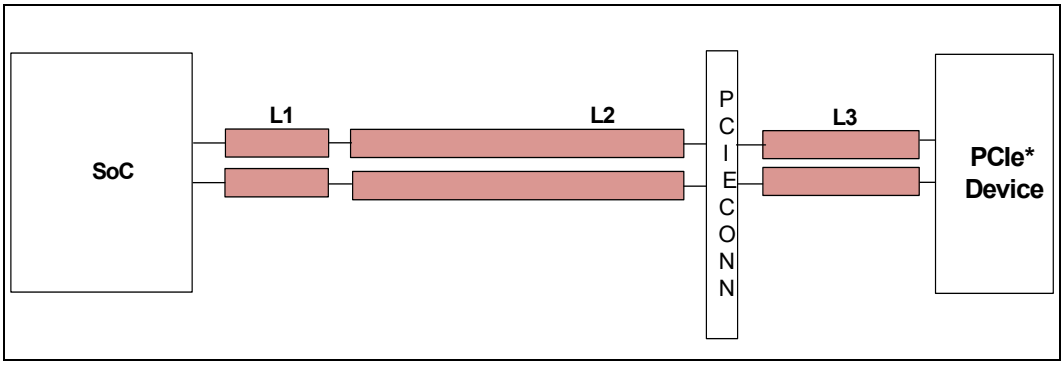


Table 3-5. PCIe Clock Topology from SoC to PCIe Device on Add-In Card

Signal Group	PCIe Reference Clocks at 100 MHz
Topology	Point-to-point differential
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	85 Ω differential. See table note.
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge to Edge Spacing (within a signal pair)	Based on reference stackup with certain assumptions
Minimum Spacing (pair-to-pair and other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Length L1	Max = 1 inch (Refer to SoC Baseboard reference stackup for breakout trace spacing/trace width recommendations)
Length L2	2 to 16 inches
Length L3	1 to 4 inches (as per PCIe* routing guidelines)
Total Length L1+L2+L3 (Baseboard + Add-in Card)	Max = 20 inches
Signal pair length matching from Driver pin to Receiver pin	± 10 mils
Pair-Pair Length (PCIe Gen3 at slot)	See Section 3.1, "Routing Guidelines for Reference Clocks"
Via Count	Max 3 vias per signal until Add In Card Connector Max 2 vias per signal on Add In Card
Layer Switching	Not Allowed

Notes:

1. PCIe3 Reference Clocks Pair-to-pair length matching applies only to adjacent agents directly connected to each other and share the same clock source. The adjacent agents are devices that directly transfer the data from one side to other side. The length is measured from Clock Buffer all the way to the PCIe Device PKG PIN. There is no pair-to-pair length matching requirement for any two agents which are not directly connected.
2. No Layer change is preferred, and stripline routing is recommended for better impedance control. Use 2 connector topology only if 1 connector topology is not possible.
3. Note that there is a higher risk involved in violating the reference clock phase jitter on a 2-connector PCI Express* Reference clock topologies.
4. Note that PCIe specifications call for trace impedance of 100 Ω on the PCIe non-riser Add In cards. However, Intel has done the necessary signal integrity analysis to show that the PCIe non-riser Add In cards will work properly on the 85 Ω Intel® Atom™ Processor C3000 Product Family.

Figure 3-7 and Table 3-6 show the topology and routing guidelines for a PCIe reference clock from the SoC on the baseboard to a PCIe slot on a riser card.

Figure 3-7. PCIe Reference Clock from SoC to PCIe Device on Add-In Card via Riser Card

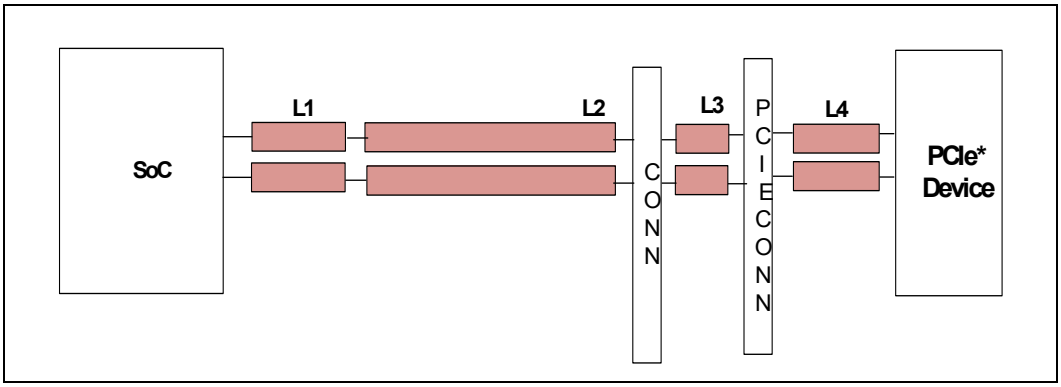


Table 3-6. PCIe Reference Clock from SoC to PCIe Device on Add-In Card via Riser Card

Parameter	PCIe Reference Clocks at 100 MHz
Topology	Point-to-point differential
Reference Plane	Ground referenced
Characteristic Trace Impedance (Z_0)	85 Ω differential
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge to Edge Spacing (within a signal pair)	Based on reference stackup with certain assumptions
Minimum Spacing (pair-to-pair and other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Breakout Length L1	Max = 1 inches (Refer to SoC Baseboard reference stackup for breakout trace spacing/trace width recommendations)
Length L2	2 to 15 inches
Length L3	2 to 15 inches
Length L4	1 to 4 inches (as per PCIe routing guidelines)
Total Length L1+L2+L3+L4 (Baseboard + Riser Card + Add-in Card)	Max = 20 inches
Signal pair length matching from Driver pin to Receiver pin	± 10 mils
Pair-Pair Length (PCIe Gen3 at slot)	See Section 3.1, "Routing Guidelines for Reference Clocks"
Layer Switching	Not Allowed
Via Count	Max 3 vias per signal until Add In Card Connector Max 2 vias per signal on Add In Card

Notes:
1. PCIe3 Reference Clocks Pair-to-pair length matching applies only to adjacent agents directly connected to each other and share the same clock source. The adjacent agents are devices that directly transfer the data from one side to other side. The length is measured from Clock Buffer all the way to the PCIe Device PKG PIN. There is no pair-to-pair length matching requirement for any two agents which are not directly connected
2. No Layer change is preferred, and stripline routing is recommended for better impedance control. Use 2 connector topology only if 1 connector topology is not possible.
3. Note that there is a higher risk involved in violating the reference clock phase jitter on a 2-connector PCI Express* Reference clock topologies.
4. Note that PCIe specifications call for trace impedance of 100 Ω on the PCIe non-riser Add In cards. However, Intel has done the necessary signal integrity analysis to show that the PCIe non-riser Add In cards will work properly on the 85 Ω Intel® Atom™ Processor C3000 Product Family.

Figure 3-8 and Table 3-7 show the topology and routing guidelines for the PCIe reference clocks from the SoC on the baseboard to a PCIe down device on the baseboard.

Figure 3-8. PCIe Reference Clock from SoC to PCIe Down Device

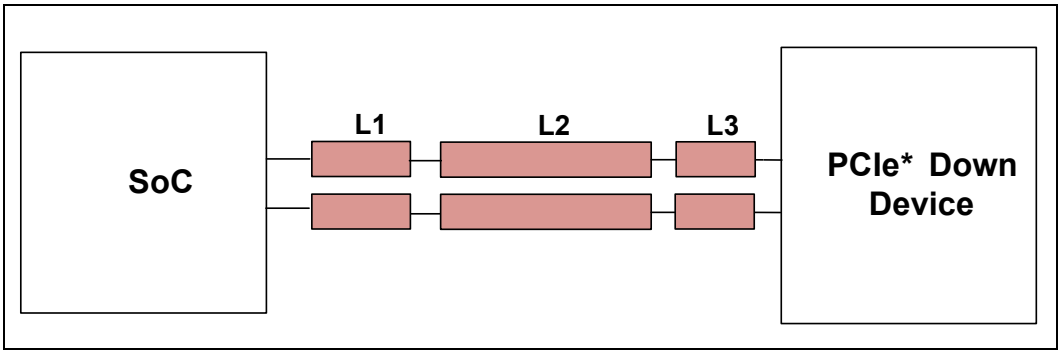


Table 3-7. PCIe Reference Clock from SoC to PCIe Down Device

Signal Group	PCIe Reference Clocks at 100 MHz
Topology	Point-to-point differential
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	85 Ω differential
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge to Edge Spacing (within a signal pair)	Based on Baseboard reference stackup
Minimum Spacing (pair-to-pair and to other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Breakout Length L1	Max = 1.5 inches
L2 Length	Max = 17 inches
Breakout Length L3	Max = 1.5 inches
Breakout Max Length L1+ L3	Max = 3 inches
Total Length L1+L2+L3	Max = 20 inches
Signal pair length matching from Driver pin to Receiver pin	± 10 mils
Pair-Pair Length	See Section 3.1, "Routing Guidelines for Reference Clocks"
Via Count	Max 2 vias per signal
Layer Switching	Not Allowed

A clock buffer can be used when the design requires to support more PCIe devices or PCIe connectors. A DB8xxZL or a DB12xxZL, for example, could be used to provide more 100 MHz differential clocks. The clock buffer will require one of the CLK_OUT_DP/DN [4:0] outputs as a reference.

Figure 3-9. Clock Buffer Reference Clock Topology - SoC to DBxxxxZL

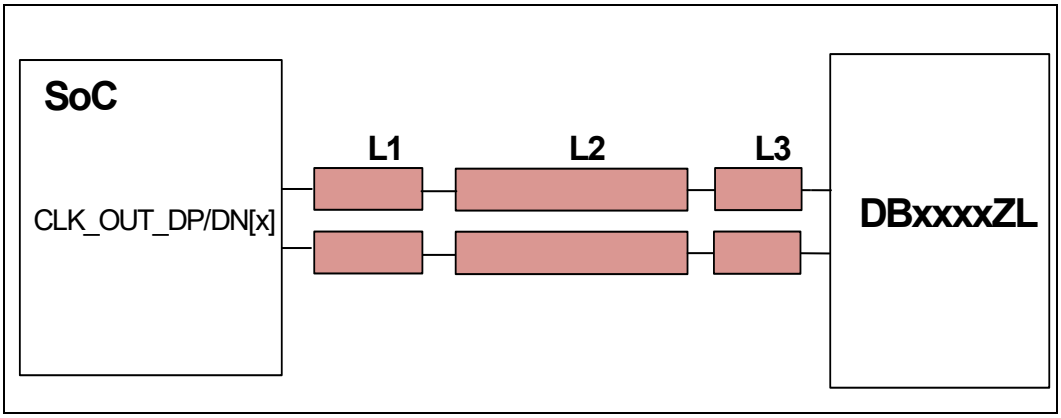


Table 3-8. Clock Buffer Reference Clock Topology - SoC to DBxxxxZL

Signal Group	SoC Reference Clocks at 100 MHz
Topology	Point-to-point differential
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	85 Ω differential
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge to Edge Spacing (within a signal pair)	Based on Baseboard reference stackup
Minimum Spacing (pair-to-pair and to other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Breakout Length L1	Max = 1.5 inches
L2 Length	Max = 17 inches
Breakout Length L3	Max = 1.5 inches
Breakout Max Length L1+ L3	Max = 3 inches
Total Length L1+L2+L3	Max = 20 inches
Signal pair length matching from Driver pin to Receiver pin	± 10 mils
Pair-Pair Length	See Section 3.1, "Routing Guidelines for Reference Clocks"
Via Count	Max 2 vias per signal
Layer Switching	Not Allowed

Figure 3-10. DBxxxxZL Reference Clock Topology - DBxxxxZL to PCIe Down Device

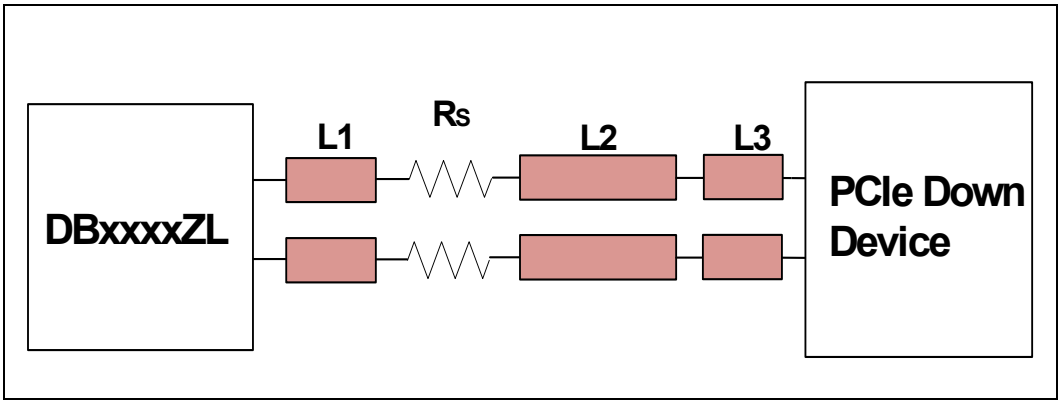


Table 3-9. DBxxxxZL Reference Clock Topology - DBxxxxZL to PCIe Connector or PCIe Down Device

Signal Group	Buffer Reference Clocks at 100 MHz
Topology	Point-to-point differential
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	85 Ω differential
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge to Edge Spacing (within a signal pair)	Based on reference stackup
Minimum Spacing (pair-to-pair and to other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Breakout Length L1	Max = 0.5 inches
Series Resistor (Rs)	27.4 Ω ± 1%
L2 Length	Max = 18 inches
Breakout Length L3	Max = 1.5 inches
Breakout Max Length L1+ L3	Max = 2 inches
Total Length L1+L2+L3	Max = 20 inches
Signal pair length matching from Driver pin to Receiver pin	± 10 mils
Pair-Pair Length	See Section 3.1, "Routing Guidelines for Reference Clocks"
Via Count	Max 2 vias per signal
Layer Switching	Not Allowed

Figure 3-11. DBxxxxZL Reference Clock Topology - DBxxxxZL to PCIe Connector

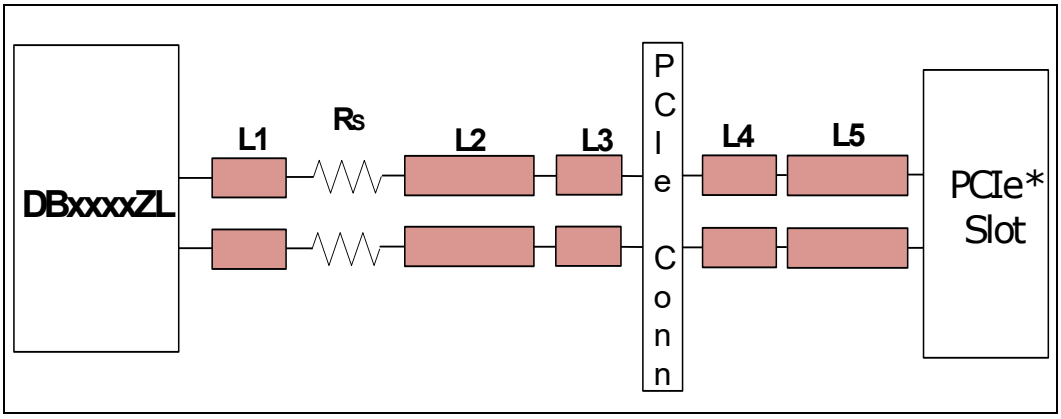


Table 3-10. DBxxxxZL Reference Clock Topology - DBxxxxZL to PCIe Connector

Signal Group	PCIe* Reference Clocks at 100 MHz
Topology	Point-to-Point Differential with Series Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_o)	85 Ω Differential.
Characteristic Trace Impedance Tolerance	Microstrip: ± 17.5% Stripline: ± 12%
Nominal Trace Width and Edge-to-Edge Spacing (within a signal pair)	Based on Reference Stack-up with Certain Assumptions
Minimum Spacing (pair-to-pair and other signals)	Microstrip: 7X height above reference plane Stripline: 3X height above reference plane
Serpentine Spacing	Microstrip: 9X height above reference plane Stripline: 5X height above reference plane
Length from Clock Driver to Rs (L1)	Maximum = 0.5 inches
Length L2	2 to 16 inches
Length L3	20 inches - L1-L2
Length L4	0.5 to 4 inches
Breakout Length L5	0.2 to 1 inches (See the CPU Baseboard Reference Stack-up for the breakout trace spacing/trace width recommendations.)
Package Length	0.2 - 1 inch
Receiver Capacitance Modeled	0.2 - 2 pF
Total Topology Length (Baseboard + Add-in Card)	Maximum = 20 inches
Signal Pair Length Matching from Driver Pin to Receiver Pin	± 10 mils
Series Resistance (Rs)	27.4 Ω ± 1%

3.4 Flex Clock Output Design Guide

In this chapter two single-ended reference clock signals are described: FLEX_CLK_SE[1:0] are two, single-ended output signals available from SoC as general purpose clocks used by components on platform.

The supported frequencies for each Flex clock are:

a. 25 MHz Reference Clock
b. 33 MHz Reference Clock
c. 48 MHz Reference Clock
d. 50 MHz Reference Clock

The designer can use soft strap (see EDS chapter 4 “Strapping and Configuration”) to enable and disable one of the supported frequencies for each Flex clock.

All single ended reference clock signals are routed at 50 Ω impedance. In addition, most single ended clocks can support double-load. Before using any of the configurations, please check the termination values for each topology correctly. Below are reference routing topologies for these signals.

The SoC has four outputs for Flex reference clocks that are single-ended clocks that can be programmed up to 50 MHz. The following topologies are Flex single-ended reference clock examples.

Figure 3-12 and Table 3-11 show the topology and routing guidelines for the Flex 48 MHz reference clock from the SoC to the receiver.

Figure 3-12. Flex Single-Ended Reference Clocks

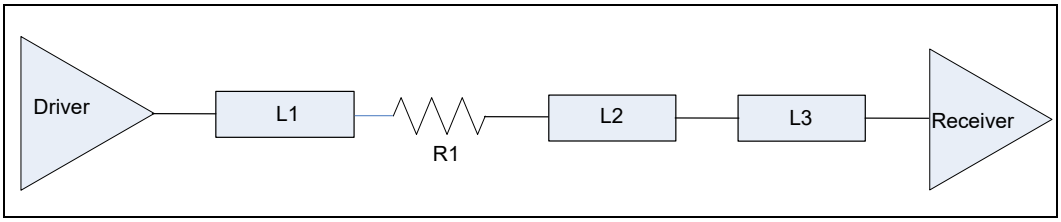


Table 3-11. Flex Single-Ended Reference Clocks

Parameter	Routing Guideline	Figure
Clock Group	25/33/50 MHz	Figure 3-12
Topology	Point-to-Point	Figure 3-12
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	50 Ω ± 15%	
Trace Width	Refer to reference stackup	
Trace Spacing	Refer to baseboard stackup	
Trace Length – L1	0 to 1 inches	Figure 3-12
Trace Length – L2	(2 to 16 inches) - L3	Figure 3-12
Breakout Routing Length L3 at the Receiver	Max = 1.5 inches (Refer to CPU Baseboard reference stackup for breakout trace spacing/trace width recommendations)	Figure 3-12
Total Length L1+L2+L3	Max = 17 inches	Figure 3-12
Series Resistor if driving single load	R1 = 22 Ω ± 5%	Figure 3-12
Maximum via Count	4	

Figure 3-13 and Table 3-12 show the topology and routing guidelines for sharing the FLEX 25 MHz/33 MHz/48 MHz/50 MHz reference clock between two down devices.

Figure 3-13. Flex Single-Ended Reference Clocks Double-Load

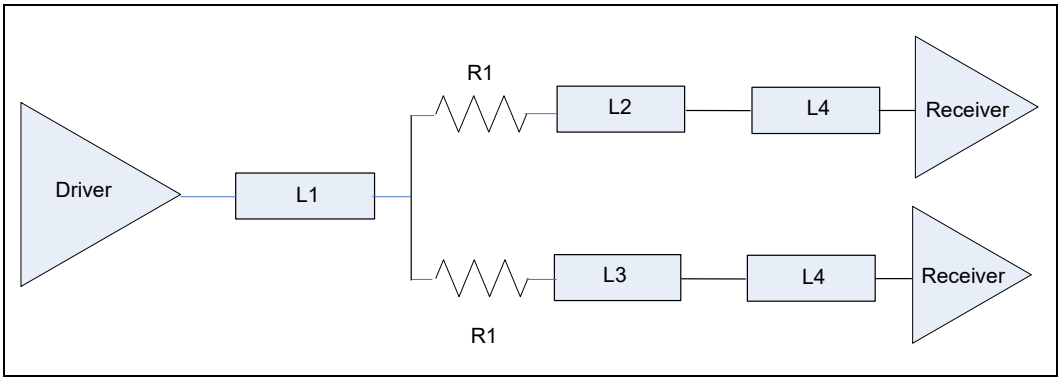


Table 3-12. Flex Single-Ended Reference Clocks Double-Load

Parameter	Routing Guideline	Figure
Clock Group	25 MHz/33 MHz/48 MHz/50 MHz	Figure 3-13
Topology	"T" topology	Figure 3-13
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	50 Ω ± 15%	
Trace Width	Refer to reference stackup	
Trace Spacing	Refer to baseboard stackup	
Trace Length – L1	0 to 1 inches	Figure 3-13
Trace Length – L2, L3	(2 to 12 inches) - L4	Figure 3-13
Breakout Routing Length L4 at the Receiver	Max = 1.5 inches (Refer to CPU Baseboard reference stackup for breakout trace spacing/trace width recommendations)	Figure 3-13
Total length (L1+L2+L4) or (L1+L3+L4)	Max = 13 inches	Figure 3-13
Series Resistor	R1 = 22 Ω ± 5%	Figure 3-13
Maximum via Count	4	

Figure 3-14. Crystal Layout Guidance

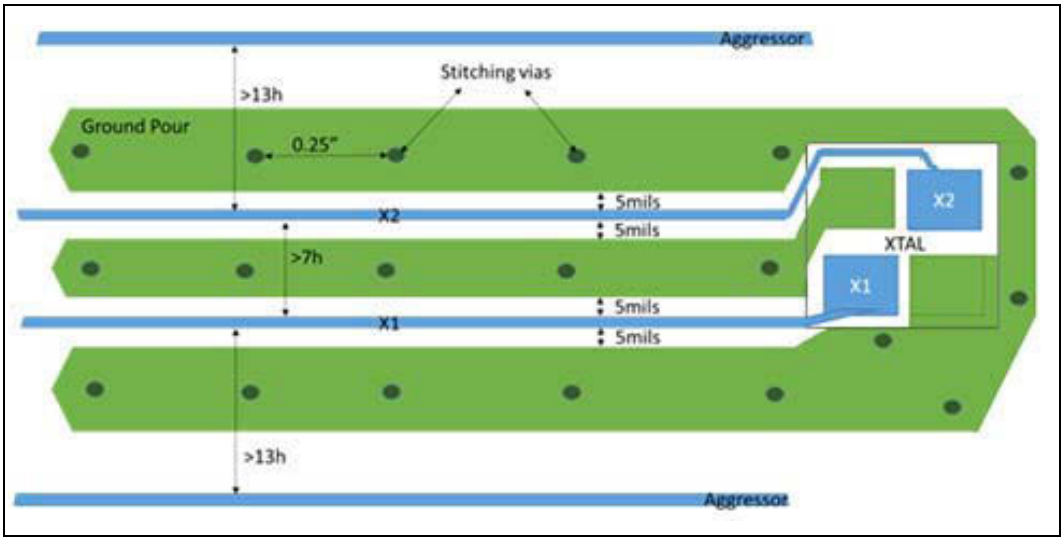
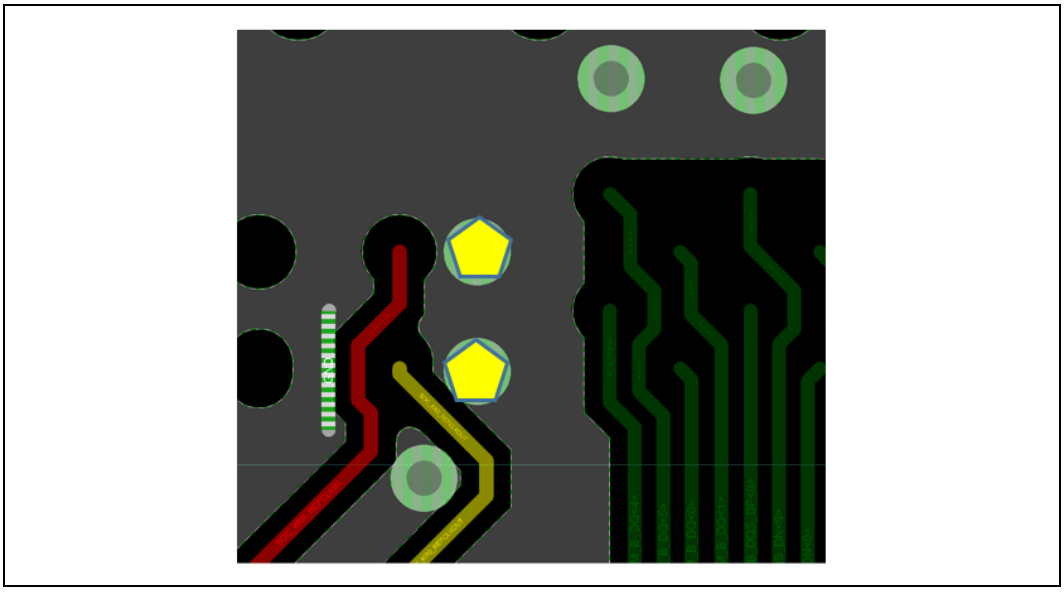


Figure 3-15. Add Two GND Vias For CLK_X1 and CLK_X2 Signals



Due to 25 MHz clock input is also supported integrated Ethernet Controller operation, the clock input is required to be 25MHz ±100ppm.

The following are crystals examples supported as reference:

- TXC: 7M25020008
- Pericom: FL2500213Z
- NDK: NX5032GA 25M EXS00A-CG03780

Based on Ci1 = Ci2 is about 2 pF, the Ce typical value is falling in the range 27 pF ~ 36 pF.

It is recommended to place GND stitching vias no more than 100 mils from the BGA pins, the spacing from the trace to the via should be minimum 5 mils, and the maximum distance to allocate the VSS vias should be 200 mils.

3.5 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Use spread spectrum clocking where possible.

Route clocks on the layer adjacent to the ground reference plane.

§ §

4 DDR4 Memory

This chapter contains information on supported modules, connectivity, module population rules, topologies, and routing guidelines for the DDR4 system memory interface.

The processor has a two-channel memory interface operating in the Independent Channel Mode, with each channel supporting memory down or up to two dual in-line memory module (DIMM) sockets. Each channel consists of 64 data and 8 ECC bits, address, control, and management signals.

Memory channel supports up to 2400MHz DDR4 speed. For dual DIMM channels with two DIMM populated, T-topology is used to support up to 2400MHz. T-topology when compared to daisy chain has the advantage of supporting maximum loading at maximum speed since reflections are eliminated by making the loads look symmetric.

Note: For this SoC at least one memory channel must be populated either channel 0 or channel 1. For the unused channel, Non-connect all the signals of this channel.

The SoC supports "Independent Channel Mode". Either channel may be populated or both. There are no DIMM matching requirements between channels. Each channel may run at different DIMM timings (RAS latency, CAS latency, and so forth).

Sockets are populated with all RDIMMs, all UDIMMs, or all SODIMMs. All DIMMs must be DDR4 DIMMs.

DIMMs with different timing parameters can be installed on different slots within the same channel, but only timings that support the slowest DIMM will be applied, i.e., the faster DIMM in a channel will run at the lower speed.

The DIMM stuffing order prioritizes the tallest connector in the channel. For the SODIMM 1DPC configuration (both regular and same-side) populating the tallest connector is preferred.

Mixing of single rank (SR) and dual rank (DR) DIMMs is allowed but there may be a speed bin loss.

In the case where mixed SODIMM connectors are used (5.2 mm and 4 mm connectors) but only one connector will be populated, load the SODIMM into the 5.2 mm connector.

For a given channel, if both connectors possess the same mechanical characteristic, the T-topology does not care which connector is populated first. This applies to (for example),

- RDIMM/UDIMM connectors.
- Homogeneous SODIMM, i.e., same height 4mm/4mm or 5.2mm/5.2mm.

It does not apply in a non-homogeneous SODIMM configuration. The tallest connector should be populated first. For example,

- 5.2mm/4mm - 5.2mm should be populated first.

4.1 DDR4 Signal Groups

The system memory interface can be divided into four signal groups:

- Source-Synchronous
- Source Clocked
- Clocks
- Miscellaneous

Table 4-1 below summarizes the different signal groupings. Refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* for more details on these signals.

Table 4-1. DDR4 Processor Signal Groups (Sheet 1 of 2)

JESD79-3E Standard Name	Controller Signal Name Channel 0	Controller Signal Name Channel 1
Source-Synchronous Signals		
DQ	DDR0_DQ[63:0]	DDR1_DQ[63:0]
CB	DDR0_ECC[7:0]	DDR1_ECC[7:0]
DQS, DQS#, R/U DIMM DQS, DQS# SODIMM	DDR0_DQS_D{NP}[17:0] DDR0_DQS_D{NP}[8:0]	DDR1_DQS_D{NP}[17:0] DDR1_DQS_D{NP}[8:0]
Source Clocked Signals		
A	DDR0_MA[13:0] DDR0_MA14_WE_N DDR0_MA15_CAS_N DDR0_MA16_RAS_N DDR0_PAR DDR0_MA17	DDR1_MA[13:0] DDR1_MA14_WE_N DDR1_MA15_CAS_N DDR1_MA16_RAS_N DDR1_PAR DDR1_MA17
BA	DDR0_BA[1:0]	DDR1_BA[1:0]
ACT#	DDR0_ACT_N_MA[15]	DDR1_ACT_N_MA[15]
BG#	DDR0_BG0_BA[2] DDR0_BG1_MA[14]	DDR1_BG0_BA[2] DDR1_BG1_MA[14]
CKE	DDR0_CKE[3:0]	DDR1_CKE[3:0]
S[1:0]# (R/U DIMM) CS0_n,CS1_n (SODIMM)	DDR0_CS_N[1:0],DDR0_CS_N[3:2]	DDR1_CS_N[1:0],DDR1_CS_N[3:2]
S[3:2]#, C2 (R/U DIMM) C0_CS2_n, C1_CS3_n (SODIMM)	None Available	None Available
ODT	DDR0_ODT[3:0]	DDR1_ODT[3:0]
Clocks		
CK, CK#	DDR0_CLK_D{NP}[3:0]	DDR1_CLK_D{NP}[3:0]
Miscellaneous - Asynchronous Reset		
RESET#	DDR01_DRAMRST_N	
ALERT#	DDR0_ALERT_N_PAR_ERR_N	DDR1_ALERT_N_PAR_ERR_N
Miscellaneous		
	DDR_SCL (See Chapter 11, "System Management Bus Interfaces")	
	DDR_SDA (See Chapter 11, "System Management Bus Interfaces")	

Table 4-1. DDR4 Processor Signal Groups (Sheet 2 of 2)

JESD79-3E Standard Name	Controller Signal Name Channel 0	Controller Signal Name Channel 1
	DDR01_COMP	
	ADR_TRIGGER	
	ADR_COMPLETE	

Note: DDR0_ALERT_N_PAR_ERR_N and DDR1_ALERT_N_PAR_ERR_N signal layout guidelines are described in below in Section 4.7.5.4, "DDR4 Alert signals: DDR0_ALERT_N_PAR_ERR_N and DDR1_ALERT_N_PAR_ERR_N".

DDR0_C0 and DDR0_C1 are the chip ID signals. These are not supported by the SoC. Leave as no connect (NC).

The Asynchronous DRAM Refresh signals, ADR_TRIGGER and ADR_COMPLETE, layout guidelines are described in Chapter 13, "I/O Interfaces."

4.1.1 DDR4 Data Strobe (DQS) to Data (DQ/ECC) Affinity

Table 4-2 below shows the data signal strobe to data signal affinity for x8, x16, and x4 DRAM device connections.

Table 4-2. DDR4 DQ/ECC to DQS Grouping

Data Group	Associated Strobe		
64 Bit Data Bus	x8 and x16	x4	
DQ[07:00]	DQS_{DP/DN}00	DQS_{DP/DN}00	DQS_{DP/DN}09
DQ[15:08]	DQS_{DP/DN}01	DQS_{DP/DN}01	DQS_{DP/DN}10
DQ[23:16]	DQS_{DP/DN}02	DQS_{DP/DN}02	DQS_{DP/DN}11
DQ[31:24]	DQS_{DP/DN}03	DQS_{DP/DN}03	DQS_{DP/DN}12
DQ[39:32]	DQS_{DP/DN}04	DQS_{DP/DN}04	DQS_{DP/DN}13
DQ[47:40]	DQS_{DP/DN}05	DQS_{DP/DN}05	DQS_{DP/DN}14
DQ[55:48]	DQS_{DP/DN}06	DQS_{DP/DN}06	DQS_{DP/DN}15
DQ[63:56]	DQS_{DP/DN}07	DQS_{DP/DN}07	DQS_{DP/DN}16
ECC[7:0]	DQS_{DP/DN}08	DQS_{DP/DN}08	DQS_{DP/DN}17

Note: In x16 configurations, only 4 DQSs are used. Others are non-connected. Also, DQS_N and DQS_P cannot be swapped.

4.1.2 DDR4 Clock to Command, Control and Address Signal Association

The following table shows the specific clock referenced to each processor DDR4 signal in the form of DLL groupings.

Table 4-3. DDR4 CMD/CTL/ADD/CLK DLL Groupings

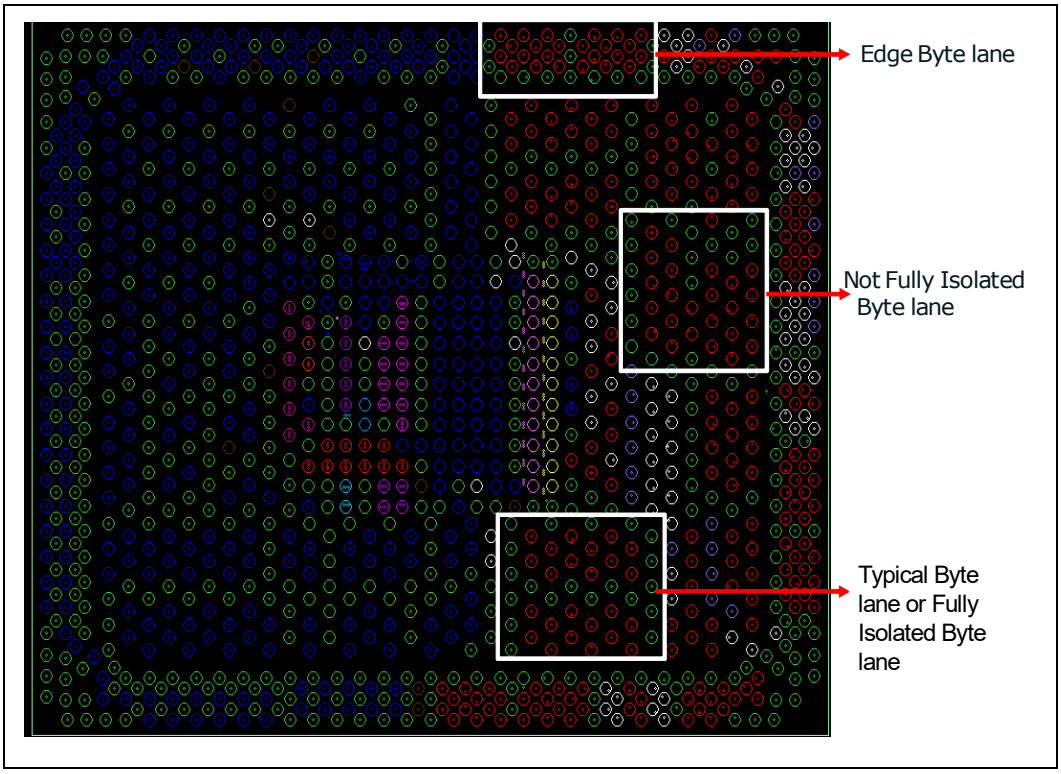
Group#	Associated CLK		Signals
	DIMM0	DIMM1	
1	DDR0_CLK[1,0]{P/N}	DDR0_CLK[3,2]{P/N}	DDR0_BG1_MA[14], DDR0_BG0_BA[2], DDR0_ACT_N_MA[15]
2	DDR0_CLK[1,0]{P/N}	DDR0_CLK[3,2]{P/N}	DDR0_MA[7], DDR0_MA[6], DDR0_MA[9], DDR0_MA[8], DDR0_MA[12], DDR0_MA[11]
3	DDR0_CLK[1,0]{P/N}	DDR0_CLK[3,2]{P/N}	DDR0_BA[1], DDR0_BA[0], DDR0_MA[10], DDR0_MA[0]
4	DDR0_CLK[1,0]{P/N}	DDR0_CLK[3,2]{P/N}	DDR0_MA[1], DDR0_PAR, DDR0_MA[3], DDR0_MA[2], DDR0_MA[5], DDR0_MA[4]
5	DDR0_CLK[1,0]{P/N}	DDR0_CLK[3,2]{P/N}	DDR0_MA[17], DDR0_MA[13], DDR0_MA15_CAS_N, DDR0_MA14_WE_N, DDR0_MA16_RAS_N
6	DDR0_CLK[0]{P/N}		DDR0_CKE[0], DDR0_CS_N[0], DDR0_ODT[0]
7	DDR0_CLK[1]{P/N}		DDR0_CKE[1], DDR0_CS_N[1], DDR0_ODT[1]
8		DDR0_CLK[2]{P/N}	DDR0_CKE[2], DDR0_CS_N[2], DDR0_ODT[2]
9		DDR0_CLK[3]{P/N}	DDR0_CKE[3], DDR0_CS_N[3], DDR0_ODT[3]

Note: Each CTL signal must be routed on the same layer with its associated LCK signals.

4.2 DDR4 General Routing Rules

4.2.1 Byte Lane Classification

Figure 4-1. DDR4 Byte Lane Classifications



4.2.2 Tabbed Routing Guide

Tabbed Routing is a method of attaching small trapezoidal tabs on adjacent parallel traces to better control the mutual capacitance and impedance of the signal traces. Tabbed routing implementation creates the opportunity for longer breakout lengths and compressed channel routing on external layers.

Tabbed routing DQ signals in a few implementations (secondary breakout/interdigital tabs, SoC pin field tabs, and open field/facing tabs) can achieve a variety of goals:

- To mitigate crosstalk and improve impedance on the very dense top surface routing layer.
- To improve the overall channel quality and to hit maximum speed. It is recommend additionally to use SoC pin field tabs (on both stripline and microstrip routing when possible) and facing tabs as shown in the CRB example. See Figure 4-2, "DDR4 Tabbed Routing Types."
- There are 6 bytelanes on the near channel and 3 bytelanes on the far channel that require top layer breakout routing. Those bytelanes are addressed in this section.

Note: Tabbed Routing is not required for the following conditions:

- Tabbed routing is not needed for CMD/ADD/CTL signals.
- 1SPC designs that target 50 Ohms for open field routing do NOT need tabbed routing.
- Stack-ups that do not allow for 3.5 mils trace width in the CPU pin field.

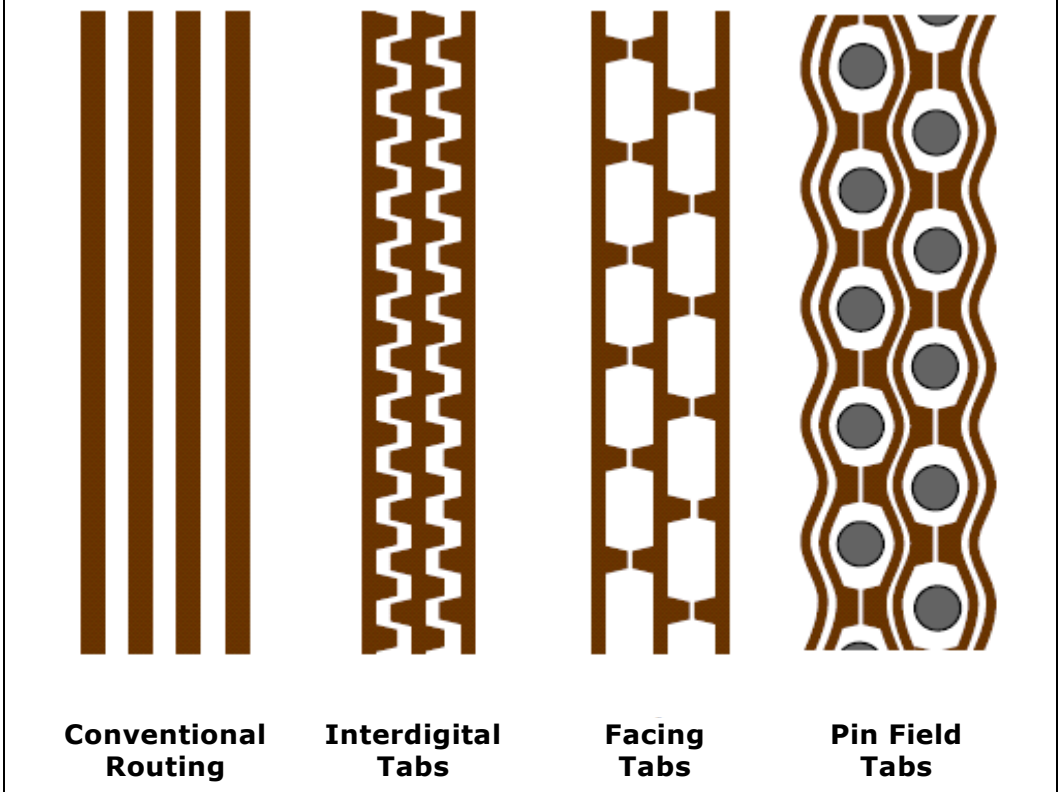
For more tabbed routing design details please refer to the following documents:

- Tabbed Transmission Line Design Basics, Rev. 1.0
- Graft Cadence Allegro PCB Editor SKILL Utility for Adding Tabbed Routing, Revision 2.5
- Tabbed Routing Design Parameter Conversion Tool for Skylake Server (Purley)

Note: The length scaling factor for microserver products between inner and outer tabbed DQ signals is not used for ease of implementation. A small routing envelope reduction would be achieved using one sided tabbed routing. Intel, however, has not pursued that routing strategy on their CRBs and it is not validated.

Note: The examples and dimensions presented are subject to change as work progresses on these connection topologies: usage and simulation results.

Figure 4-2. DDR4 Tabbed Routing Types



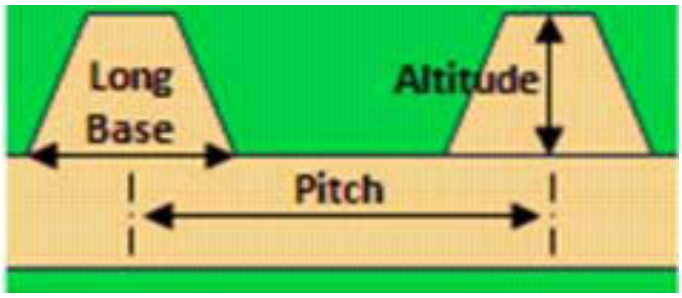
All tabbed routing solutions affect both impedance and noise

Pin Field tabs are better suited to impedance control

Interdigital Tabs and Facing Tabs are better suited to noise control
-Used in breakout and open field regions

Note: Facing Tabs not used on the CRBs described in this design guide. Furthermore, Interdigital tabbed routing for the Harrisonville platform requires boundary bits to have the same trace width and tab dimensions as the inner bits.

Figure 4-3. DDR4 Tab Design details



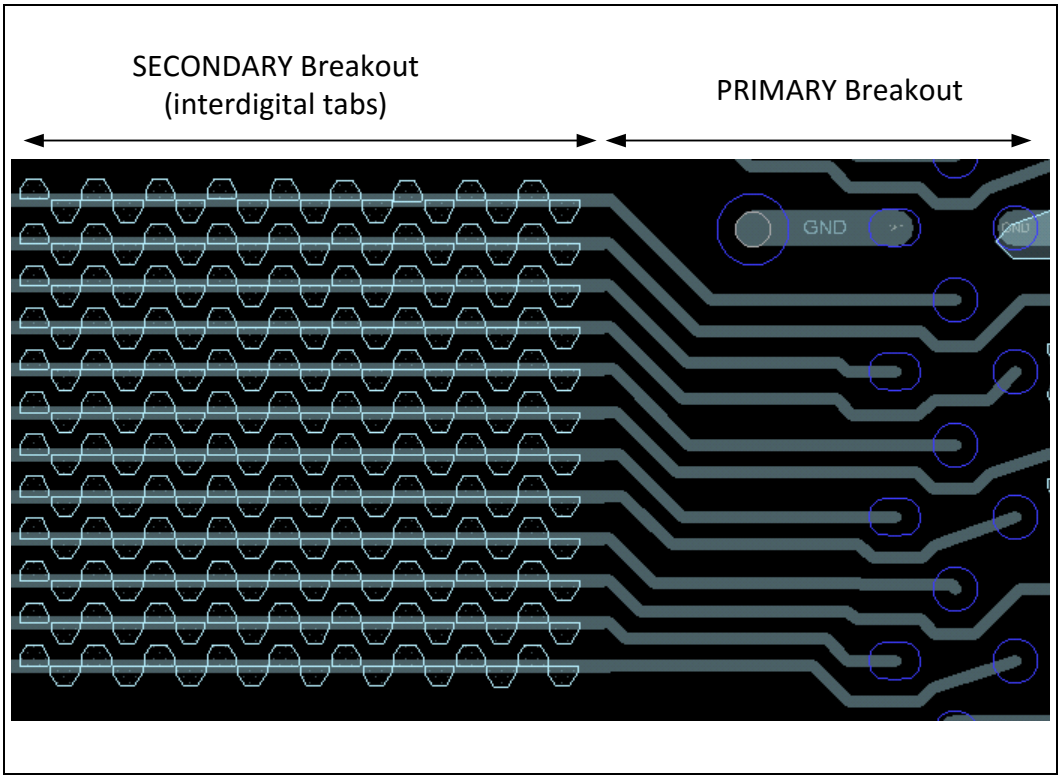
Pin Field Tabbed Lines (microstrip & stripline)
long base = 14 mils (microstrip/ stripline)
short base = 11 mils (microstrip/stripline)
altitude = 6.75 mils
line-to-line spacing in tabbed route section: 4 mils
width of nets in tabbed route section: 3.5 mils

Interdigital Tabbed Lines (microstrip – escape region)
long base = 8 mils
short base = 4 mils
altitude = 3.5 mils
pitch = 17 mils
line-to-line spacing in tabbed route section: 7.5 mils
width of nets in tabbed route section: 4 mils

Interdigital Tabbed Lines (microstrip-open field region)
long base = 6 mils
short base = 4 mils
altitude = 7 mils
Pitch = 30 mils
line-to-line spacing in tabbed route section: 12 mils
width of nets in tabbed route section: 4 mils

Note: Actual shape height which always equals ½ trace width + altitude shown above for single-sided tabs is different for traces with tabs on both sides of trace.

Figure 4-4. DDR4 Tab Design: Primary and Secondary Breakout Routing



4.2.2.1 Tabbed Routing Design recommendations

- Each DQ or DQS within a bytelane must have the same number of tabs. In the pin field tabbed routing should use the same number of tabs ± 1 tab for all bits.
- If a DQ or DQS breakout length will not allow tabbed design then none of the other longer DQ or DQS within the bytelane may have tabbed routing.
- Since each DQ or DQS trace within a bytelane must have the same number of tabs, treat each section (secondary breakout and open field tabbed routing) as independent regions. Interdigital tabbed routing requires boundary bits to have same trace width and tab dimensions as inner bits.
- The bytelane-to-bytelane spacing will be measured from trace-to-trace not from tab-to-tab.
- DQ bytelanes routed with tabbed routing (open field tabbed and secondary breakout tabbed) require 12*h* spacing for DQ to DQ within a bytelane, DQ to another DQ in the other memory channel, DQ to Command/Address/Command, and DQ to clock. The dielectric height, *h*, is measured to the nearest reference plane.
- No tab routing of any kind may be used for CMD/ADD/CTL/CLK signals.

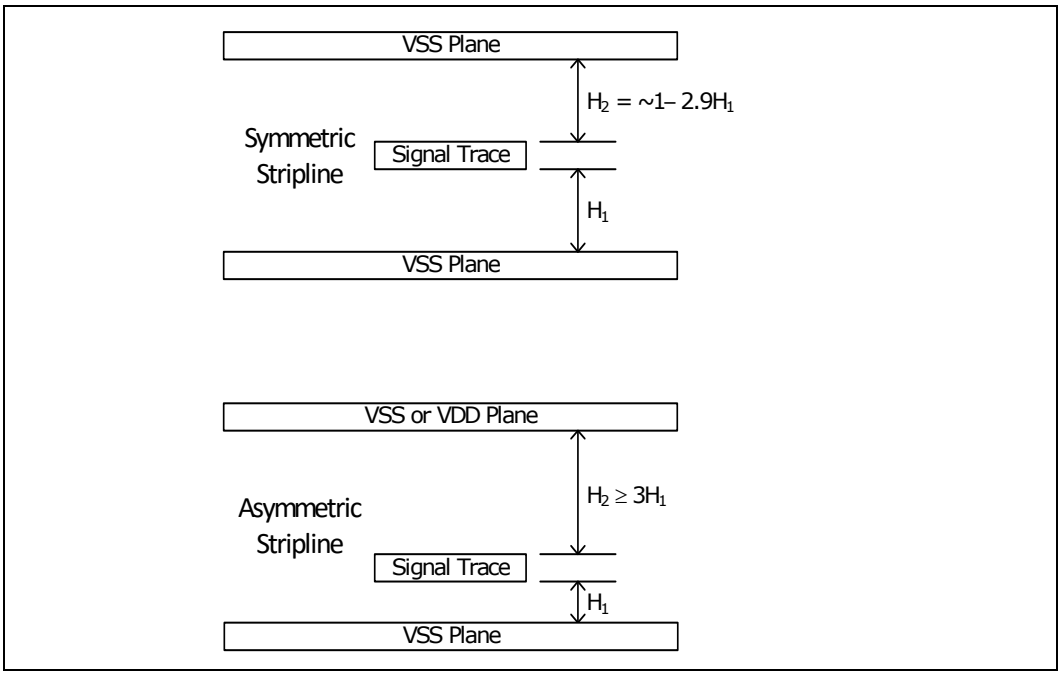
Note: Boundary lines or boundary bits should have double sided tabs.

4.2.3 General Design Guidelines

DDR4 DQ, DQS, and ECC signals require VSS referencing. No plane split crossings are allowed.

Dual referencing with VDD and VSS is allowed for DQ signals when the VDD plane is at least 3X the distance from the signal to VSS. (Example: DQ signal to VSS = 4mils, DQ signal to VDD ≥ 12 mils).

Figure 4-5. Referencing — Data and Data Strobe Signal Types



DDR4 CLK, CMD, and CTL signals require VDD referencing. No plane split crossings are allowed.

Dual referencing with VDD and VSS is allowed when the VSS plane is at least 3X the distance from the signal to VDD.

CLK and CTL signals for each DIMM must be routed on the same layer (See Table 4-3).

For memory down design case, CLK, CMD and CTL signal can reference to GND plane.

Microstrip routing for RDIMMs and UDIMMs is allowed. DDR4 DQ, DQS, and ECC signals are allowed to do microstrip routing for RDIMMs and UDIMMs. Stripline routing, however, is preferred. Only stripline routing is allowed for SODIMMs.

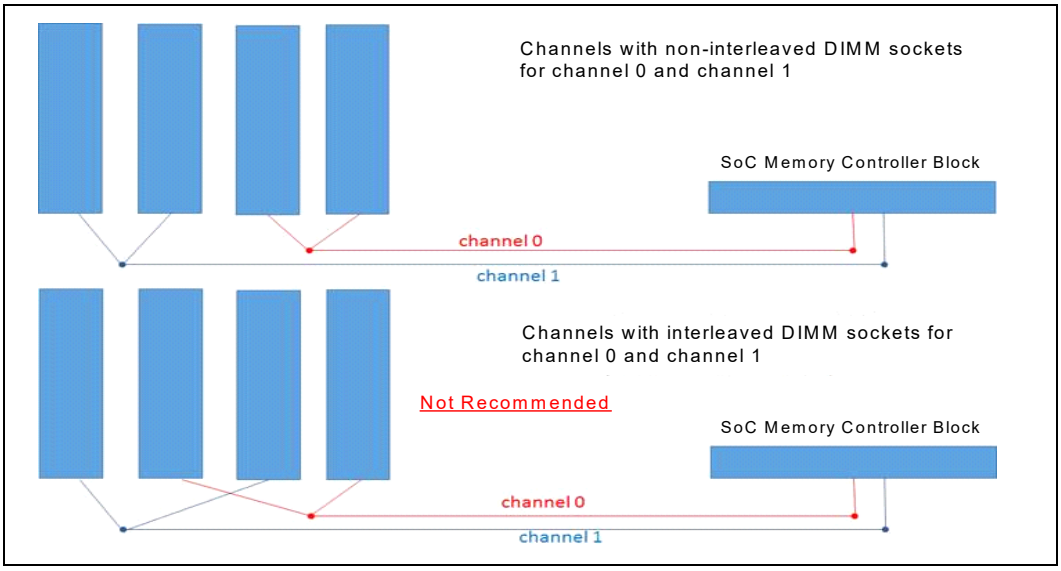
CMD, CTL and CLK signals can use Stripline and Microstrip routing for RDIMMs and UDIMMs. Microstrip routing is not advised for SODIMM configurations.

It is recommended for each CPU and DIMM socket that a Vss pin have a dedicated Vss via on the board following the same patterns as the package or socket pinout. This helps insure that the signal return path and isolation are preserved throughout the vertical transition path. Be aware that the VSS via sharing, if unavoidable, must be minimized.

There are several strong recommendations listed below that are to be followed when determining the DIMM socket placement and DIMM signal routing.

Do not interleave the DIMM sockets for channel 0 and 1.

Figure 4-6. Example of Interleaved and Non-Interleaved Sockets



Note: DIMM-to-DIMM spacing may be affected by thermal, mechanical, and airflow factors required for developing a thermally viable solution. Deviations based on platform thermal requirements should be carefully weighed against possible degradation of signal quality.

4.2.4 Stack-up Guidelines

The memory routing guidelines contained in this document assume the stack-ups described in Chapter 2, "Platform Stack-up and General Design Considerations". Platform designers may have to adjust trace width and/or spacing to meet impedance/crosstalk requirements if a different stack-up is used. Please note that special care is required for Dual Stripline stack up with signal to signal separation that is less than 10h due to extremely high inter layer routing coupling, refer to Chapter 2, "Platform Stack-up and General Design Considerations" for more details.

Table 4-4 below shows the PCB variation for DDR4 interface modeled by Intel. Refer to Appendix B for stack-up details.

Table 4-4. PCB Variation for Memory Interface

Parameter	Typical	Range
Dielectric height (h)	Refer to Appendix B for the stack-up details	± 0.5 mils
Trace width (w)		± 0.5 mils
Trace thickness (t)		± 0.2 mils
Dielectric permittivity (ε_ρ)		± 0.3

Note: The *Platform Design Guide (PDG)* is developed based on reasonable assumptions for Printed Circuit Board (PCB) High Volume Manufacturing (HVM) variations. Intel encourages discussion on the HVM parameter variations with the PCB suppliers. If these PCB variations cannot be met, specific transmission line models need to be constructed and simulated for risk assessment.

DDR4 signals routed on a microstrip or stripline layer must not be routed over plane splits for the near referencing plane. Care must be taken to ensure that the DQ/DQS/ECC signals are routed over a continuous return path.

It is recommended that referencing on the far plane should be strictly limited to DDR4 voltage planes only (DDR4: Vdd, Vpp, or Vss).

Considering manufacturing tolerances, it is recommended to leave 5 mils of spacing for signal routing near an edge or via. Routing a signal over voids is not allowed for more than 100 mil.

Keep DDR4 routing away from the components used in switching regulator circuits and any non-DDR4 related routing and components. DDR4 routing distance to high noise VR vias and shapes is at least 50 mils and to high noise VR traces at least 100 mils. DDR4 traces cannot be routed under phase fill nor near high noise VR inductors (at least 100 mil spacing is required). At least 300 mil spacing is required between a DDR4 via and a high noise VR via. If ground vias are added between these vias, the spacing can be reduced to 100 mils.

4.3 Two DIMM Slots Per Channel Design Guidelines

The platform can be designed to support two DIMMs slots per channel. Following guidelines support the design with UDIMM or RDIMM or SODIMM.

Table 4-8 shows DIMM connections for the socket specific clock, CKE, CS, and ODT signals.

Figure 4-7. DIMM Layout Implementation (Single Channel)

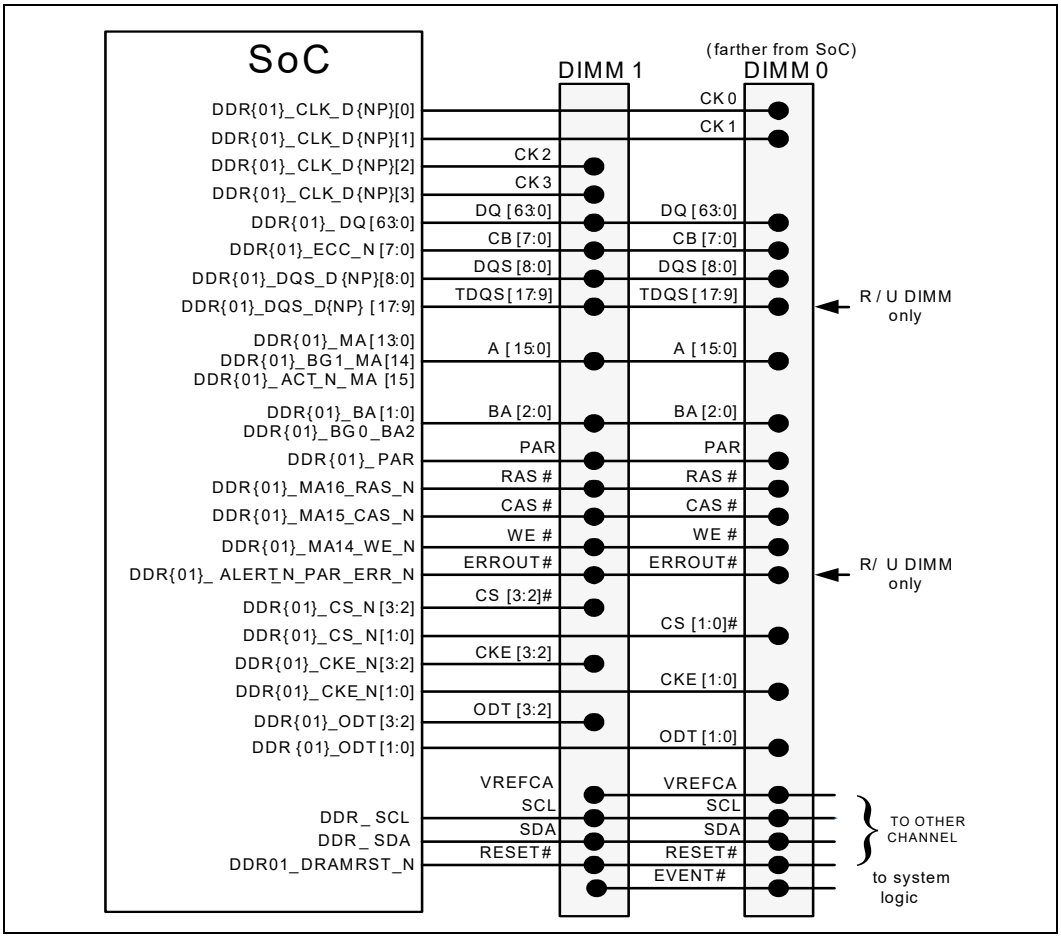


Table 4-5. DDR4 Processor Signal to DIMM Pin Mapping

DIMM	RDIMM pin	SODIMM pin	CPU Signal	DIMM Connections for	
				1DPC	2DPC
0	S0#	CS0_n	DDR{01}_CS_N[0]	Y	Y
0	S1#	CS1_n	DDR{01}_CS_N[1]	Y	Y
1	S0#	CS0_n	DDR{01}_CS_N[2]	N/A	Y
1	S1#	CS1_n	DDR{01}_CS_N[3]	N/A	Y
0	ODT0	ODT0	ODT0	Y	Y
0	ODT1	ODT1	ODT1	Y	Y
1	ODT0	ODT0	ODT2	N/A	Y
1	ODT1	ODT1	ODT3	N/A	Y
0	CKE0	CKE0	CKE0	Y	Y
0	CKE1	CKE1	CKE1	Y	Y
1	CKE0	CKE0	CKE2	N/A	Y
1	CKE1	CKE1	CKE3	N/A	Y
0	CK0	CK0_t	CLK_DP0	Y	Y
0	CK0#	CK0_c	CLK_DN0	Y	Y
0	CK1	CK1_t	CLK_DP1	Y	Y
0	CK1#	CK1_c	CLK_DN1	Y	Y
1	CK0	CK0_t	CLK_DP2	N/A	Y
1	CK0#	CK0_c	CLK_DN2	N/A	Y
1	CK1	CK1_t	CLK_DP3	N/A	Y
1	CK1#	CK1_c	CLK_DN3	N/A	Y

4.3.1 DDR4 Data, Data Strobe, Address and Command Signals

Data and strobe signals (DQ[63:00], DQS_{DP/DN}[17:00], ECC[7:0]) and Address/Command signals (MA[13:00], MA[17], BA[1:0], BG[1:0], RAS_N/MA[16],CAS_N/MA[15], WE_N/MA[14], PAR, and ACT_N) are routed in a "T" topology, shown in Figure 4-8.

Figure 4-9, Table 4-6, and Table 4-8 show the recommended topology and layout routing guidelines for the DDR4 data, strobe, address, and command signals.

Table 4-2 summarizes the DQ/ECC to DQS mapping. It is important to match the DQ/ECC signals to their associated DQS from processor signal pad to DIMM pin.

Address/Command signals need to be routed with power referencing as they are power referenced on the processor and on the DIMMs. VDDQ power island will need to be cut into the ground plane between the processor and the DIMMs to allow continuous power referencing for these signals.

Note: Bit swapping for DQ (data bits) is only allowed within a DQS (Data Strobe). This means:

- If the design supports x4 SDRAM devices then DQ bits can only be swapped within a nibble (4-bit) lane.
- If the design only supports x8 and/or x16 SDRAM devices then DQ bits can be swapped within an byte (8-bit) lane.

Tabbed routing not needed on the address. command, and clock signals.

Figure 4-8. DDR4 Source-Synchronous Signal (DQ, DQS, Address, Command) Routing

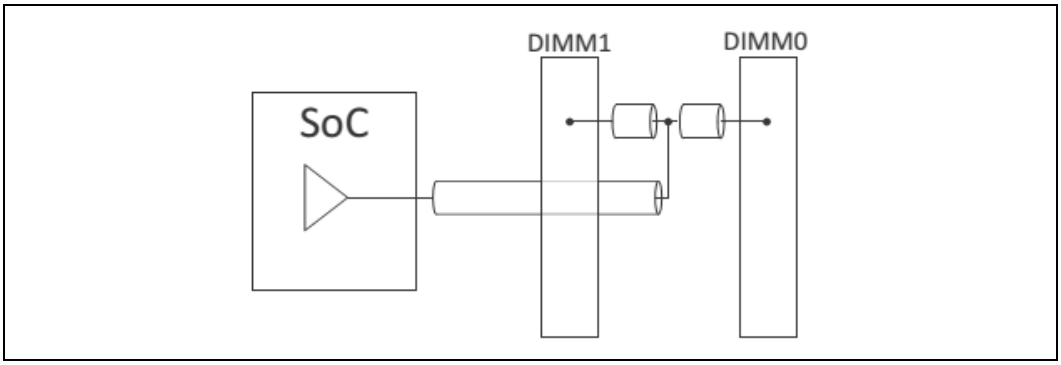
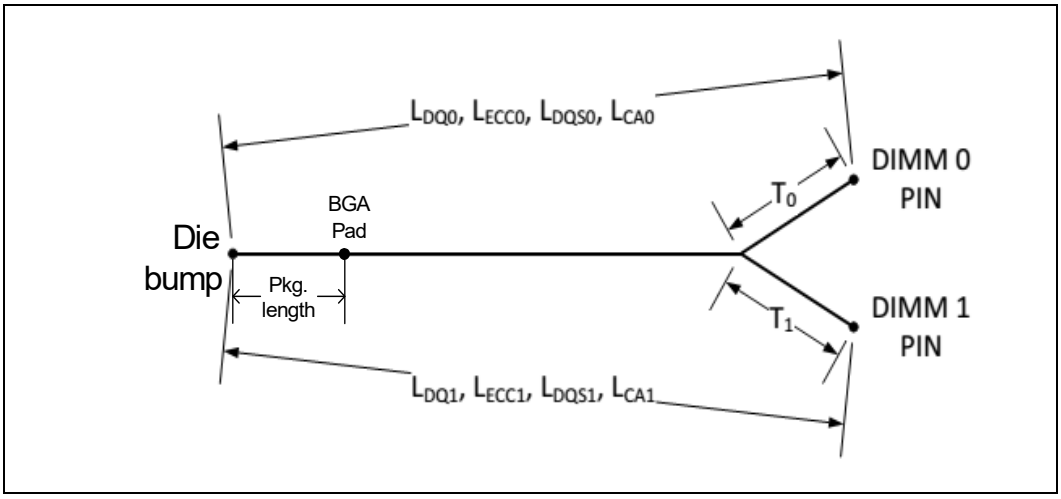


Table 4-6. DDR4 "T" Topology Length Matching

	Figure 4-9 ref.	mils
Stub length, DQ, ECC, DQS, CA	T_0, T_1	RDIMM, UDIMM < 350 SODIMM < 250
Mismatch between any DQ/ECC and DQS, within byte lane	$\lvert L_{DQ}-L_{DQS}\rvert$, $\lvert L_{ECC}-L_{DQS}\rvert$	300
Mismatch between any DQs or ECCs, within byte lane	$\lvert L_{DQx}-L_{DQy}\rvert$, $\lvert L_{ECCx}-L_{ECCy}\rvert$	100
Mismatch of T stubs on same net for DQ, DQS, CA	$\lvert T_0-T_1\rvert$	10

For T-topology branch routing a trace width of 3.5 mils is recommended (or the minimum manufacturing trace width). T-branch sections can have a minimum spacing of 6.9 mils (microstrip) or 4.9 mils (stripline) for 2 track routing for RDIMM/UDIMM boards. If needed, necking down the trace width to 3.5 mils and spacing to 4 mils (3 track routing for RDIMM/UDIMM boards) is allowed for a max accumulated length of 100 mils. Bytelane to bytelane reduced spacing of 9 mils can be allowed for up to 100 mils cumulative length.

Figure 4-9. DDR4 "T" Topology Length Diagram



4.3.1.1 Breakout Types

There are two types of breakout routings: homogeneous and two track routing.

Figure 4-10. Homogeneous Routing Breakout for "edge" Bytelanes. The Strobe signals are highlighted in yellow.

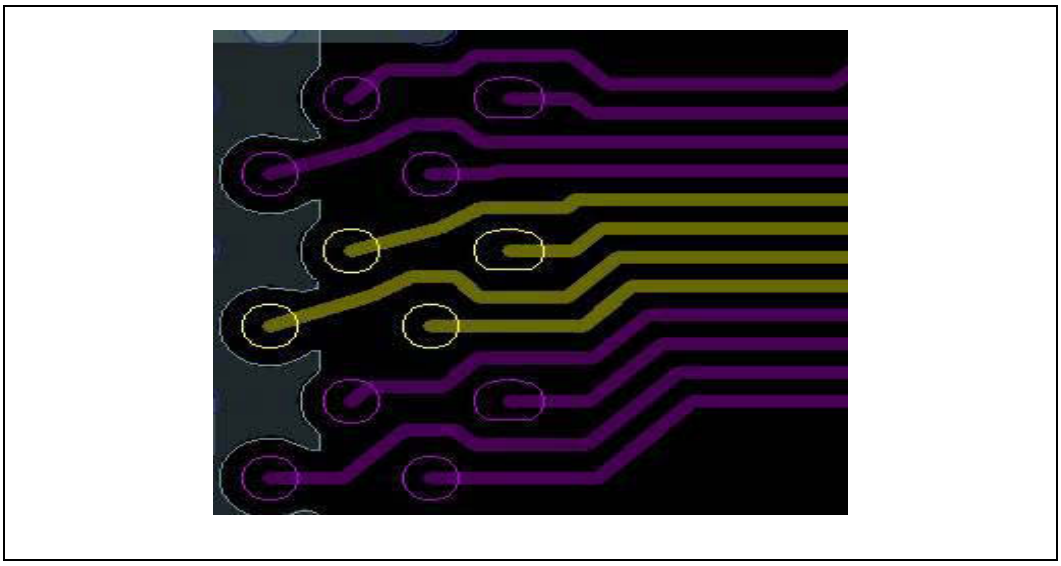


Figure 4-11. 2 Track Routing Breakout with Tabs in the Pin Field.

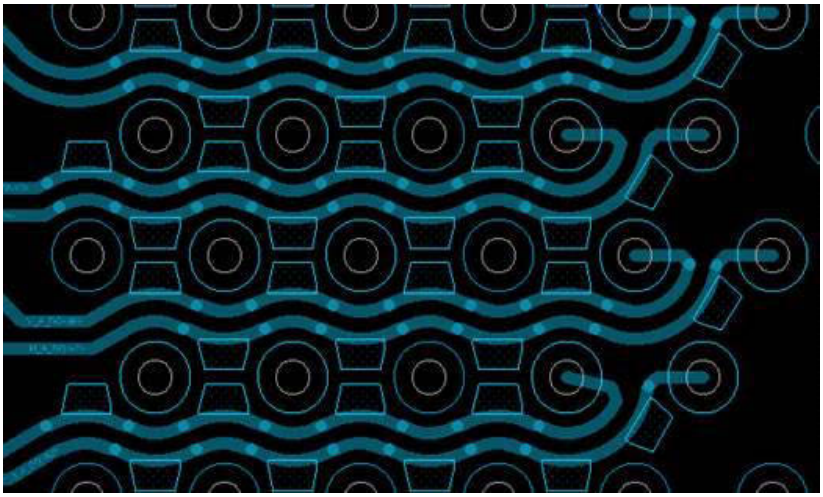
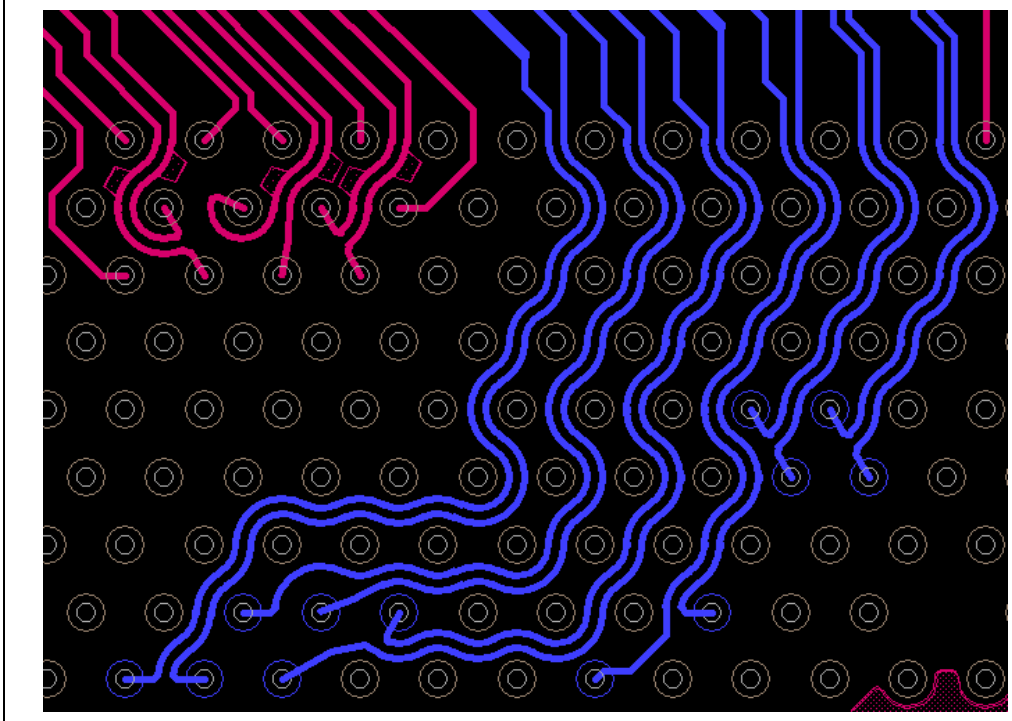


Figure 4-12. 2 Track Routing Example for CMD/ADD/CTL/CLK Signals



The following applies to DQ/DQS/Command/Address/Control/Clock Signal Groups.

3.5-mil width/4-mil spacing is recommended with 2 track routing (track to track minimum spacing of 16 mils) within the BGA area. 4 mil width is preferred when not using a 2 track or restricted spacing design.

Outside the BGA area maintain 2 track routing or spread out to form uniform spacing (4 mil width with 8 mil spacing, for example) when possible. DQS signals within a pair can maintain 4 mils spacing outside the BGA area. Spacing violations in breakout region must not exceed 0.5 mils.

Length matching should not be done in the processor breakout region; signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Avoid serpentine routing in this region. OPEN field width is allowed (preferred) after the dogbone if the OPEN field spacing can be maintained. This includes the reduced spacing allowance in Note 3 of Table 4-7.

Note: For all routing guidelines "*h*" is the dielectric height measured to the nearest reference plane.

Table 4-7. DDR4 Data and Strobe Routing Guidelines (Sheet 1 of 2)

Parameter	Guideline	Figure
Signal Group	DQ[63:00], ECC[7:0], DQS_{DP/DN}[17:00]	
Topology	"T"	Figure 4-8
Reference Plane	Data and strobe: Dual referencing with VDD and VSS is allowed for DQ when the VDD plane is at least 3X the distance from the signal versus VSS. Address and command: VDD referenced	Figure 2-1
Layer Assignment[1]	Microstrip or Stripline (preferred)	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
DQ/ECC Characteristic Trace Impedance (Zo)	40 Ω ± 10% (Microstrip) 40 Ω ± 10% (Stripline)	
DQS Single Ended Characteristic Trace Impedance (Zo) [2]	40 Ω ± 10% (Microstrip) 40 Ω ± 10% (Stripline)	
DQ/ECC/DQS Nominal Self Spacing in the Open Field	≥ 6.4*h* for Microstrip ≥ 4.5*h* for Stripline	
DQ/ECC Nominal Trace Spacing (intra-byte lane) in Open Field (between Processor and Closest DIMM Slot) [1, 3, 4]	≥ 6.4*h* Microstrip ≥ 4.5*h* Stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the inter-byte lane boundaries) [5]	≥ 12*h* Microstrip ≥ 11*h* Stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the ch-to-ch boundaries on the same layer) [5]	≥ 12*h* Microstrip ≥ 11*h* Stripline	
DQ/ECC Nominal Trace Spacing in DIMM Pin Field [6, 7]	7 mils for both Microstrip and Stripline for 2 track routing (RDIMM and UDIMM) 8 mils for both Microstrip and Stripline for homogeneous routing (SODIMM)	
DQS Nominal Differential Trace Spacing (Open Field and DIMM Pin Field) [8]	5 mils Microstrip 4.5 mils Stripline Open Field minimum target spacing for DQS_P/DQS_N if needed can be 4 mils for both Microstrip and Stripline routing.	
DQS to DQ Nominal Trace Spacing (Open Field and DIMM Pin Field) [3, 6]	≥ 8*h* Microstrip ≥ 6.5*h* Stripline	
Trace Length max, die to DIMM pin (Figure 4-9: L_{DQ0}, L_{DQ1}, L_{DQS0}, L_{DQS1}) with package length	Ch. 0 RDIMM, UDIMM min = 2.0", max 4.3" Ch. 0 SODIMM: min = 1.8", max = 3.1" Ch. 1 RDIMM, UDIMM min = 2.4", max = 5.6" Ch. 1 SODIMM: min = 2.2", max = 4.6"	Figure 4-9, Table 4-6
Length Tuning Requirement - Data to Strobe (Figure 4-9)	Within a data group (defined in Table 4-2), DQ/ECC and DQS lengths must match as shown in the table. Within a DQS pair, the P and N signals must match to each other within 5 mils.	Figure 4-9, Table 4-6
Length Tuning Requirement - Data to Data (Figure 4-9)	Within a data group (defined in Table 4-2), DQ or ECC signals should match to each other within as shown in the table. No length matching across DQ groups.	Figure 4-9, Table 4-6

Table 4-7. DDR4 Data and Strobe Routing Guidelines (Sheet 2 of 2)

Parameter	Guideline	Figure
"T" junction to DIMM pin routing, both arms	3.5 mil width, 16 mil spacing	Figure 4-9, Table 4-6
Processor Breakout Requirements	Primary Breakout - 3.5-mil width/4-mil spacing with 2 track routing (track to track spacing minimum of 16 mils) within BGA area. 4 mil width preferred if not 2 track or restricted spacing. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing when possible. DQS signals within a pair can maintain 4 mils spacing after BGA area. Spacing violations in breakout region must not exceed 0.5 mils. Minimize the length of those violations. Allow 3.5 mil width and 4 mil spacing for up to 150 mils accumulated trace length outside of the BGA area. Total breakout routing cannot exceed 600 mils for stripline and microstrip. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field where they attain the normal width/spacing. Avoid serpentine routing in this region. OPEN field width is allowed, and preferred, after the dogbone if OPEN field spacing can be maintained including the reduced spacing allowance in note 8.	
Dogbone	Max length = 50 mils	

Notes:

1. Signals within a group, including associated strobes, must be routed on the same layer. Refer to Table 4-2 for definition of data groups and associated strobes.
2. Board designers using stack-ups other than the reference stack-ups must follow the single ended impedance guidelines for trace width.
3. Open field regions can have reduced nominal spacing for no more than,
   - 100mils cumulative length when the nominal spacing violation is less than 1h mils (h is the dielectric height from the closest reference plane)
   - 200mils cumulative length when the nominal spacing violation is less than h/2 (where h is the dielectric height from the closest reference plane)

   For example if h equals 4 mils:
   - 4 mil (h) violation of the nominal spacing (13.5 mils) is allowed for a 100 mil length. Spacing can be 13.5-4 = 9.5 mils for up to 100 mils.
   - 2 mil (h/2) violation of the nominal spacing (13.5 mils) is allowed for 200 mils length. Spacing can be 13.5-2 = 11.5 mils for up to 200mils
4. This same spacing guideline is applied between DQ/ECC and all other non-DDR signals unless otherwise specified in this document.
5. This same spacing guideline should be applied between DQ/ECC and high speed differential signals such as PCIe*/SATA 6 Gb/USB 3.0/USB 2.0 routes.
6. Minimal Trace Spacing in the DIMM Pin Field can be 6.9/4.9 mils (Microstrip/Stripline) (2 track routing). If needed, necking down the trace width to 3.5 mils and spacing to 4 mils (3 track routing) is allowed for a maximum length of 100 mils.
   - When routing with homogeneous spacing in the DIMM Field region (SODIMM boards) maintain a spacing of 11*h* between DQ and another DQ in the same bytelane, DQ and another DQ on the other memory channel, DQ to Command/Address/Control, and DQ to clock.
7. Avoid routing DQ/ECC/DQS signals from different bytes and/or different channels in the same track between pins in the DIMM pin field region. Channel-to-Channel and Bytelane-to-Bytelane spacing does not need to be met in the DIMM pin field region.
8. Keep nominal spacing wherever possible. Restrict DIMM pin field routing to 1-track only where possible. Limit the length where a DQS pair splits around a DIMM pin to no more than 1 pin.

Table 4-8. DDR4 Command and Address Routing Guidelines

Parameter	Guideline	Figure
Signal Group	MA[13:0], MA14_WE_N, MA15_CAS_N, MA16_RAS_N, BG1_MA[14], BG0_BA[2], BA[1:0], BG1_MA[14], ACT_N_MA15, PAR	
Topology	"T"	Figure 4-8
Reference Plane	VDDQ Referenced Dual referencing with VDD and VSS is allowed for CMD/ADD when the VSS plane is at least 3X the distance from the signal to VDD. (Example: signal to VDD = 4mils, signal to VSS 12mils).	Figure 2-1
Layer Assignment [1]	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
Characteristic Trace Impedance (Z_0)	40 Ω ± 10% (Microstrip) 40 Ω ± 10% (Stripline)	
Nominal Trace Spacing in Open Field (between Processor and Closest DIMM Slot) [2]	5.4*h* (Microstrip) 4.3*h* (Stripline)	
Nominal Trace Self-Spacing in the Open Field and DIMM Field (when applicable)	$\geq$ 5.4*h* (Microstrip) $\geq$ 4.3*h* (Stripline)	
CMD to DQ Nominal Trace Spacing in Open Field [2]	$\geq$ 11*h* Microstrip $\geq$ 11*h* Stripline	
Nominal Trace Spacing in DIMM Pin Field [2]	7 mils/47 mils for both Microstrip and Stripline for 2 track routing (RDIMM and UDIMM) 8 mils for both Microstrip and Stripline for homogeneous routing (SODIMM)	
Trace Length Maximum, die-to-DIMM pin (Figure 4-9: L_{CA0}, L_{CA1}), with package length	Ch. 0 RDIMM, UDIMM Min = 1.7", max 3.85" Ch. 0 SODIMM: min = 1.5", max = 3.35" Ch. 1 RDIMM, UDIMM Min = 2.00", max 4.8" Ch. 1 SODIMM: min = 1.9", max = 4.6"	Figure 4-9, Table 4-6
"T" junction to DIMM pin routing, both arms	A trace width of 3.5 mils is recommended (or the minimum manufacturing trace width), T-branch sections can have a minimum spacing of 6.9 mils (microstrip) or 4.9 mils (stripline): 2 track routing for RDIMM/UDIMM boards. If needed, necking down the trace width to 3.5 mils and spacing to 4 mils (3 track routing for RDIMM/UDIMM boards) is allowed for a max accumulated length of 100 mils. Bytelane to bytelane reduced spacing of 9 mils can be allowed for up to 100 mils cumulative length.	
Length Tuning Requirement, including package length	All address and command signals need to match to all CLK signals within 1" at each DIMM.	
Length Tuning Requirement max(LCA) - min(LCA), including package length	Within a DLL group (defined in Table 4-3), command and address signals need to match to each other within 25 mils. No length matching across CMD DLL groups.	Figure 4-9, Table 4-6
Processor Breakout Requirements	3.5 mil width/4 mil minimum spacing (with 2 track routing track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. Total breakout routing cannot exceed 1" for stripline (2 track routing) and 700 mils for microstrip (2 track routing), 250 mils for homogeneous (4 mils wide/ 4 mils spacing) spacing. This length should be minimized. Trace to trace spacing violations of 0.5 mils can be tolerated for up to 100 mils cumulative length. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Avoid serpentine routing in this region.	

Notes:
1. Signals within a group must be routed on the same layer. Refer to Table 4-3 for definition of data groups and associated strobes.
2. Keep nominal spacing wherever possible. Minimize reduced spacing in the DIMM field.

4.3.2 DDR4 Control Signals

Figure 4-13. DDR4 Control Signal Diagram

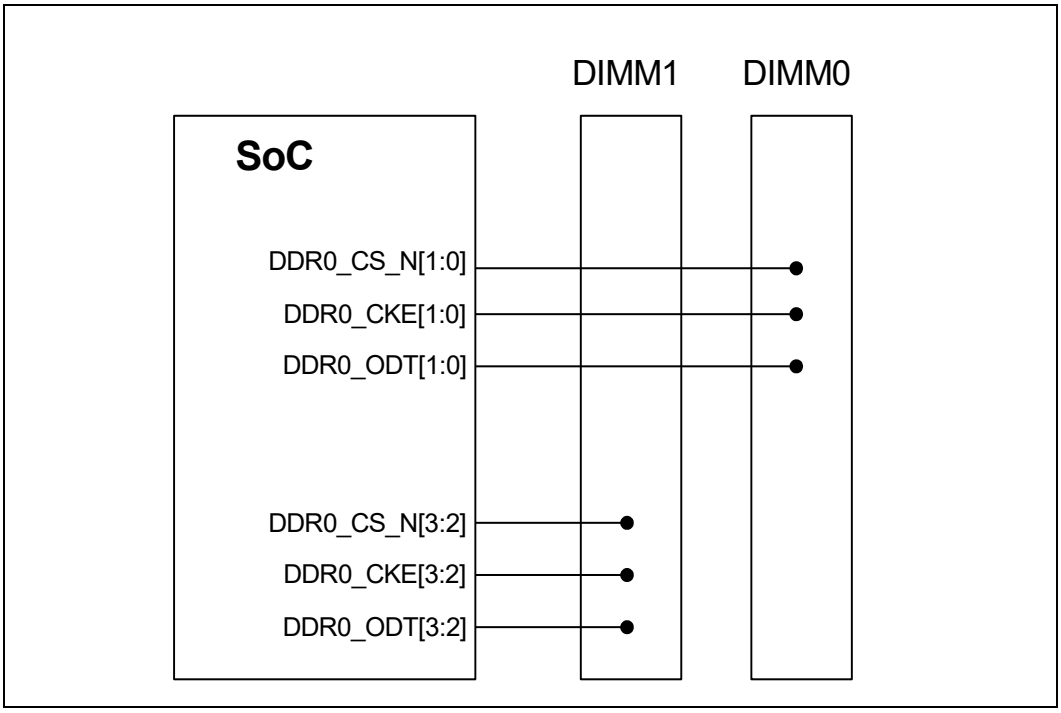


Table 4-9. DDR4 Point-to-Point Control Signal Routing Guidelines (Sheet 1 of 2)

Parameter	Guidelines	Figure
Signal Group	CS_N[3:0], ODT[3:0], CKE[3:0]	
Topology	Point-to-point	Figure 4-17
Reference Plane	VDDQ Referenced Dual referencing with VDD and VSS is allowed for CTL when the VSS plane is at least 3X the distance from the signal to VDD. (Example: signal to VDD = 4mils, signal to VSS 12mils).	Figure 2-1
Layer Assignment [1]	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
Layer constraint	Signals in groups 6, 7, 8, and 9 must be routed on the same layer as their associated clock.	Table 4-3
Characteristic Trace Impedance (Zo)	40 Ω ± 10% (Microstrip) 40 Ω ± 10% (Stripline)	
Nominal Trace Spacing in Open Field [2]	≥ 5.4*h* Microstrip ≥ 4.3*h* Stripline	
Nominal Trace Self-Spacing in the Open Field and DIMM Field (when applicable)	≥ 5.4*h* (Microstrip) ≥ 4.3*h* (Stripline)	
CTL to DQ Nominal Trace Spacing in Open Field [2]	≥ 11*h* Microstrip ≥ 11*h* Stripline	

Table 4-9. DDR4 Point-to-Point Control Signal Routing Guidelines (Sheet 2 of 2)

Parameter	Guidelines	Figure
Nominal Trace Spacing in DIMM Pin Field [2]	7 mils/47 mils for both Microstrip and Stripline for 2 track routing (RDIMM and UDIMM) 8 mils for both Microstrip and Stripline for homogeneous routing (SODIMM) If needed, necking down the trace width to 3.5 mils and spacing to 4 mils (3 track routing) is allowed for a max accumulated length of 0.1”.	
Trace Length Maximum, die-to-DIMM Pin with package length	Ch. 0 long RDIMM, UDIMM Min = 1.50”, max 3.6” Ch. 0 long SODIMM: min = 1.5”, max = 3.6” Ch. 1 short RDIMM, UDIMM min = 1.7”, max 4.4” Ch. 1 short SODIMM: min = 1.7”, max = 4.4”	Figure 4-13
Length Tuning Requirement with package length	Within a DLL group (defined in Table 4-3), each CTL signal needs to match to the associated CLK signal within these limits: • RDIMM: within 100 mils • UDIMM: within 25 mils • SODIMM: within 25 mils No length matching is needed across CTL DLL groups. Control signals must be routed on the same layer as associated clock. Package length must be included when matching lengths within a DLL group.	Figure 4-13
Processor Breakout Requirements	3.5 mil width/4 mil minimum spacing (with 2 track routing track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/ 8-mil spacing. Total breakout routing cannot exceed 1” for stripline (2 track routing), 600 mils for microstrip (2 track routing), and 250 mils for homogeneous (4 mils wide/ 4 mils spacing) spacing. This length should be minimized. Trace to trace spacing violations of 0.5 mils can be tolerated for up to 100 mils cumulative length. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/ spacing. Avoid serpentine routing in this region.	

Notes:
1. Signals within a group must be routed on the same layer. Refer to Table 4-3 for definition of data groups and associated strobes.
2. Keep nominal spacing wherever possible. Minimize reduced spacing in the DIMM field.

4.3.3 DDR4 Clock Signal Guidelines

The SoC provides four differential clock pairs (CLK_{DP/DN}[3:0]). The processor generates and drives these differential clock signals required by the DDR4 interface. No external clock driver is required.

One differential clock pair is routed to each DIMM connector (see Table 4-5). The differential clock pair must be routed differentially from the processor balls to their associated DIMM pins and must maintain the correct isolation spacing from other signals. While serpentining the differential clock pair must maintain correct spacing to remain differential as well.

The clock signals need to be routed with power referencing as they are power referenced on the processor and on the DIMMs. VDDQ power island needs to be cut into the ground plane between the processor and the DIMMs to allow continuous power referencing for the clock signals.

Clock design is using point to point clock topology. Figure 4-14 and Table 4-10 below show the recommended topology and layout routing guidelines for the DDR4 differential clocks that are point-to-point to the DIMM.

Figure 4-14. DDR4 Clock Signal Diagram

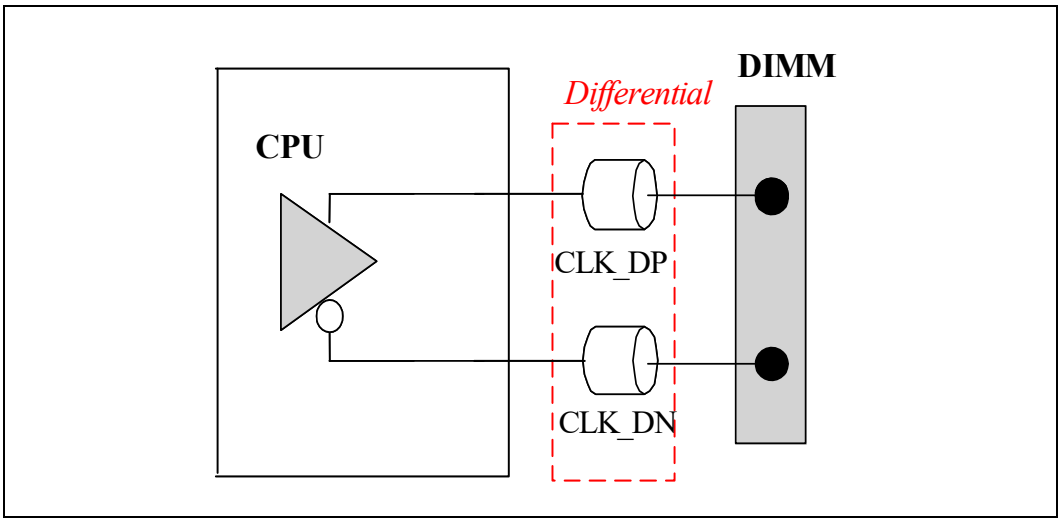


Table 4-10. DDR4 Clock Signal Routing Guidelines

Parameter	Guideline	Figure
Signal Group	CLK_{DP/DN}[0],CLK_{DP/DN}[1], CLK_{DP/DN}[2],CLK_{DP/DN}[3]	
Topology	Point-to-point	Figure 4-14
Reference Plane	VDDQ referenced Dual referencing with VDD and VSS is allowed for CLK when the VSS plane is at least 3X the distance from the signal to VDD. (Example: signal to VDD = 4mils, signal to VSS 12mils).	Figure 2-1
Layer Assignment	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field (SODIMM only: layer change at connector is allowed)	Figure 2-1
Characteristic Trace Impedance (Zo) [1]	40 Ω ± 10% (Microstrip) 40 Ω ± 10% (Stripline)	
DN to DP Trace Spacing in Open Field	5 mils (Microstrip) 4.5 mils (Stripline)	
DN to DP Differential Trace Spacing in DIMM Pin Field [2]	5 mils (Microstrip) 4.5 mils (Stripline)	
Nominal Trace Self-Spacing in the Open Field and DIMM Field (when applicable)	$\geq$ 5.4*h* (Microstrip) $\geq$ 4.3*h* (Stripline)	
Group Spacing: CLK to CLK and CLK to Command/ Address/Control	$\geq$ 5.4*h* (Microstrip) $\geq$ 4.3*h* (Stripline)	
Group Spacing: CLK to DQ	$\geq$ 11*h* (Microstrip and Stripline)	
Trace Length - die to DIMM Pin with package length	RDIMM/UDIMM/SODIMM Min = 1.5” (Microstrip) Max = 3.6” (Microstrip) Min = 1.7” (Stripline) Max = 4.4” (Stripline)	Figure 4-14
Processor Breakout Requirements	3.5 mil width/4 mil minimum spacing (with 2 track routing track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. Total breakout routing cannot exceed 1” for stripline (2 track routing), 600 mils for microstrip (2 track routing), and 550 mils for homogeneous (4 mils wide/ 4 mils spacing) spacing. This length should be minimized. Trace to trace spacing violations of 0.5 mils can be tolerated for up to 100 mils cumulative length. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Avoid serpentine routing in this region.	
Length Tuning Requirement with package length	Within a CLK pair, the P and the N signals must match to each other within 2 mils.	Figure 4-14
Length Tuning Requirement for clocks to same DIMM	|max(CLK_D{NP}[0]) - min(CLK_D{NP}[1])| ≤ 5 mils |max(CLK_D{NP}[2]) - min(CLK_D{NP}[3])| ≤ 5 mils	Figure 4-14

Notes:
1. Board designers using stack-ups other than the reference stack-ups are encouraged NOT to follow differential impedance but to follow Single Ended impedance guideline and same differential spacing of 5 mils microstrip and 4.5 mils stripline.
2. Keep nominal spacing wherever possible. Route differentially.
3. Clock signals do not need tabbed routing.

4.4 One DIMM Slot per Channel Guidelines

One DIMM (UDIMM, RDIMM, or SODIMM) per channel at a maximum interface speed of 2400 MT/s can be supported. Tabbed routing is not needed nor recommended for this design topology.

4.4.1 DDR4 Data, Data Strobe, and ECC Signals

Table 4-2 summarizes the DQ/ECC to DQS mapping. It is important to match the DQ/ECC signals to their associated DQS from processor signal pad to DIMM pin. Figure 4-15 and Table 4-11 below show the recommended topology and layout routing guidelines for the DDR4 data signals.

Figure 4-15. DDR4 Data and Data Strobe Routing Diagram

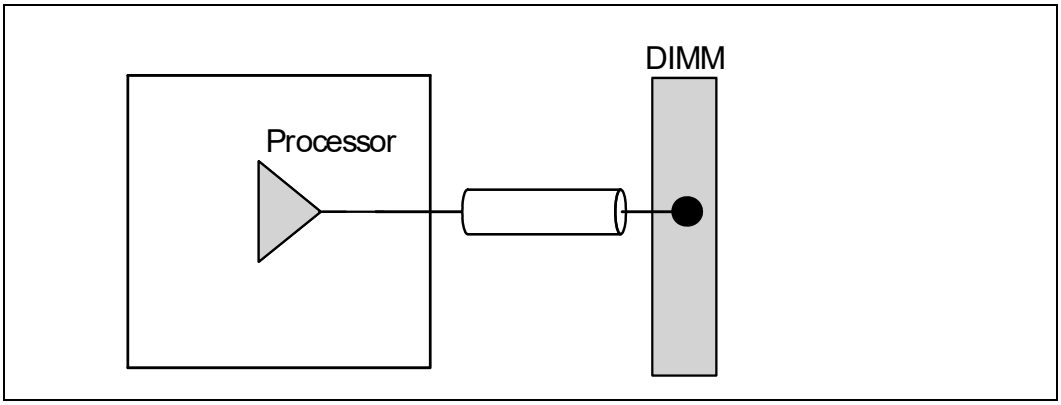


Table 4-11. DDR4 Data and Strobe Routing Guidelines (Sheet 1 of 2)

Parameter	Guideline	Figure
Signal Group	DQ[63:00], ECC[7:0], DQS_{DP/DN}[17:00]	
Topology	point-to-point	Figure 4-8
Reference Plane	Ground referenced	Figure 2-1
Layer Assignment [1]	Microstrip or Stripline (preferred)	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
DQ/ECC Characteristic Trace Impedance (Zo)	50 Ω ± 10% (Microstrip) 50 Ω ± 10% (Stripline)	
DQS Single Ended Characteristic Trace Impedance (Zo) [2]	50 Ω ± 10% (Microstrip) 50 Ω ± 10% (Stripline)	
DQ/ECC/DQS Nominal Trace Width (stack up dependent)	4.13 mils (Microstrip) 4.0 mils (Stripline)	
DQ/ECC/DQS Nominal Self Spacing in the Open Field	≥ 16 mils (Microstrip) ≥ 16 mils (Microstrip)	
DQ/ECC Nominal Trace Spacing (intra-byte lane) in Open Field (between Processor and Closest DIMM Slot) [1, 3, 4]	≥ 4.8*h* Microstrip ≥ 4.0*h* Stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the inter-byte lane boundaries) [5]	≥ 12.8*h* Microstrip ≥ 11*h* Stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the ch-to-ch boundaries on the same layer) [5]	≥ 12.8*h* Microstrip ≥ 11*h* Stripline	
DQ/ECC Nominal Trace Spacing in DIMM Pin Field [6, 7]	7.03*h* Microstrip 3.25*h* Stripline	
DQS Nominal Differential Trace Spacing (Open Field and DIMM Pin Field) [8]	5 mils Microstrip 5 mils Stripline Open Field minimum spacing for DQS_P/DQS_N if needed can be 4 mils for both Microstrip and Stripline routing.	
DQS to DQ Nominal Trace Spacing (Open Field DIMM Pin Field) [3, 6, 8]	≥ 4.8*h* Microstrip ≥ 4*h* Stripline	
Trace Length max, die to DIMM pin with package length	RDIMM/UDIMM • Microstrip =1.5” - 4.3” • Stripline =1.9” - 5.6” SODIMM • Microstrip =1.3” - 3.1” • Stripline =1.7” - 4.6”	Figure 4-9, Table 4-6
Length Tuning Requirement - Data to Strobe (Figure 4-9)	Within a data group (defined in Table 4-2), DQ/ECC and DQS lengths must match as shown in the table. Within a DQS pair, the P and N signals must match to each other within 5 mils.	Figure 4-9, Table 4-6

Table 4-11. DDR4 Data and Strobe Routing Guidelines (Sheet 2 of 2)

Parameter	Guideline	Figure
Length Tuning Requirement - Data to Data (Figure 4-9)	Within a data group (defined in Table 4-2), DQ or ECC signals should match to each other within as shown in the table. No length matching across DQ groups.	Figure 4-9, Table 4-6
Processor Breakout Requirements	3.5-mil width/4-mil spacing for 2 track routing the track to track minimum spacing is 16 mils within BGA area. After BGA area spread out use 4-mil width/8-mil spacing or maintain 2 track routing. DQS signals within a pair can maintain 4 mils spacing after BGA area. Spacing violations in breakout region must not exceed 0.5 mils. Minimize the length of those violations. Total breakout routing cannot exceed 600 mils for stripline and microstrip. Minimize this length as much as possible. Length matching should not be done in the processor breakout region. Signals should route directly from their pin to the exit of the pin field where they attain the normal width/spacing. Avoid serpentine routing in this region. Maximum breakout length can be violated, if unavoidable, by as much as 50 mils without significant impact to overall voltage timing margins.	
Processor land to motherboard via	Max length = 50 mils	

Notes:

1. Signals within a group, including associated strobes, must be routed on the same layer. Refer to Table 4-2 for definition of data groups and associated strobes.
2. Board designers using stack-ups other than the reference stack-ups must follow the single ended impedance guidelines for trace width.
3. Open field regions can have reduced nominal spacing for no more than,
   - 100mils cumulative length when the nominal spacing violation is less than 1*h* mils (*h* is the dielectric height from the closest reference plane).
   - 200mils cumulative length when the nominal spacing violation is less than *h*/2 (where *h* is the dielectric height from the closest reference plane).

     For example if h equals 4 mils:
   - 4 mil (*h*) violation of the nominal spacing (13.5 mils) is allowed for a 100 mil length. Spacing can be 13.5-4 = 9.5 mils for up to 100 mils.
   - 2 mil (*h*/2) violation of the nominal spacing (13.5 mils) is allowed for 200 mils length. Spacing can be 13.5-2 = 11.5 mils for up to 200mils.
4. This same spacing guideline is applied between DQ/ECC and other non-DDR signals unless otherwise specified elsewhere in this document.
5. This same spacing guideline should be applied between DQ/ECC and all high speed differential signals such as PCIe*/SATA 6 Gb/USB 3.0/USB 2.0 routes.
6. Minimal Trace Spacing in the DIMM Pin Field can be 6.9/4.9 mils (Microstrip/Stripline) (2 track routing). If needed, necking down the trace width to 3.5 mils and spacing to 4 mils (3 track routing) is allowed for a maximum length of 100 mils.
7. Avoid routing DQ/ECC/DQS signals from different bytes and/or different channels in the same track between pins in the DIMM pin field region. Channel-to-Channel and Bytelane-to-Bytelane spacing does not need to be met in the DIMM pin field region.
8. Keep nominal spacing wherever possible. Restrict DIMM pin field routing to 1-track only where possible. Limit the length where a DQS pair splits around a DIMM pin to no more than 1 pin.

4.4.2 DDR4 Command and Address Signals

The processor Address/Command signals are source-clocked output signals that include MA[13:00], BG[1:0], BA[1:0], MA_16_RAS_N, MA_15_CAS_N, MA_14_WE_N, PAR, and ACT_N.

The Address/Command signals are "clocked" into the DIMMs using the positive edge of the differential clock signals. The processor drives the Address/Command and clock signals together.

These signals need to be routed with power referencing as they are power referenced on the processor and on the DIMMs. VDDQ power island needs to be cut into the ground plane between the processor and the DIMMs to allow continuous power referencing for these signals.

Figure 4-16 and Table 4-12 below show the recommended point-to-point topology and routing guidelines for these signals.

Figure 4-16. DDR4 Command and Address Signal Diagram, 1SPC

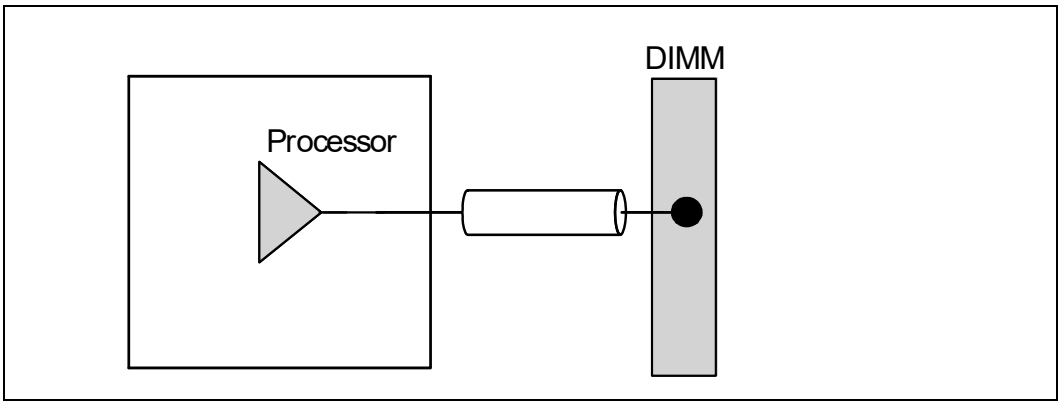


Table 4-12. DDR4 Command and Address Routing Guidelines

Parameter	Guideline	Figure
Signal Group	MA[13:00], BA[1:0], BG[1:0], MA_16_RAS_N, MA_15_CAS_N, MA_14_WE_N, PAR, ACT_N	
Topology	Point-to-point	Figure 4-16
Reference Plane	VDDQ Referenced	Figure 2-1
Layer Assignment [1]	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
Characteristic Trace Impedance (Z_0)	40 Ω ± 15% (Microstrip) 40 Ω ± 10% (Stripline)	
Nominal Trace Width (stack-up dependent)	6.5 mils (Microstrip) 6.13 mils (Stripline)	
Nominal Trace Spacing in Open Field (between Processor and Closest DIMM Slot) [2]	5.4*h* mils Microstrip 4.3*h* mils Stripline	
CMD to DQ Nominal Trace Spacing in Open Field [2]	≥ 10*h* Microstrip ≥ 8*h* Stripline	
Nominal Trace Spacing in DIMM Pin Field [2]	7 mils/47 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace width to 4 mils and spacing to 4 mils (3 track routing) is allowed for a max accumulated length of 0.1”.	
Trace Length - die-to-DIMM with package length	RDIMM/UDIMM Min = 1.2” (Microstrip) Max = 3.85” (Microstrip) Min = 1.5” (Stripline) Max = 4.8” (Stripline) SODIMM Min = 1.0” (Microstrip) Max = 3.35” (Microstrip) Min = 1.4” (Stripline) Max = 4.6” (Stripline)	Figure 4-16
CMD/ADD to CLK, with package length	All CMD signals need to match to all CLK signals within 1”.	
Length Tuning Requirement within DLL groups with package length	Within a DLL group (defined in Table 4-3), CMD signals need to match to each other within 25 mils. No length matching across CMD DLL groups.	Figure 4-16
Processor Breakout Requirements	3.5-mil width/4-mil spacing with 2 track routing (track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. Total breakout routing cannot exceed 1” for stripline and 700 mils for microstrip. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Accordingly, avoid serpentine routing in this region.	

Notes:
1. Signals within a group must be routed on the same layer. Refer to Table 4-3 for definition pf data groups and associated strobes.
2. Keep nominal spacing wherever possible. Minimize reduced spacing in the DIMM field.

4.4.3 DDR4 Control Signals

The processor provides four chip select (CS_N) signals, four ODT signals, and four CKE signals, of which CS_N[1:0], ODT[1:0], and CKE[1:0] are used for 1 DIMM slot per channel designs.

These signals need to be routed with power referencing as they are power referenced on the processor and on the DIMMs. VDDQ power island needs to be cut into the ground plane between the processor and the DIMMs to allow continuous power referencing for these signals.

All of these signals are routed point-to-point for the two DIMM slot per channel topology.

Figure 4-17 and Table 4-13 below show the topology and layout routing guidelines for the control signals that are point-to-point to the DIMM.

Figure 4-17. DDR4 Control Signal Diagram

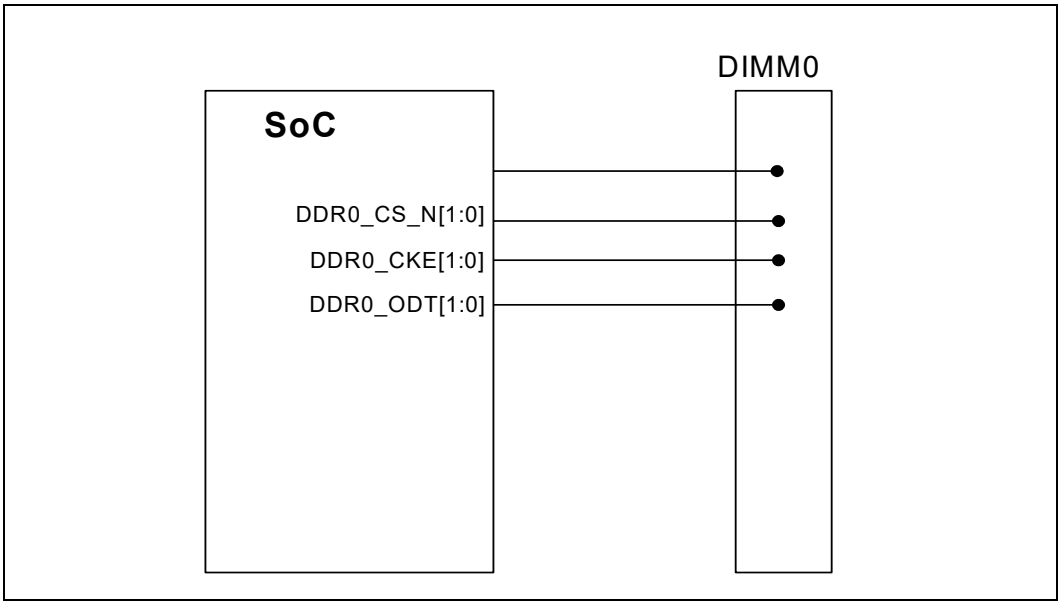


Table 4-13. DDR4 Point-to-Point Control Signal Routing Guidelines

Parameter	Guidelines	Figure
Signal Group	CS_N[1:0], ODT[1:0], CKE[1:0]	
Topology	Point-to-point	Figure 4-17
Reference Plane	VDDQ Referenced	Figure 2-1
Layer Assignment [1]	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
Characteristic Trace Impedance (Zo)	40 Ω ± 15% Microstrip 40 Ω ± 10% Stripline	
Nominal Trace Width (stack-up dependent)	6.5 mils Microstrip 6.13 mils Stripline	
Nominal Trace Spacing in Open Field (between Processor and Closest DIMM Slot) [2]	5.4*h* mils Microstrip 4.3*h* mils Stripline	
CTL to DQ Nominal Trace Spacing in Open Field [2]	≥ 10*h* Microstrip ≥ 8*h* Stripline	
Nominal Trace Spacing in DIMM Pin Field [2]	7 mils/47 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace width to 4 mils and spacing to 4 mils (3 track routing) is allowed for a max accumulated length of 0.1”.	
Trace Length - die-to-DIMM (Figure 4-17) Pin with package length	RDIMM/UDIMM/SODIMM • Min = 1.0” (Microstrip) • Max = 3.66” (Microstrip) • Min = 1.2” (Stripline) • Max = 4.4” (Stripline)	Figure 4-17
Length Tuning Requirement with package length	Within a DLL group (defined in Table 4-3), each CTL signal needs to match to the associated CLK signal within these limits: • RDIMM: within 100 mils • UDIMM: within 25 mils • SODIMM: within 25 mils No length matching is needed across CTL DLL groups. Control signals must be routed on the same layer as associated clock. Package length must be included when matching lengths within a DLL group	Figure 4-17
Processor Breakout Requirements	4-mil width/4-mil spacing with 2 track routing (track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. Total breakout routing cannot exceed 1” for stripline and 550 mils for microstrip. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/ spacing. Accordingly, avoid serpentine routing in this region.	

Notes:
1. Signals within a group must be routed on the same layer. Refer to Table 5-6 for definition pf data groups and associated strobes.
2. Keep nominal spacing wherever possible. Minimize reduced spacing in the DIMM field.

4.4.4 DDR4 Clock Signal Guidelines

The processor provides four differential clock pairs (DDRx_CLK_DP/DN[3:0]). The processor generates and drives these differential clock signals required by the DDR4 interface.

The differential clock pairs must be routed differentially from the processor balls to their associated DIMM pins and must maintain the correct isolation spacing from other signals. When the signals serpentine, it is important to maintain the minimum spacing to other DDR4 signals. While serpentining, the differential clock pair must maintain correct spacing to remain differential as well.

Note: The clock signals need to be routed with power referencing as they are power referenced on the processor and on the DIMMs. A VDDQ power island will need to be cut into the ground plane between the processor and the DIMMs to allow continuous power referencing for the clock signals.

Note: Tabbed routing not needed on these signals

Figure 4-18 and Table 4-14 show the recommended topology and layout routing guidelines for the DDR4 differential clocks that are point-to-point to the DIMM.

Figure 4-18. DDR4 Clock Signal Diagram

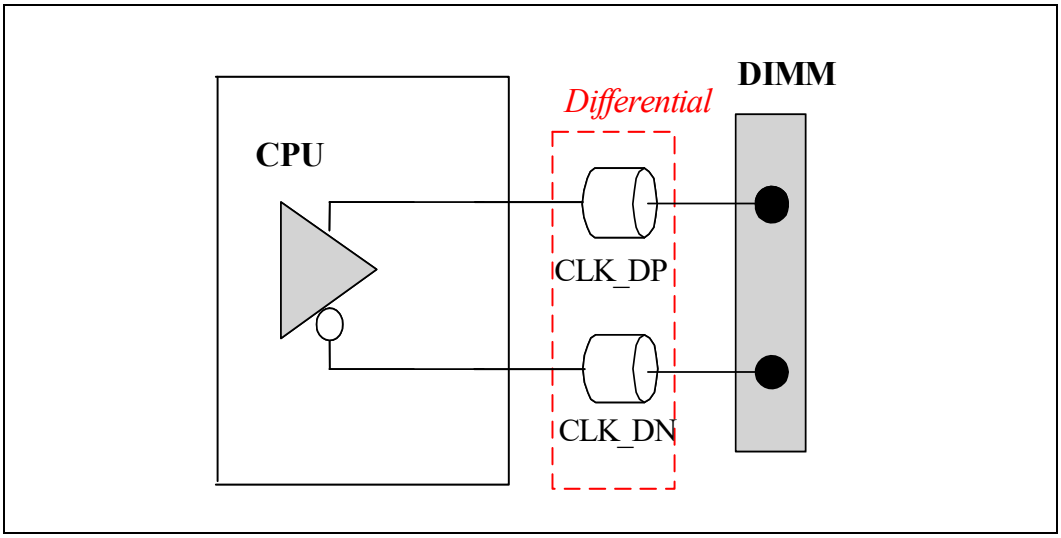


Table 4-14. DDR4 Clock Signal Routing Guidelines

Parameter	Guideline	Figure
Signal Group	CLK_{DP/DN}[0,1]	
Topology	Point-to-point	Figure 4-18
Reference Plane	VDDQ referenced	Figure 2-1
Layer Assignment	Microstrip or Stripline	Figure 2-1
Layer Changes Allowed [1]	Layer change only allowed from Microstrip to Stripline or to other Microstrip layer at CPU pin-field	Figure 2-1
Characteristic Trace Impedance (Zo)	40 Ω ± 15% (Microstrip) 40 Ω ± 10% (Stripline)	
Nominal Trace Width (stack-up dependent)	6.5 mils (Microstrip) 6.13 mils (Stripline)	
Nominal Trace Spacing in Open Field (between Processor and Closest DIMM Slot)	1.33*h* mils (Microstrip) 2*h* mils (Stripline)	
DN to DP Differential Trace Spacing in DIMM Pin Field	5 mils/5 mils (Microstrip/Stripline)	
Group Spacing	13.5 mils/12 mils (Microstrip/Stripline) minimum from any signal	
Trace Length - die-to-DIMM Pin with package length	RDIMM/UDIMM/SODIMM Min = 1.0” (Microstrip) Max = 3.6” (Microstrip) Min = 1.2” (Stripline) Max = 4.4” (Stripline)	Figure 4-18
Processor Breakout Requirements	3.5-mil width/4-mil spacing with 2 track routing (track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. CLK signals within a pair can maintain 4 mils spacing after BGA area. Total breakout routing cannot exceed 1” for stripline and 600 mils for microstrip. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Accordingly, avoid serpentine routing in this region.	
Length Tuning Requirement with package length	Within a CLK pair, the P and the N signals must match to each other within 2 mils.	Figure 4-18
Length Tuning Requirement for clocks to same DIMM with package length	|max(CLK_D{NP}[0]) - min(CLK_D{NP}[2])| ≤ 5 mils	Figure 4-18

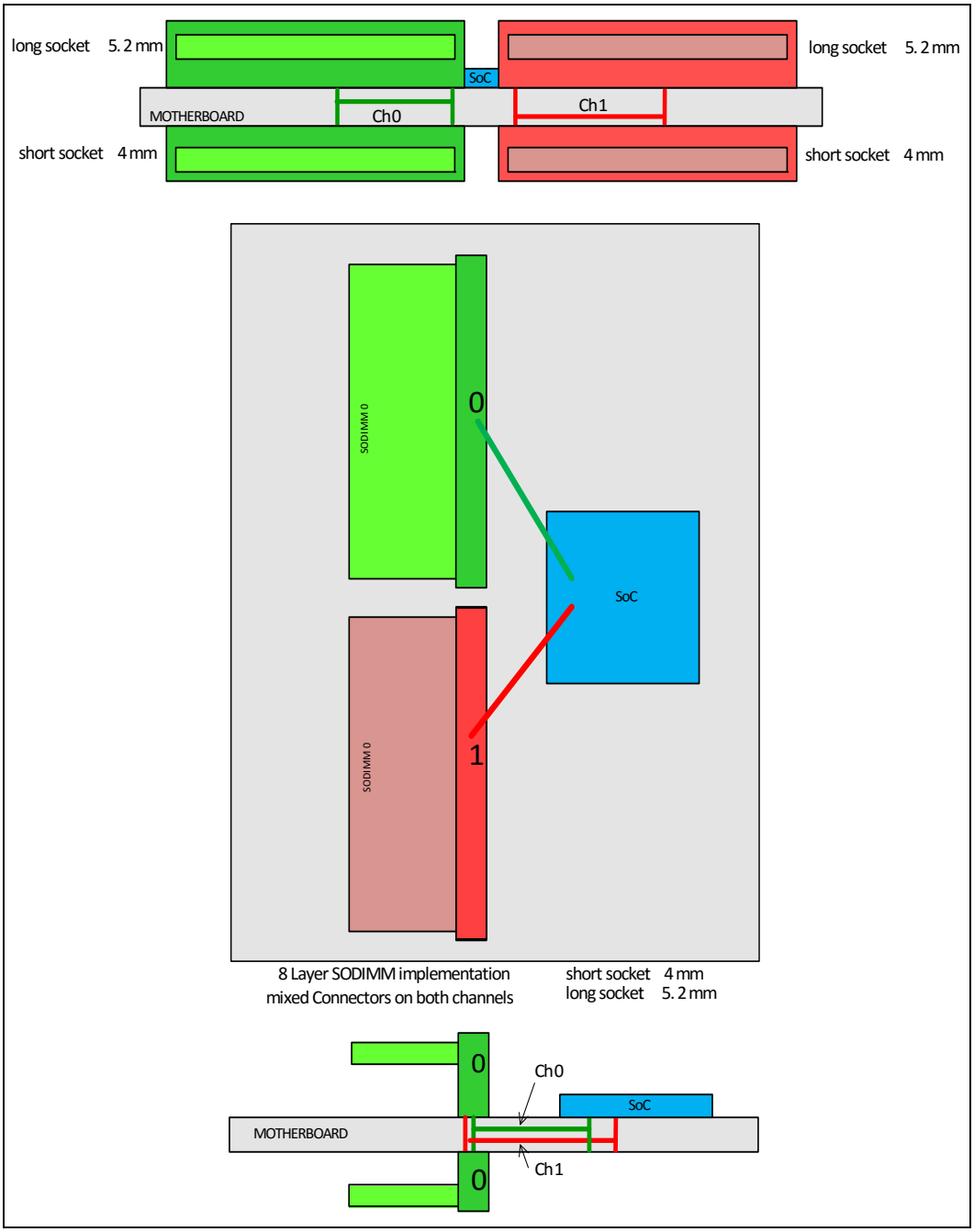
Notes:
1. Board designers using stack-ups other than the reference stack-ups are encouraged NOT to follow differential impedance, but to follow Single Ended impedance guideline and the same differential spacing of 5 mils for microstrip and 4.5 mils for stripline.

Keep nominal spacing wherever possible. Route differentially.

4.4.5 SODIMM Special Design Guide

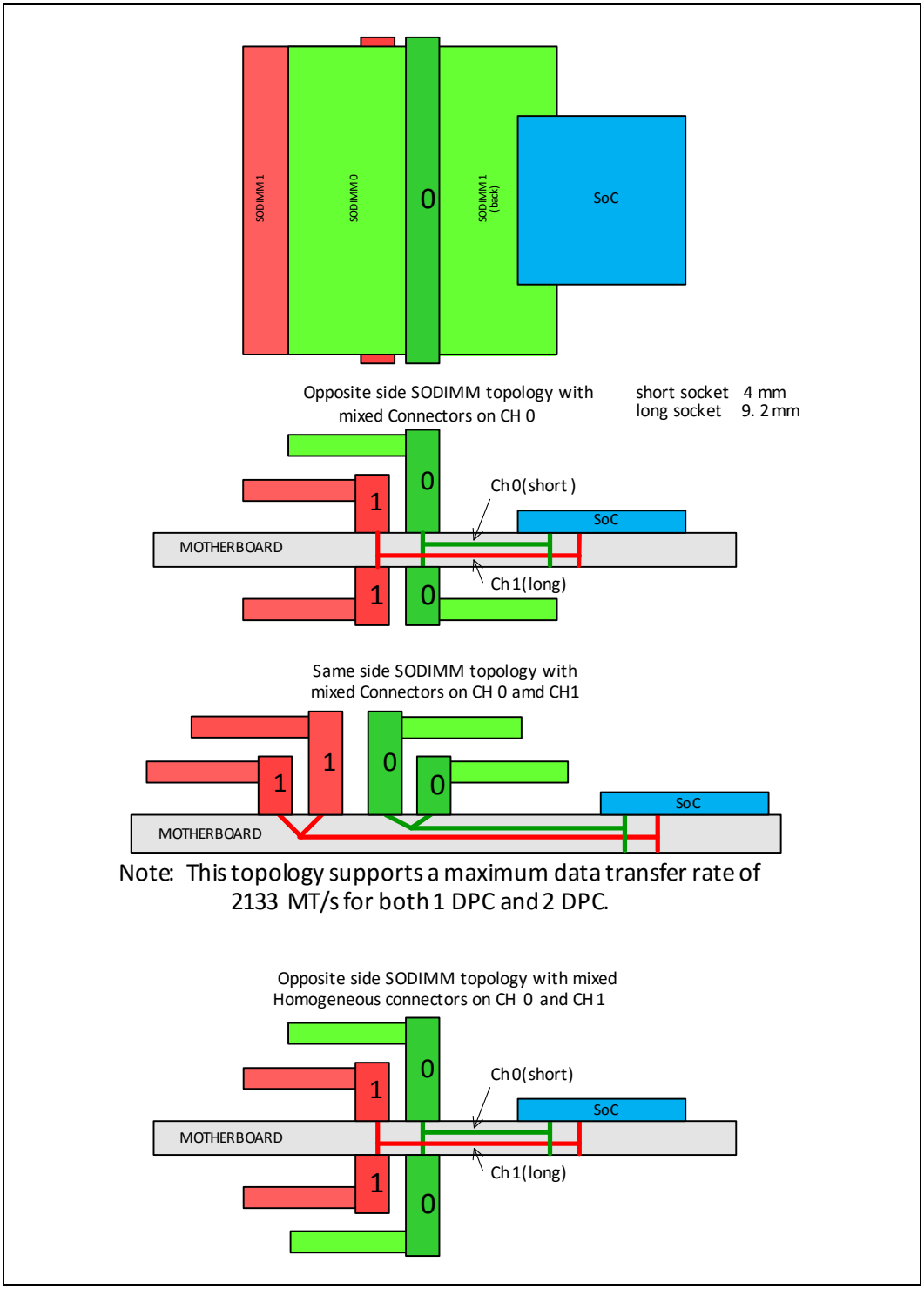
The platform can support two SODIMMs per channel. SODIMM placement is shown in Figure 4-19.

Figure 4-19. SODIMM Layout



A 10 layer board allows the SODIMM back to back configuration and the use of 9.2mm connector. These are not allowed on an 8 layer design.

Figure 4-20. SODIMM Layout

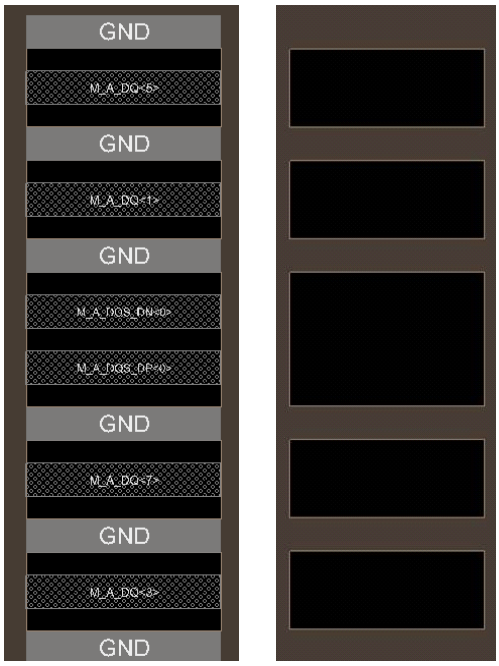


4.4.6 SODIMM Ground Plane Voiding for DQ and DQS

To reach higher speeds, the ground plane should be voided under the DQ (including ECC bits) and DQS pads of the surface mount SODIMM connector as shown in Figure C-9. Detail of the void under a single pad is shown in Figure C-10.

Due to routing congestion, some pads in the near channel may not be voided because the void would prevent a good return path for other signals. The lack of voids is mitigated by the shorter channel length.

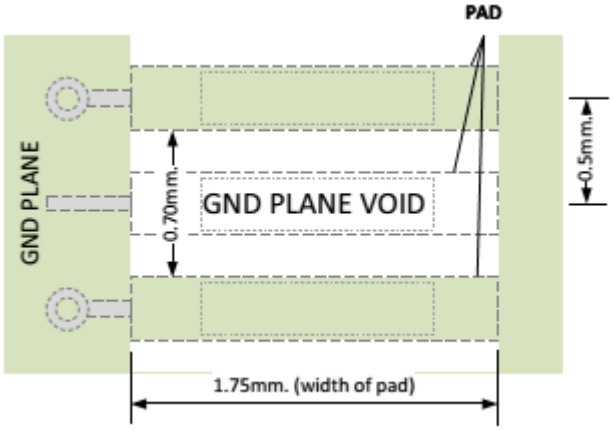
Figure 4-21. SODIMM Ground Plane Voiding



GND voiding underneat the DQ/DQS SODIMM connector pins.
View with PINS

GND voiding underneath the DQ/DQS SODIMM connector pins
View of GND reference plane on top layer

Figure 4-22. SODIMM DQ/DQS Pad Void



4.5 Memory Down Design Guidelines

The DDR4 SDRAM devices can be either x16 or x8 (see Table 4-15). The Dual-Die Package (DDP) or x4 organized SDRAM devices are not supported. Each memory down channel will also have a Serial Presence Device (SPD) down on the board. The SPD will be accessible via the SMBus and be programmed with data similar to that used by UDIMM devices. This will ensure that the Memory Reference Code (MRC) configures the memory controller device properly. Table 4-15 presents the supported memory down configurations.

Table 4-15 shows memory down topology and platform configuration support.

Table 4-15. Routing Topology Support Memory Down Configurations

Configuration Index	Memory Down Configurations				
	Data Rate	# of Ranks	SDRAM Organization	# of SDRAM Devices	ECC/Non-ECC
1	2400	1 Rank	x8	9	ECC
2	2400	2 Ranks	x8	18	ECC
3	2400	1 Rank	x16	5	ECC
4	2400	2 Ranks	x16	10	ECC

The memory down devices employ a clamshell layout meaning one rank on the top of the board and the second rank on the bottom side of the board similar to a double-sided UDIMM layout.

4.5.1 DDR4 Design Considerations

4.5.1.1 Length Considerations and Routing Strategy

There are two levels of length constraints placed on each signal group within the interface:

- **Absolute length constraints**
  - The absolute length constraints are provided in the constraint tables for each signal group. These constraints define the length range over which signals meet signal integrity rules. To ensure clock relative AC timing margins, a subset of this solution space is then defined via a set of clock length matching formulas. These two sets of overlapping length constraints then determine the final routing solution space for a particular platform design.
  - Perform a preliminary test route to establish the natural bounds on all signals groups. Once established, the target lengths for each channel clock group can then be defined so that an acceptable solution space is available when length matching formulas are applied.
- **Clock length matching requirements**
  - The clock target minimum length is typically constrained by the control to clock length matching rules.
  - There is no data strobe to clock matching requirement as in past designs.

4.5.1.2 Stack-Up and Layer Utilization

While building the stack-up and layer utilization schemes, care must be taken not to compromise the underlying impedance, velocity, and coupling assumptions used in verifying the signal integrity and timing of the interface. A particular trace width and spacing (provided) must meet the target impedance requirements when implemented on the reference stack-up. Platform designers may have to adjust trace width and/or spacing to meet impedance/crosstalk and loss requirements if a different stack-up is used.

The following guidelines are targeted for platforms that utilize the 6-layer reference stack-up in addendum B.

- All command/address and control signals are routed as stripline except where required to make surface-layer component connections. This minimizes the impact of layer-to-layer PCB variances on timing margins.
- Individual signal groups may be partitioned between routing layers in any manner necessary to facilitate board routing.
- Individual byte lanes must be routed as a group on the same layer or on a single layer pair with matched segment lengths on each layer. This minimizes data to strobe skew.
- Ensure reference plane transition vias are located in close proximity (within 150 mils/3.81 mm) of signal transition vias whenever signals are routed on multiple layers so that the associated return currents can transition between reference planes.

4.5.1.3 Byte Lane Integrity

- Data lane swapping within the same channel is allowed. If swapping is used, DQ signals within a channel must match its associated DQS signal. Moreover, the signal must be properly adjusted to comply with the required length matching requirements.
- Each data byte group can be treated as eight separate and independent byte lanes for routing.
- Byte lanes may be partitioned between any routing layers as required to complete the route.
- Individual byte lanes must be routed as a group on the same layer or on a single layer pair with matched segment lengths on each layer. This minimizes data to strobe skew.

4.5.1.4 Reference Planes

- It is required that all data, data strobe, control, command and clock signal routing layers be referenced to solid GND reference planes unless otherwise specified. These reference planes must be continuous so that return currents can image the signal trace over the entire path. Routing over plane partitions or voids is not allowed. In the case of stripline layers, Intel recommends, unless otherwise specified, that both reference planes be solid GND planes.
- Care should also be taken whenever signals are routed on multiple layers to ensure reference plane transition vias are located in close proximity to the signal transition vias so that the associated return currents can transition between reference planes.
- Intel also recommends not to use internal reference planes for power distribution in the areas adjacent to DDR4 signal routing. In the event of a secondary reference plane being used for power distribution, it is required that the plane should be quiet by design so as to avoid unintended coupling into DDR4 signals. Routing over voids or partitions should be avoided.
- Additionally, Intel recommends to keep DDR4 routing at least 100 mils away and to keep DDR vias at least 300 mils away from the components used in switching regulator circuits and from any other non-DDR related routes and components.

4.5.1.5 Package Length Compensation

All length matching is done from the processor die-pad to SDRAM device pin. This is done to account for, and in some cases, compensate for the package length variance across each signal group. This compensation is referred to as package length compensation and is an integral part of the overall length matching process. Due to the stringent data to strobe length matching requirements within each byte lane, package length compensation is extremely important within individual byte lanes, and it is very important within the pairs of each differential clock.

4.5.1.6 ZQ Resistor Implementation for Memory Down Devices

The processor does not support ZQ calibration with the ZQ resistor shared between two SDRAM devices. Hence, for memory down topology implementation, Intel recommends using a separate ZQ resistor for each SDRAM device. This resistor should be 240 Ω (±1%) and connected between the ZQ signal and GND. For other details on the ZQ signal, see the DDR4 SDRAM Standard JESD79-4A (Section 4.12).

4.5.2 DDR4 Memory Down Guidelines

The design guides in this section comply for x8 and x16 SDRAM memory down topologies. The guidelines are provided for each corresponding signal group: source-synchronous, source clocked, clocks, and miscellaneous. The guideline supports up to two ranks per channel.

4.5.2.1 Length Matching and Length Formulas

All signal groups are length-matched to the DDR clocks signals. The clocks signals themselves are length-tuned to a fixed length across each channel. The amount of minimum to maximum length variance allowed for each group around the clock reference length varies from signal group to signal group, depending on the amount of timing variance that can be tolerated.

A simplified summary of the length matching formulas for each signal group is provided in Table 4-16.

Table 4-16. Length Matching Formulas

Command, Control and Clock Signal Groups	Matching Rules
Control signals from SOC to each SDRAM device	within 30 mils
Command signals within DLL Command Group from SOC to each SDRAM device	within 30 mils
Control Group-to-Clock from SOC to each SDRAM device	+/- 50 mils
DLL Command Group-to-Clock to first SDRAM device	+/- 300 mils
DLL Command Group-to-Clock from SDRAM device to SDRAM device (single rank)	+/- 75 mils
DLL Command Group-to-Clock from SDRAM device to SDRAM device (dual rank only) x16 SDRAMs	(Clock - 100 mils) < Command < Clock
DLL Command Group-to-Clock from SDRAM device to SDRAM device (dual rank only) x8 SDRAMs	(Clock - 150 mils) < Command < (Clock - 100 mils)

4.5.2.2 DDR4 Data, Data Strobe, and ECC Signals

Figure 4-23. Data Group DQ/ECC Signal Topology

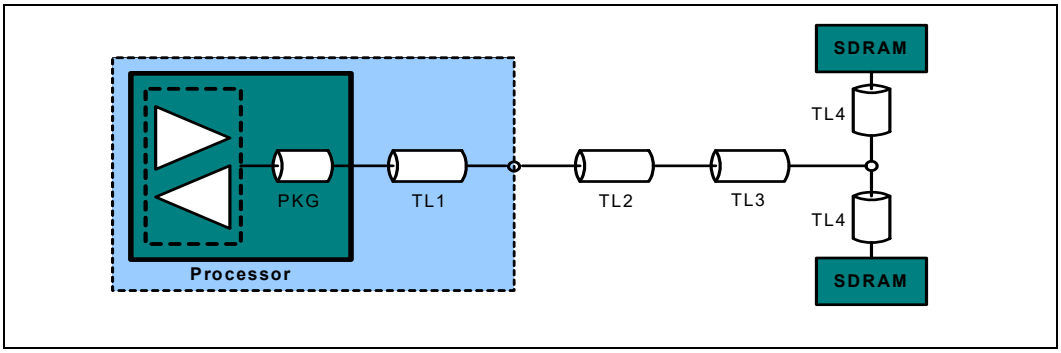


Figure 4-24. Data Group DQS Signal Topology

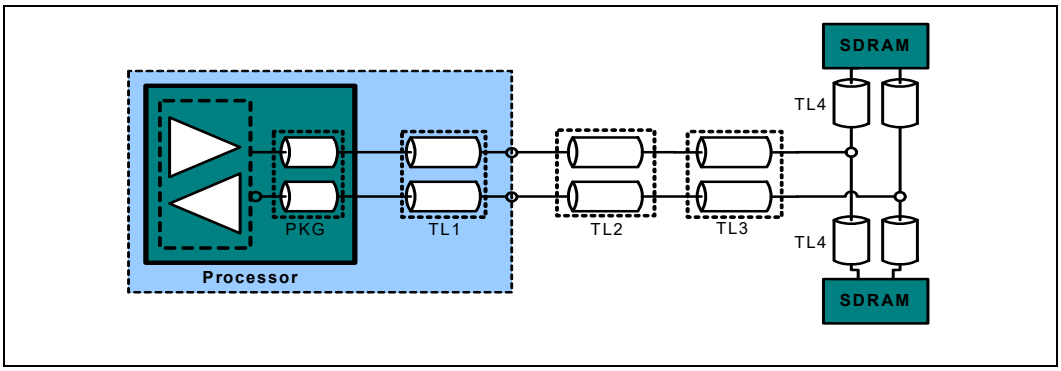


Table 4-17. DDR4 Data, Data Strobe, and ECC Routing Guidelines (Sheet 1 of 2)

Parameter	Guideline	Figure
Signal Group	DQ[63:00], ECC[7:0], DQS_{DP/DN}[17:00]	
Reference Plane	Ground referenced	Figure 4-24
Layer Assignment[1]	Microstrip or stripline (preferred)	Figure 4-24
Layer Changes Allowed	Layer change only allowed from microstrip to stripline or to other microstrip layer at CPU pin field	Figure 4-24
DQ/ECC Characteristic Trace Impedance (Z_o)	50 Ω ± 10% (microstrip) 50 Ω ± 10% (stripline)	
DQS Single Ended Characteristic Trace Impedance (Z_o)[2]	50 Ω ± 10% (microstrip) 50 Ω ± 10% (stripline)	
DQ/ECC Nominal Trace Spacing (intra-byte lane) in Open Field - TL3[1, 3, 4]	≥ 15 mils microstrip ≥ 15 mils stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the inter-byte lane boundaries) - TL3[5]	≥ 30 mils microstrip ≥ 30 mils stripline	
DQ/ECC Nominal Trace Spacing in Open Field (at the ch-to-ch boundaries on the same layer)TL3[5]	≥ 30 mils microstrip ≥ 30 mils stripline	
DQS to DQ Nominal Trace Spacing Open Field - TL3[3,5]	≥ 20 mils microstrip ≥ 20 mils stripline	
DQ/ECC/DQS Trace Length Max., Die to SDRAM Pin Figure 4-24: PKG + TL1 + TL2 + TL3 + TL4	min = 2.24”, max 6”	Figure 4-24

Table 4-17. DDR4 Data, Data Strobe, and ECC Routing Guidelines (Sheet 2 of 2)

Parameter	Guideline	Figure
DQ/ECC/DQS Trace Length Max. for TL4	< 100 mils	
Length Tuning Requirement - DQ/ECC/DQS	+/-10 mils	Figure 4-24
Length Tuning Requirement - DQS P Between N Signals (Figure 4-24)	+/- 5 mils	Figure 4-24
Processor Breakout Requirements - TL1, TL2	The 3.5-mil width/4-mil spacing for 2 track routing the track-to-track minimum spacing is 16 mils within the BGA area. After the BGA area spreads out, use 4-mil width/8-mil spacing or maintain 2 track routing. DQS signals within a pair can maintain 4 mils spacing after the BGA area. Spacing violations in the breakout region must not exceed 0.5 mils. Minimize the length of those violations. Total breakout routing cannot exceed 600 mils for stripline and microstrip. Minimize this length as much as possible. Length matching should not be done in the processor breakout region. Signals should route directly from their pin to the exit of the pin field where they attain the normal width/spacing. Avoid serpentine routing in this region. The maximum breakout length can be violated, if unavoidable, by as much as 50 mils without significant impact to the overall voltage timing margins.	
Dogbone	Max. length = 50 mils	

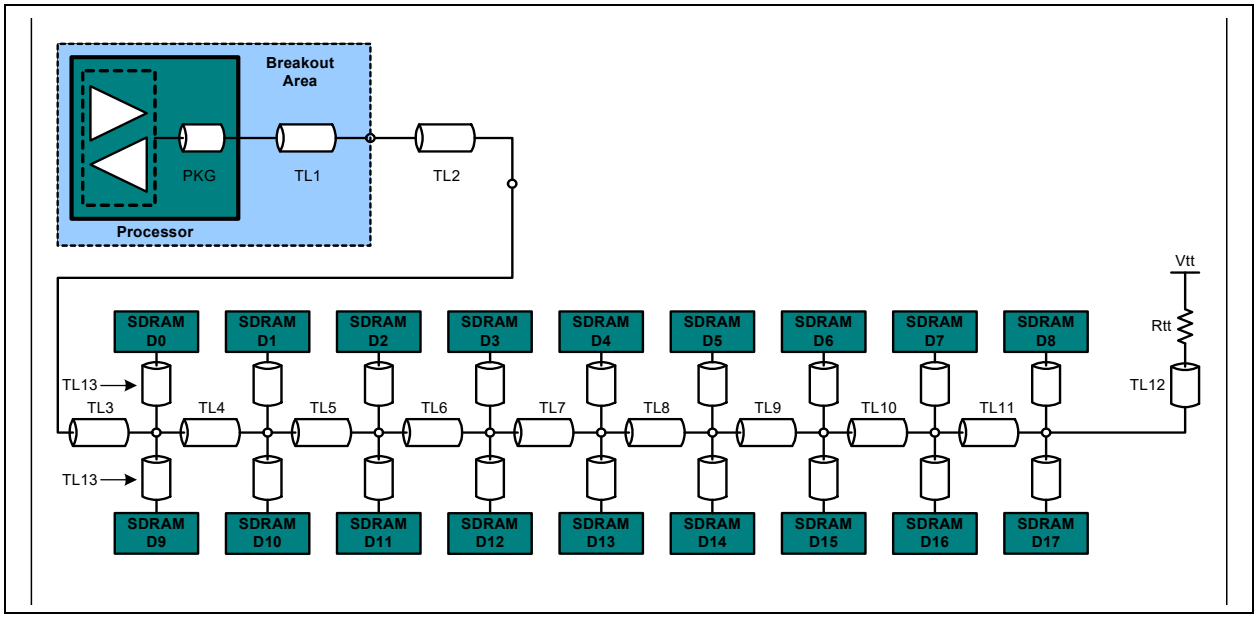
Notes:

1. Signals within a group, including associated strobes, must be routed on the same layer.
2. Board designers using stack-ups other than the reference stack-ups must follow the single ended impedance guidelines for trace width.
3. Open field regions can have reduced nominal spacing for no more than:
   - 100 mils cumulative length when the nominal spacing violation is less than 1h mils (h is the dielectric height from the closest reference plane).
   - 200 mils cumulative length when the nominal spacing violation is less than h/2 (where h is the dielectric height from the closest reference plane).

   For example, if h equals 4 mils:
   - The 4 mil (h) violation of the nominal spacing (13.5 mils) is allowed for a 100-mil length. Spacing can be 13.5-4 = 9.5 mils for up to 100 mils.
   - The 2 mil (h/2) violation of the nominal spacing (13.5 mils) is allowed for a 200-mils length. Spacing can be 13.5-2 = 11.5 mils for up to 200mils
4. This same spacing guideline is applied between DQ/ECC and all other non-DDR signals unless otherwise specified in this document.
5. This same spacing guideline should be applied between DQ/ECC.

4.5.2.3 DDR4 Command and Address Signals

Figure 4-25. Dual Rank Address/Command Group Signal Topology Diagram



4.6 DIMM SPD Addressing Requirements

Intel strongly recommends the DIMM connector SPD addressing match the Customer Reference Board (CRB) implementations shown in Table 4-25. The addressing is defined as below for the DIMMs connected to each processor in the design. The addressing is based upon the channel number and the DIMM number within that channel, so the addressing still applies to designs implementing fewer channels or fewer DIMMs per channel.

The addressing also supports the Temperature Sensing On-Die (DTS) registers.

Note: This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Table 4-18. SODIMM Socket SPD Address Configurations

Channel	DIMM Slot	SPD Address	DTS Address	SA[2:0]
0	DIMM0	0xA0	0x30	000
	DIMM1	0xA2	0x32	001
1	DIMM0	0xA4	0x34	010
	DIMM1	0xA6	0x36	011

4.7 DDR4 Low Speed Signals

The topologies for the Test and Alert signals are described in this section.

4.7.1 Miscellaneous

Routing guidelines for MEM_HOT_N and DDR SPD are in Chapter 14, "SoC Miscellaneous I/O Signals" and Chapter 12, "SMBus 2.0" respectively.

4.7.1.1 DDR01_DRAMRST_N

The SoC provides a single DDR01_DRAMRST_N signal for all DIMMs. The memory controller asserts this active-low signal to the DIMMs to reset the DRAM devices as the system memory voltage plane is ramping or power cycling. This signal must connect to all DIMM RESET# pins.

Figure 4-26. DDR01_DRAMRST_N signal (1SPC and 2SPC) - 10 Layer Daisy chain with T Branch

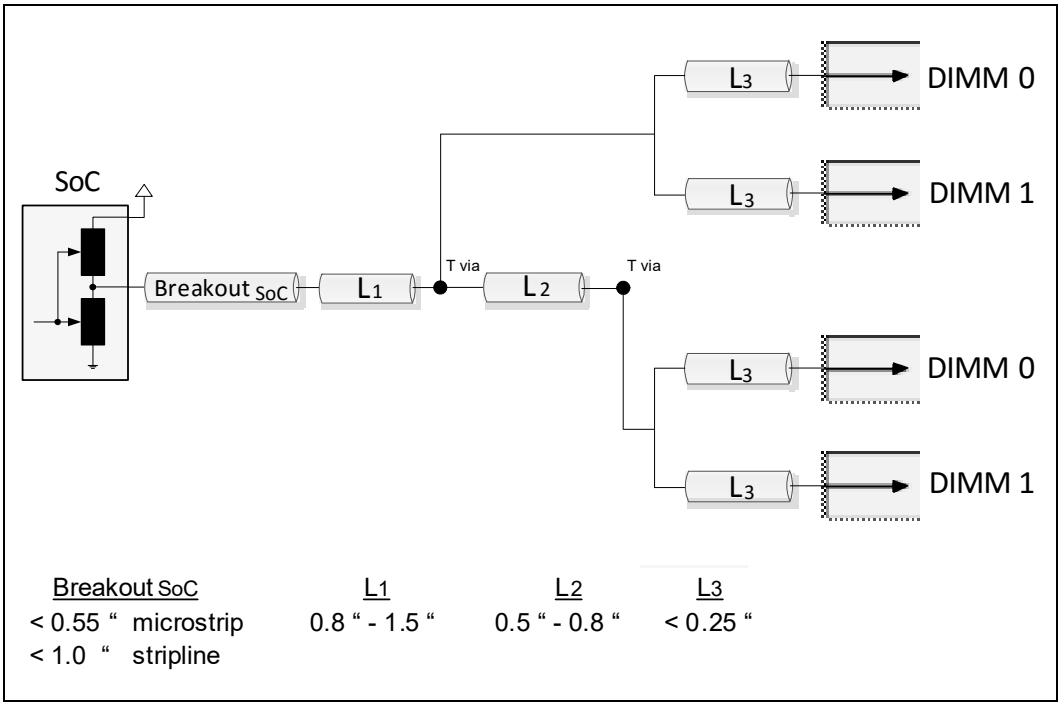


Table 4-19. DDR01_DRAMRST_N Signal Routing Guidelines for 1 or 2 SPC - 10 layer Daisy chain with T branch

Parameter	Guidelines	Figure
Signal Group	DDR01_DRAMRST_N	
Topology	Double T. T connections between channels and T connections at the DIMM components.	Figure 4-33
Reference Plane	Ground Referenced	Figure 4-33
Layer Assignment	Microstrip or Stripline	Figure 4-33
Characteristic Trace Impedance (Z_0)	50 Ω ± 15% (Microstrip) 50 Ω ± 10% (Stripline)	
Nominal Trace spacing in Open Field (between the SoC and the closest DIMM slot)	13.5 mils (Microstrip) 12 mils (Stripline)	
Nominal Trace Spacing in the DIMM	6.9 mils/4.9 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace to 4 mils and spacing to 4 mils (3 track routing) is allowed for a maximum accumulated length of 0.1”.	
Trace Length L1 - SoC Signal Pad to first Tvia	Min = 0.8” Max = 1.5”	Figure 4-33
Trace Length L2 - Tvia to Tvia	Min =0.5” Max = 0.8”	
Trace Length L3 - Secondary Tbranch	Max = 0.25”	
SoC Breakout Requirements	4 mil width/4 mil spacing with 2 track routing (with a track to track minimum of 17 mils) within BGA area. After BGA area maintain a 2 track routing or spread out with 4 mil width/8 mil spacing. Total breakout routing cannot exceed 1” for stripline and 550 mils for microstrip. This length should minimized.	

4.7.1.2 MEM_HOT_N

The MEM_HOT_N, LVCMOS signal is an input to the SoC and initiates action by the SoC to throttle back the memory. It is driven by external logic based on system-defined requirements, typically regarding over-temperature conditions. See Chapter 14, “SoC Miscellaneous I/O Signals”, section 14.1.3.

4.7.1.3 DDR SPD

The SoC provides SMBus signals DDR_SCL and DDR_SDA for interfacing to the DIMM Serial Presence Detect (SPD). These signals connect to all DIMMs.

See Chapter 11, “System Management Bus Interfaces.” SMBus legacy signals (SMB_LEG_DATA, SMB_LEG_CLK, and SMB_LEG_ALERT_N) are used for the DIMM components.

4.7.2 DDR4 Alert signals: DDR0_ALERT_N_PAR_ERR_N and DDR1_ALERT_N_PAR_ERR_N

The DDR4 interface includes an active-low, asynchronous alert input to the processor that is connected to the output from the DIMM. When using any type of DDR4 DIMMs an address parity output is driven from the processor at the same time as the address signals. The register and/or DRAMs on the receiving DIMM will compare the parity of the received address to the received parity bit. If a difference is found, the DIMM will assert the DDRx_ALERT_N_PAR_ERR_N signal to alert the processor to a corrupted address. There is one alert signal per channel. Figure 4-34 shows an example of a DDR4 Alert topology for 2SPC, with guidelines in Table 4-27. 1SPC uses the L1 length.

Figure 4-27. DDRx_ALERT_N_PAR_ERR_N Signals (2SPC)

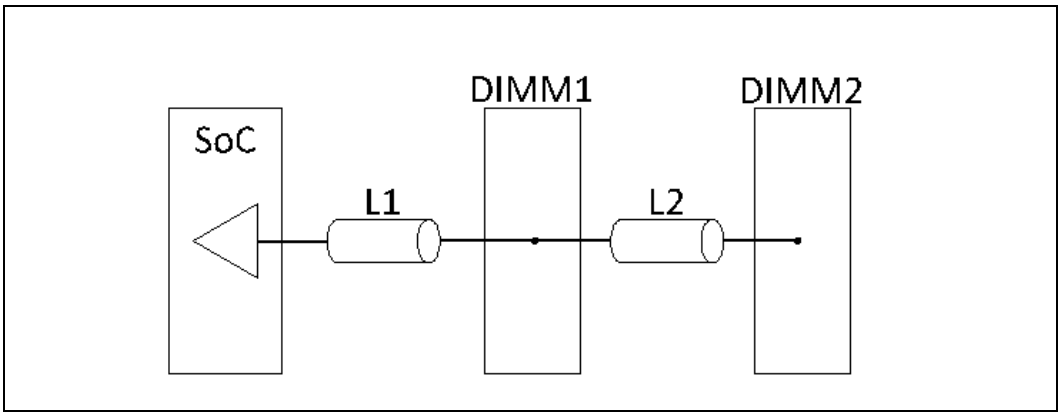


Table 4-20. DDR4 Alert Signal Routing Guidelines for 1 or 2 SPC

Parameter	Guidelines	Figure
Signal Group	DDRx_ALERT_N_PAR_ERR_N	
Topology	Daisy Chain	Figure 4-18
Reference Plane	VDDQ Referenced	Figure 4-18
Layer Assignment	Microstrip or Stripline	Figure 4-18
Characteristic Trace Impedance (Z_0)	40 Ω ± 15% (Microstrip) 38 Ω ± 10% (Stripline)	
Nominal Trace spacing in Open Field (between the SoC and the closest DIMM slot)	13.5 mils (Microstrip) 12 mils (Stripline)	
Nominal Trace Spacing in the DIMM	6.9 mils/4.9 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace to 4 mils and spacing to 4 mils (3 track routing) is allowed for a maximum accumulated length of 0.1”.	
Trace Length L1 - SoC Signal Pad to first DIMM Pin	Min = 1.5” Max = 3”	Figure 4-18
Trace Length L2 - DIMM Pin to DIMM Pin	Min =0.375” Max = 0.525”	
SoC Breakout Requirements	4 mil width/4 mil spacing with 2 track routing (with a track to track minimum of 17 mils) within BGA area. After BGA area maintain a 2 track routing or spread out with 4 mil width/8 mil spacing. Total breakout routing cannot exceed 1” for stripline and 550 mils for microstrip. This length should minimized.	

4.7.3 DDR01_COMP

There is one compensation pin for both DDR memory Channels 0 and 1. The SoC uses the compensation signal to adjust the system memory buffer pull-up and pull-down output impedance characteristics for the channel over temperature, process, and voltage variations.

Figure 4-28. DDR Compensation Resistor for DDR4

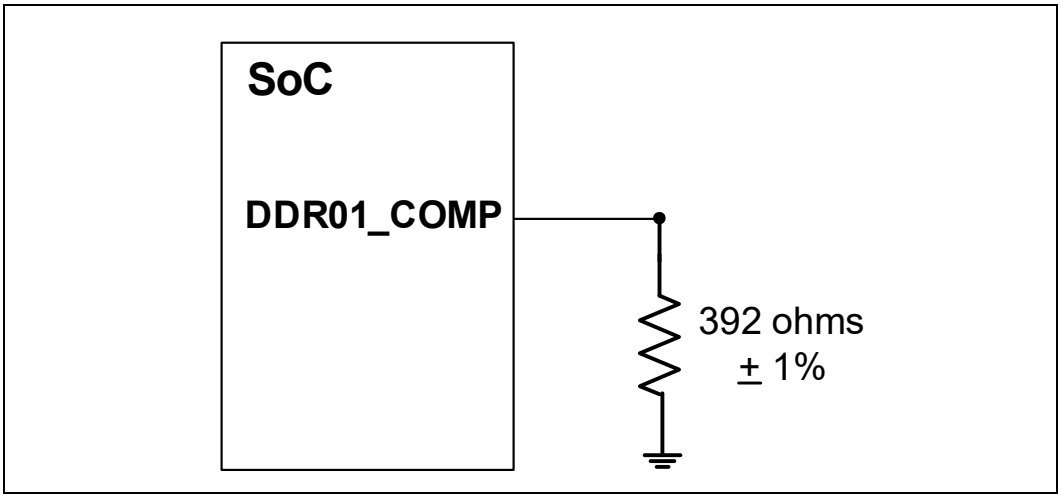


Table 4-21. DDR RCOMP Routing Guidelines

Parameter	Guidelines	Notes
Signal Reference	Ground or Power	
Maximum via Count	2	
Width	5 mils minimum	
Spacing	10 mils minimum	1
Component Distance	The resistor needs to be placed as close to the SoC as possible within 1.0” of the SoC package.	

Note:
1. The spacing can be reduced to 5 mils for the shorter length routing segments. This spacing is a trace-to-trace spacing between the RCOMP[2:0] signal and any other signals.

Table 4-22. Dual Rank DDR4 Command and Address Routing Guidelines

Parameter	Guideline	Figure
Signal Group	MA[13:00], BA[1:0], BG[1:0], MA_16_RAS_N, MA_15_CAS_N, MA_14_WE_N, PAR, ACT_N	
Rtt	36 Ω	
Topology	Point to point	Figure 4-25
Reference Plane	VDDQ or ground referenced	Figure 4-25
Layer Assignment[1]	Stripline	Figure 4-25
Layer Changes Allowed	Layer change only allowed from microstrip to stripline or to other microstrip layer at CPU pin field	Figure 4-25
Characteristic Trace Impedance (Z_0) TL2-TL3 TL4-TL11	 40 Ω ± 10% 55 Ω ± 10%	
Nominal Trace Width (stack-up dependent)	6.8 mils (stripline)	
Nominal Trace Spacing to Other Command, Address and Control signals, Open Field - TL2	≥ 13 mils stripline	
CMD to All Other Signals Nominal Trace Spacing in Open Field[1]	≥ 13 mils stripline	
Nominal Trace Spacing in SDRAM Field	≥ 8 mils stripline	
Total Trace Length - Die-to-DIMM with Package Length PKG + TL1 + TL2 + TL3 + TL4 + TL5 + TL6 + TL6 + TL7 + TL8 +TL9 + TL10 + TL11	Max. = 12 inches	Figure 4-25
PKG+TL1+TL2+TL3	Min. = 3 inches	
Trace Length - SDRAM Device to SDRAM Device TL4, TL5, TL6, TL7, TL9, TL10, TL11	Min. = 450 mils Max. = 500 mils	
Trace Length SDRAM Device 5 to SDRAM 6, TL8 (to allow addition routing channel in SDRAM field)	Min. = 575 mils Max. = 625 mils	
Trace Length - Stub TL13	<120 mils	
Trace Length - TL12	<500 mils	
Length Tuning Requirement Between CMD/ADD to CLK, with Package Length	Die to end of open field (to first SDRAM device) +/-150 mils SDRAM device to SDRAM device -150 mils to -100 mils	
Length Tuning Requirement within DLL Groups with Package Length	Within a DLL group (defined in Table 4-3), CMD signals need to match to each other within 25 mils. No length matching across CMD DLL groups.	Figure 4-25
Processor Breakout Requirements	The 4-mil width/4-mil spacing with 2 track routing (track-to-track minimum of 17 mils) within BGA area. After the BGA area maintains 2 track routing or spreads out with 4-mil width/8-mil spacing, total breakout routing cannot exceed 500 mils. This length should be minimized. Length matching should not be done in the processor breakout region, but the signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Accordingly, avoid serpentine routing in this region.	

Note:
1. Signals within a group must be routed on the same layer. Refer to Table 4-3 for a definition of the CMD/ADD CTL/CLK groups.
2. This table also applies to single rank.

4.7.3.1 DDR4 Control Signals

The processor provides four chip select (CS_N) signals, four ODT signals, and four CKE signals.

Figure 4-29. Control Group Signal Topology Diagram

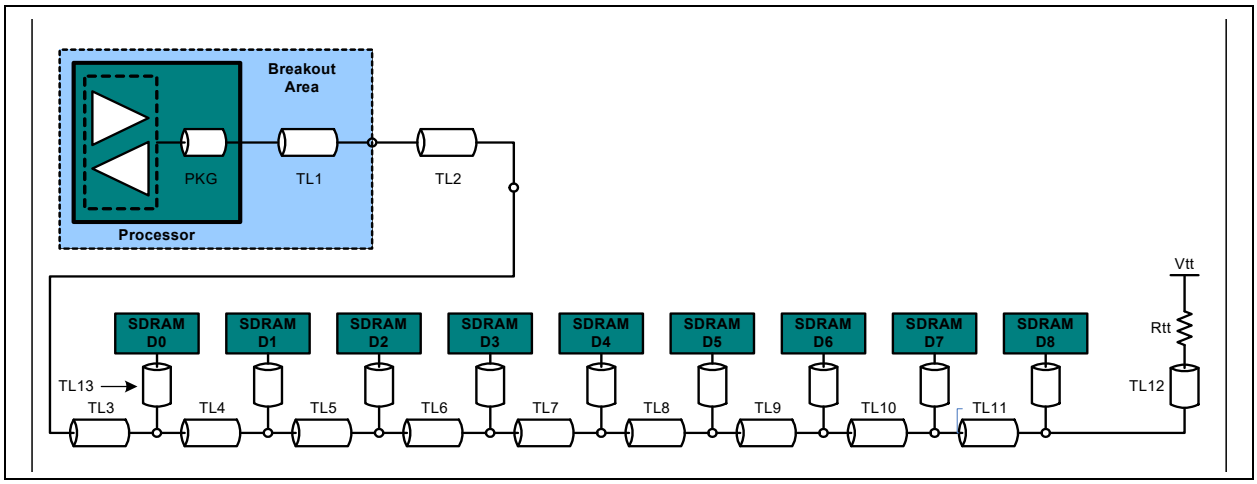


Table 4-23. DDR4 Point-to-Point Control Signal Routing Guidelines

Parameter	Guidelines	Figure
Signal Group	CS_N[1:0], ODT[1:0], CKE[1:0]	
Rtt	36 Ω	
Topology	Point to point	Figure 4-29
Reference Plane	VDDQ or ground referenced	Figure 4-29
Layer Assignment[1]	Stripline	Figure 4-29
Layer Changes Allowed	Layer change only allowed from microstrip to stripline	Figure 4-29
Characteristic Trace Impedance (Z_0) TL2-TL3 TL4-TL11	 40 Ω ± 10% 55 Ω ± 10%	
Nominal Trace Width (stack-up dependent)	Meet target impedance	
Nominal Trace Spacing in Open Field (between processor and first SDRAM device)[1]	≥ 13 mils stripline	
CTL to All Other Signals Nominal Trace Spacing in Open Field[1]	≥ 13 mils stripline	
Nominal Trace Spacing in SDRAM Field[1]	≥ 8 mils stripline	
Total Trace Length - Die-to-SDRAM with Package Length PKG + TL1 + TL2 + TL3 + TL4 + TL5 + TL6 + TL6 + TL7 + TL8 +TL9 + TL10 + TL11 +TL12	Max. = 12 inches	Figure 4-29
PKG+TL1+TL2+TL3	Min. = 3 inches	
Trace Length - SDRAM Device to SDRAM Device TL4, TL5, TL6, TL7, TL9, TL10, TL11	Min. = 450 mils Max. = 500 mils	
Trace Length SDRAM device 5 to SDRAM 6, TL8 (to allow addition routing channel in SDRAM field)	Min. = 575 mils Max. = 625 mils	
Trace Length - Stub TL13	<120 mils	
Trace Length - TL12	<500 mils	
Length Tuning Requirement within Control Signal DLL Group, with Package Length	within 30 mils	Figure 4-29
Processor Breakout Requirements	The 4-mil width/4-mil spacing with 2 track routing (track to track minimum of 17 mils) within BGA area. After BGA area maintain 2 track routing or spread out with 4-mil width/8-mil spacing. Total breakout routing cannot exceed 500 mils. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/spacing. Accordingly, avoid serpentine routing in this region.	

Note:
1. Signals within a group must be routed on the same layer.

4.7.3.2 DDR4 Clock Signals

The clock signal group includes four differential clock pairs. The processor generates and drives one set of the differential clock pair to each rank of the memory down configuration.

Figure 4-30. Clock Signal Topology

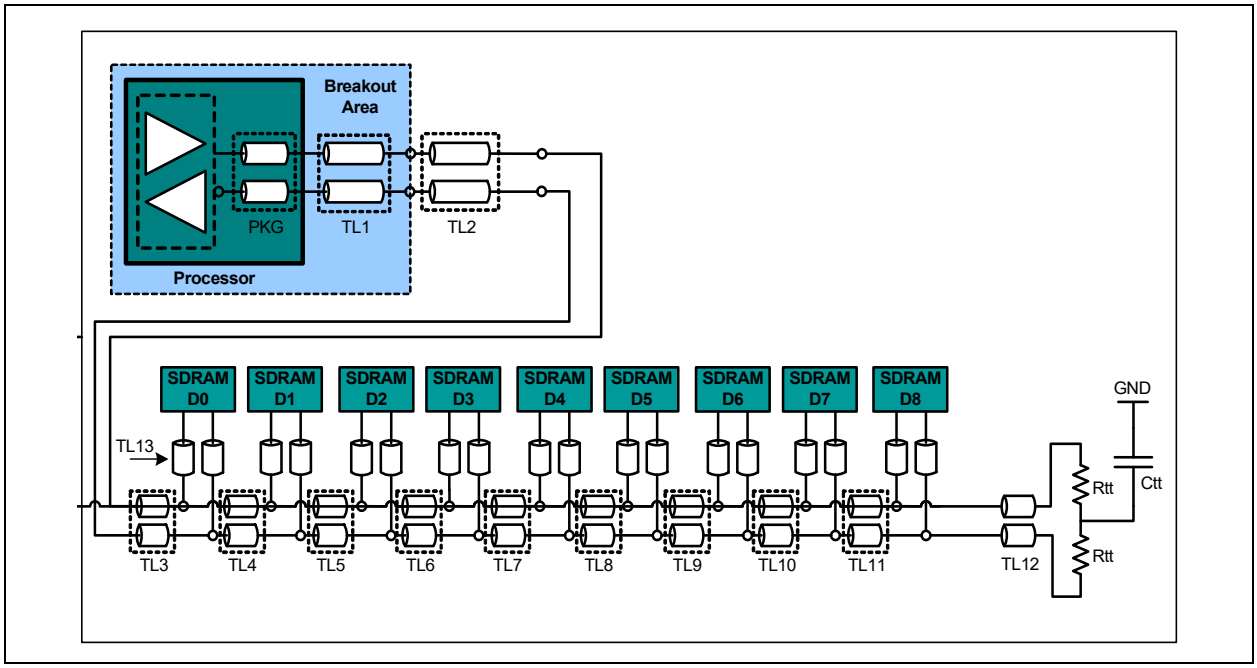


Table 4-24. DDR4 Clock Signal Routing Guidelines

Parameter	Guideline	Figure
Signal Group	CLK_DP/DN[0,1]	
Rtt, Ctt	36 Ω, 0.1 µF	
Topology	Point to point	Figure 4-30
Reference Plane	VDDQ or ground referenced	Figure 4-30
Layer Assignment	Stripline	Figure 4-30
Layer Changes Allowed[1]	Layer change only allowed from microstrip to stripline	Figure 4-30
Characteristic Trace Impedance (Z_0) TL2-TL3 TL4-TL11	 40 Ω ± 10% 55 Ω ± 10%	
Nominal Trace Width (stack-up dependent)	6.8 mils (stripline)	
Nominal Trace Spacing to Other Signals in Open Field, TL2	≥ 13 mils Stripline	
DN to DP Differential Trace Spacing in DIMM Pin Field[1]	5 mils/5 mils stripline	
Group Spacing	13.5 mils/12 mils (microstrip/stripline) minimum from any signal	
Total Trace Length - Die-to-SDRAM with Package Length PKG + TL1 + TL2 + TL3 + TL4 + TL5 + TL6 + TL6 + TL7 + TL8 +TL9 + TL10 + TL11	Max. = 12 inches	Figure 4-30
PKG+TL1+TL2+TL3	Min. = 3 inches	
Trace Length TL12	< 500 mils	
Trace Length Stub TL13	<120 mils	
Processor Breakout Requirements	The 3.5-mil width/4-mil spacing with 2 track routing (track-to-track minimum of 17 mils) within the BGA area. After the BGA area maintains 2 track routing or spread out with 4-mil width/8-mil spacing, the CLK signals within a pair can maintain 4-mils spacing after the BGA area. Total breakout routing cannot exceed 1” for stripline and 600 mils for microstrip. This length should be minimized. Length matching should not be done in the processor breakout region, but signals should route directly from their pin to the exit of the pin field, where they attain the normal width/ spacing. Accordingly, avoid serpentine routing in this region.	
Length Tuning Requirement with Package Length	Within a CLK pair, the P and the N signals must match to each other within 2 mils.	Figure 4-30
Length Tuning Requirement for Clocks to same DIMM with Package Length	|max(CLK_D{NP}[0]) - min(CLK_D{NP}[2])| ≤ 5 mils	Figure 4-30

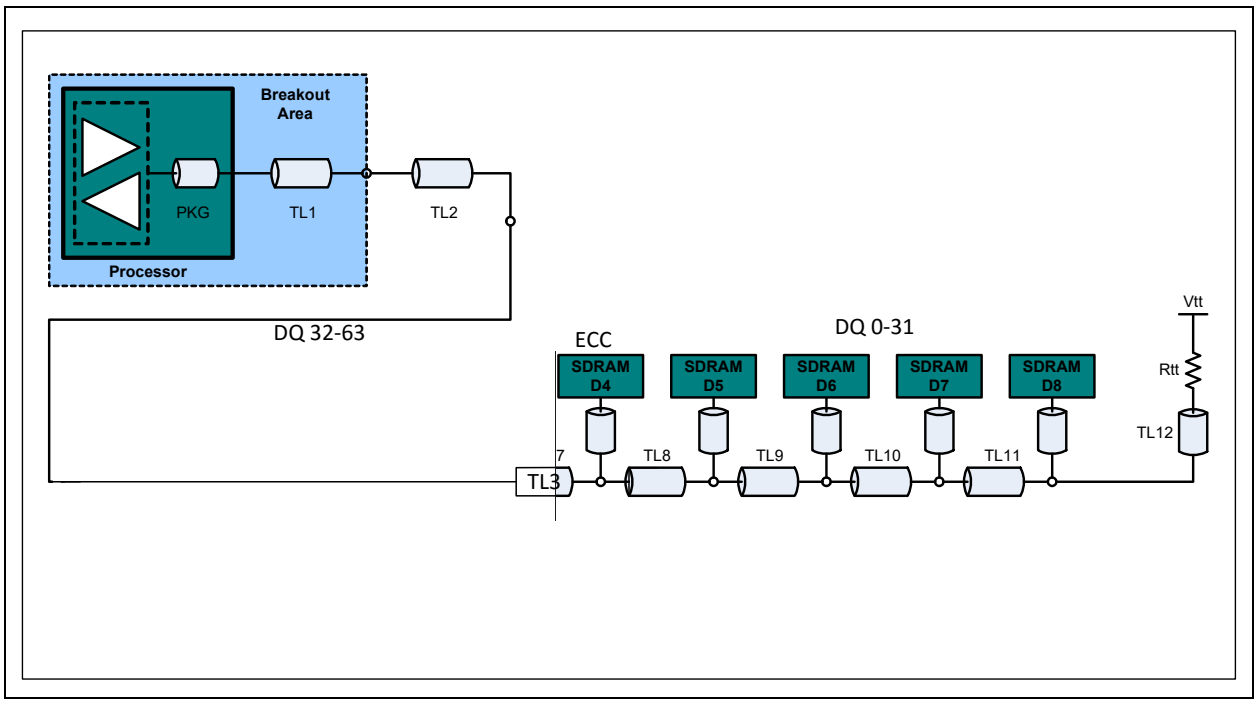
Note:
1. Board designers using stack-ups other than the reference stack-ups are encouraged NOT to follow differential impedance, but to follow the single ended impedance guideline and a differential spacing of 4.5 mils for stripline.

When using x16 SDRAM devices all relative design guide rules are the same as the x8 rules described in this guideline.

4.7.4 32 Bit Memory Down Design Guide

When supporting a platform that is intended to support both 64 bit and 32 bit data buses, the design can follow the same rule set described above (normal 64 bit operation). In 32 bit mode only the lower 32 bits are used, as such the SDRAMs connected to the lower 32 bits must be the SDRAMs closest to the terminating resisters. See Figure 4-31. Also note that the length rule between the last SDRAM and the terminating resisters will also dictate how to layout topology.

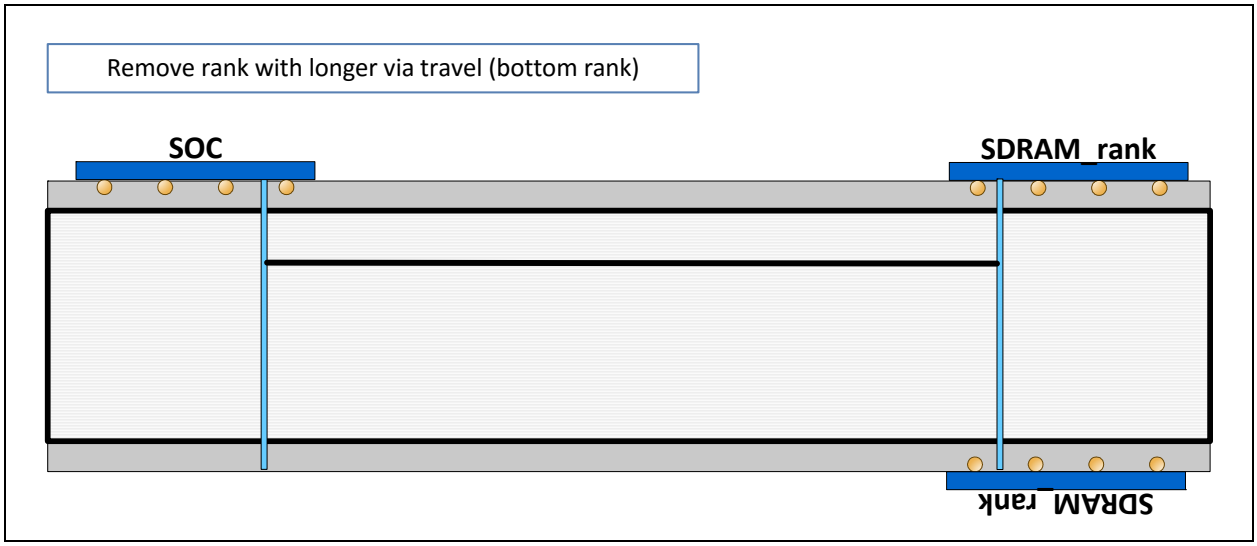
Figure 4-31. Supporting x32 Bit Data Bus



4.7.4.1 Supporting Dual Rank and Single Rank Options

When designing a platform intended to support both dual rank and single rank options follow the stuffing rule outlined in Figure 4-32.

Figure 4-32. Supporting Dual Rank and Single Rank Options



Intel strongly recommends the DIMM connector or memory down SPD addressing match the Customer Reference Board (CRB) implementations shown in Table 4-25. The addressing is defined as below for the DIMMs or Memory Down connected to each processor in the design. The addressing is based upon the channel number and the DIMM number within that channel, so the addressing still applies to designs implementing fewer channels or fewer DIMMs per channel. For memory down, the address is based on channel.

The addressing also supports the Temperature Sensing On-Die (DTS) registers.

Note: This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Table 4-25. R/U/SO DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SPD Address	DTS Address	SA[2:0]
0	DIMM0	0xA0	0x30	000
	DIMM1	0xA2	0x32	001
1	DIMM0	0xA4	0x34	010
	DIMM1	0xA6	0x36	011

Note: Memory down SPD address configurations are same as above table for channel 0 and channel 1.

4.7.5 DDR4 Low Speed Signals Design Guides

4.7.5.1 DDR01_DRAMRST_N

The SoC provides a single DDR01_DRAMRST_N signal for all DIMMs. The memory controller asserts this active-low signal to the DIMMs to reset the DRAM devices as the system memory voltage plane is ramping or power cycling. This signal must connect to all DIMM RESET# pins.

Figure 4-33. DDR01_DRAMRST_N signal Design Topology

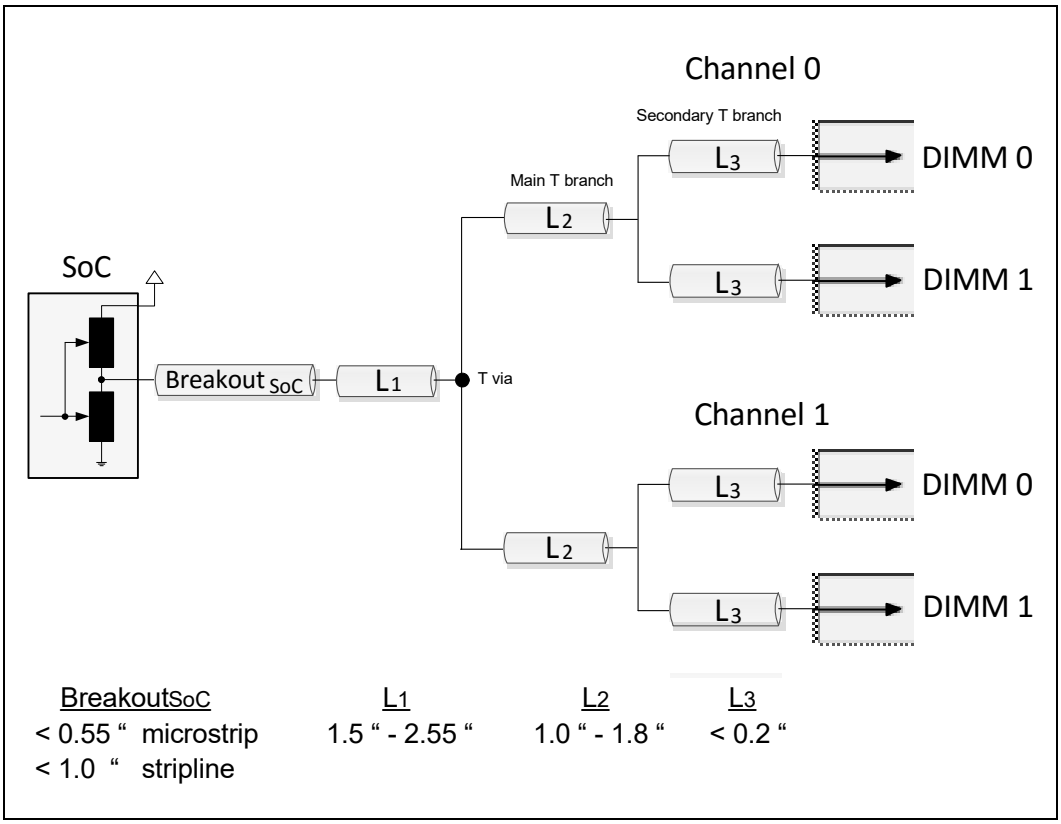


Table 4-26. DDR01_DRAMRST_N Signal Routing Guidelines

Parameter	Guidelines	Figure
Signal Group	DDR01_DRAMRST_N	
Topology	Double T. T connections between channels and T connections at the DIMM components.	Figure 4-33
Reference Plane	Ground Referenced	Figure 4-33
Layer Assignment	Microstrip or Stripline	Figure 4-33
Characteristic Trace Impedance (Z_0)	50 Ω ± 15% (Microstrip) 50 Ω ± 10% (Stripline)	
Nominal Trace spacing in Open Field (between the SoC and the closest DIMM slot)	13.5 mils (Microstrip) 12 mils (Stripline)	
Nominal Trace Spacing in the DIMM	6.9 mils/4.9 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace to 4 mils and spacing to 4 mils (3 track routing) is allowed for a maximum accumulated length of 0.1”.	
Trace Length L1 - SoC Signal Pad to first Tvia	Min = 1.5” Max = 2.55”	Figure 4-33
Trace Length L2 - Main Tbranch	Min =1.0” Max = 1.8”	
Trace Length L3 - Secondary Tbranch	Max = 0.2”	
SoC Breakout Requirements	4 mil width/4 mil spacing with 2 track routing (with a track to track minimum of 17 mils) within BGA area. After BGA area maintain a 2 track routing or spread out with 4 mil width/8 mil spacing. Total breakout routing cannot exceed 1” for stripline and 550 mils for microstrip. This length should minimized.	

4.7.5.2 MEMHOT_N

The MEMHOT_N, LVCMOS signal is an input to the SoC and initiates action by the SoC to throttle back the memory. It is driven by external logic based on system-defined requirements, typically regarding over-temperature conditions. See Chapter 13, “I/O Interfaces”, Section 13.1.4.

4.7.5.3 DDR SPD

The SoC provides SMBus signals DDR_SCL and DDR_SDA for interfacing to the DIMM Serial Presence Detect (SPD). These signals connect to all DIMMs. See Chapter 11, “System Management Bus Interfaces”. SMBus legacy signals (SMB_LEG_DATA, SMB_LEG_CLK, and SMB_LEG_ALERT_N) are used for the DIMM components.

4.7.5.4 DDR4 Alert signals: DDR0_ALERT_N_PAR_ERR_N and DDR1_ALERT_N_PAR_ERR_N

The DDR4 interface includes an active-low, asynchronous alert input to the processor that is connected to the output from the DIMM. When using any type of DDR4 DIMMs an address parity output is driven from the processor at the same time as the address signals. The register and/or DRAMs on the receiving DIMM will compare the parity of the received address to the received parity bit. If a difference is found, the DIMM will assert the DDRx_ALERT_N_PAR_ERR_N signal to alert the processor to a corrupted address. There is one alert signal per channel. Figure 4-34 shows an example of a DDR4 Alert topology with guidelines in Table 4-27.

Figure 4-34. DDRx_ALERT_N_PAR_ERR_N signals - Daisy Chain

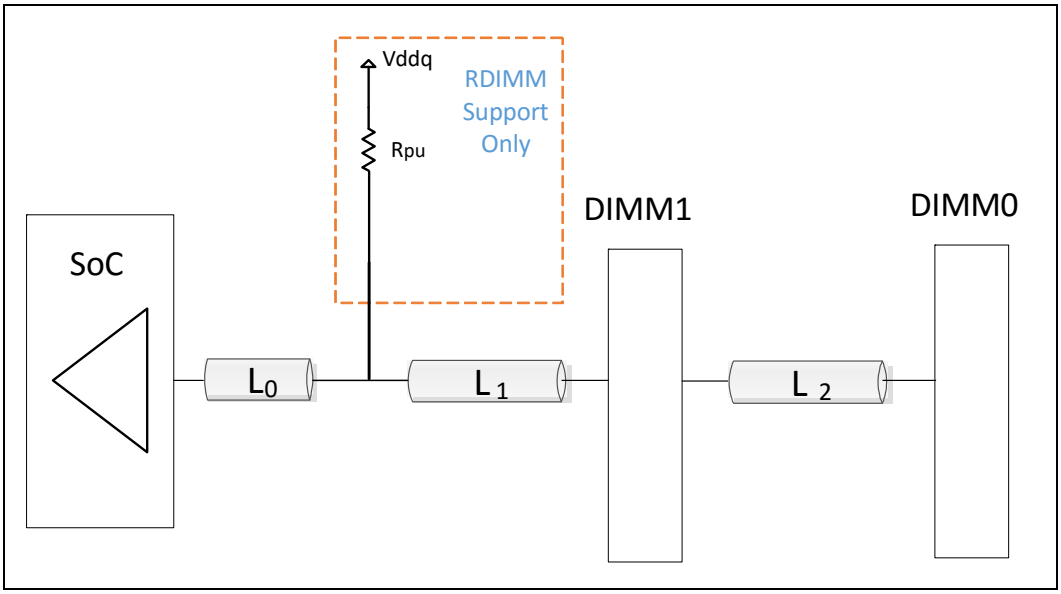


Table 4-27. DDR4 Alert Signal Routing Guidelines

Parameter	Guidelines	Figure
Signal Group	DDRx_ALERT_N_PAR_ERR_N	
Topology	T-topology for SODIMM (max T branch length = 200 mils) Daisy Chain for RDIMM/UDIMM	Figure 4-18
Reference Plane	VDDQ Referenced	Figure 4-18
Layer Assignment	Microstrip or Stripline	Figure 4-18
Characteristic Trace Impedance (Z_0)	40 Ω ± 15% (Microstrip) 38 Ω ± 10% (Stripline)	
Nominal Trace spacing in Open Field (between the SoC and the closest DIMM slot)	13.5 mils (Microstrip) 12 mils (Stripline)	
Nominal Trace Spacing in the DIMM	6.9 mils/4.9 mils (Microstrip/Stripline) (2 track routing) If needed, necking down the trace to 4 mils and spacing to 4 mils (3 track routing) is allowed for a maximum accumulated length of 0.1”.	
Trace Length die-to-DIMM Pin with package length (PKG+L0+L1)	Min = 1.5” Max = 3”	Figure 4-18
Trace Length L2 - DIMM Pin to DIMM Pin (Daisy Chain)	Min = 0.375” Max = 0.525”	
SoC Breakout Requirements	4 mil width/4 mil spacing with 2 track routing (with a track to track minimum of 17 mils) within BGA area. After BGA area maintain a 2 track routing or spread out with 4 mil width/8 mil spacing. Maximum Length of the L0 segment before insertion of the pull-up resistor is 550 mils for both stripline and microstrip. This length should be minimized.	
R_{pu} (RDIMM Support Only)	40 Ω ± 1% tied to VDDQ. Minimize the segments connecting the pull-up resistor to the signal trace and VDDQ.	

4.7.5.5 DDR01_COMP

There is one compensation pin for both DDR memory Channels 0 and 1. The SoC uses the compensation signal to adjust the system memory buffer pull-up and pull-down output impedance characteristics for the channel over temperature, process, and voltage variations.

Figure 4-35. DDR Compensation Resistor for DDR4

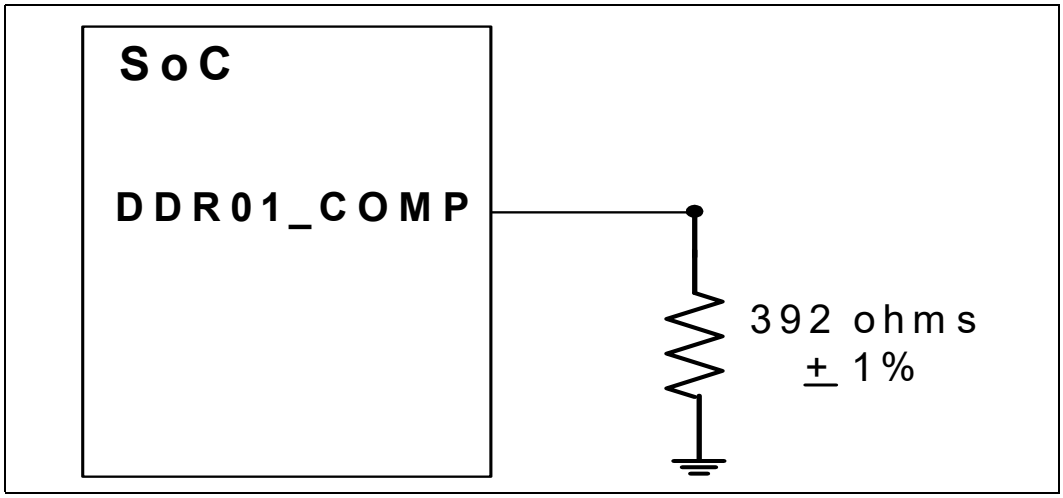


Table 4-28. DDR RCOMP Routing Guidelines

Parameter	Guidelines	Notes
Signal Reference	Ground or Power	
Maximum via Count	2	
Width	5 mils minimum	
Spacing	10 mils minimum	1
Component Distance	The resistor needs to be placed as close to the SoC as possible within 1.0” of the SoC package.	

Note:
1. The spacing can be reduced to 5 mils for the shorter length routing segments. This spacing is a trace-to-trace spacing between the RCOMP[2:0] signal and any other signals.

4.7.5.6 VREFCA

The DDR4 system memory reference voltage is used by the DIMMs to compare the input data signal levels. Each DDR4 DIMM has one voltage reference input, VREFCA. VREFCA is used by all the command, address, and control signals.

Figure 4-36. DDR4 VREFCA Daisy Chain, Single Channel Configuration

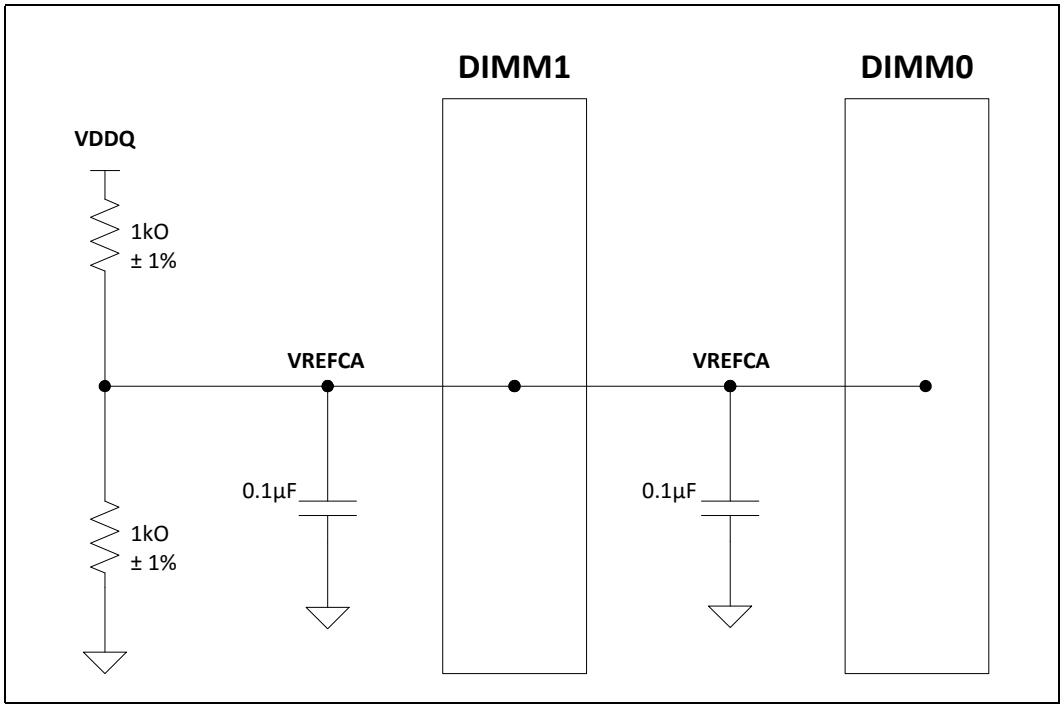


Table 4-29. DDR4 VREFCA Routing Guidelines

Parameter	Guidelines
Signal Reference	Ground or Power
Maximum via Count	2
Width	4 mils minimum
Spacing	10 mils minimum
Voltage Divider Resistor Value	1 kΩ ± 1%
Decoupling Capacitor at each DIMM	0.1 uF

§ §

5 PCI Express*

The PCIe* bus in Table 5-2 are a subset of the HSIO 20 lanes (SKU dependent) available for PCIe* Gen3, SATA, and USB 3.0. The description about how the bus in Table 5-2 is associated with the 20 HSIO Lanes and how to configure the HSIO are in Chapter 10, "Flexible I/O Adapter (FIA) Overview" of the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4.*

Table 5-1. Signal Names and Descriptions

Signal Names	Direction	Shared	Description
PCI Express RP Cluster 0 - SoC Root Ports 0, 1, 2, and 3			
PCIE0_RP0_RP3_TX_DP[7:0] PCIE0_RP0_RP3_TX_DN[7:0]	O, Differential	n/a	**Transmit (Tx):** These differential output signals are internal to the SoC. The actual signal pins are determined by the FIA configuration.
PCIE0_RP0_RP3_RX_DP[7:0] PCIE0_RP0_RP3_RX_DN[7:0]	I, Differential	n/a	**Receive (Rx):** These differential input signals are internal to the SoC. The actual signal pins are determined by the FIA configuration.
PCIE_CLKREQ_N[3:0]	I,O-OD	Yes	**Reference Clock Control:** These active-low signals are used for reference clock control. See CLKREQ# signal in the PCIe Mini CEM specification.
PCI Express RP Cluster 1 - SoC Root Ports 4, 5, 6, and 7			
PCIE1_RP4_RP7_TX_DP[7:0] PCIE1_RP4_RP7_TX_DN[7:0]	O, Differential	n/a	**Transmit (Tx):** These differential output signals are internal to the SoC. The actual signal pins are determined by the FIA configuration.
PCIE1_RP4_RP7_RX_DP[7:0] PCIE1_RP4_RP7_RX_DN[7:0]	I, Differential	n/a	**Receive (Rx):** These differential input signals are internal to the SoC. The actual signal pins are determined by the FIA configuration.
PCIE_CLKREQ_N[7:4]	I,O-OD	Yes	**Reference Clock Control:** These active-low signals are used for reference clock control. See CLKREQ# signal in the PCIe Mini CEM specification.
Common to All Root Ports			
CLK_OUT_DP[4:0] CLK_OUT_DN[4:0]	O, Differential	No	**Differential Reference Clock:** These differential output signals can be used to provide a PCIe interface clock to external PCIe devices. These five sets of output signals enable the platform board design to have five PCIe devices without requiring a clock-buffer component. ***Note:*** While there are eight PCIE_CLKREQ_N signal pins, there are only five Differential Reference Clock pins provided. Clock buffering may be needed on some platform board designs.

5.1 PCIe* Layout General Design Guidelines

This section gives routing guidelines that are specific to PCIe*. See Chapter 2, "Platform Stack-up and General Design Considerations" for additional guidelines that apply to PCIe and other buses.

Table 5-2. PCI Express* Base Specification Compliance 3.0

Guideline	Follow the routing guidelines in the PCI Express Base Specification, Revision 3.0
Applicable buses	PCIe
Purpose	Maintain compatibility with the Base Spec.
Significance	High

Table 5-3. Via Stub Length

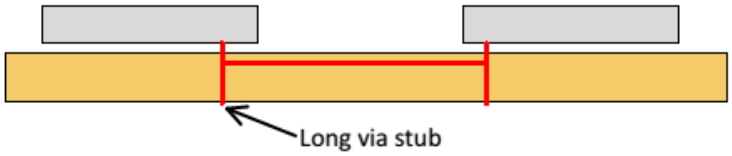
Guideline	Via stubs have a negative impact on link performance. Minimize via stub length, especially for high risk (long) links. Refer to specific topologies for maximum allowable via stub.
Purpose	To improve link performance by minimizing via stub length. Via stub introduces discontinuity (due to its capacitive nature) and can have significant detrimental impact on link performance
Significance	High. See guideline for impact at particular via length.
Implementation	Simulation showed that via stub length is more important in terms of eye measurements than number of vias and via length. Therefore, avoid routing longest (or other high risk) link on top layers that may cause long via stubs. Try to use a board as thin as possible, this will help to reduce the via stub length. 

Table 5-4 gives general design rules. Topology specific values are denoted by the tags <Via stub>, <Insertion Loss>, <Space>, <Min Length>, and <Max Length>. The values for each of these is shown in a table accompanying each topology.

Table 5-4. General PCIe* Design Rules

Layout Guideline	Breakout	Non-Breakout	Units	Notes
Transfer rate	5 for Gen2 and 8 for Gen3		GT/s	
Interleaved or non-interleaved	Non-Interleaved			1
Reference Plane	Ground Referenced			
Via stub length (max)	<Via stub>		mils	2
Max IL target @ 4 GHz, dry 25C	<Insertion Loss>		dB/inch	3
Differential Trace Impedance	Breakout region	85 ± 17.5% on Microstrip 85 ± 12.0% on Stripline	Ω	4
Spacing across pairs within the same port	4 mils	<Space>	mils	
Spacing to other signals	≥ 4h or separate layers	stripline 5*h*; microstrip 11*h*	mils	5
Spacing across pairs within the same port on riser	N/A	15*h* unless otherwise noted	mils	5
Tx_sig to Rx_via	2	N/A		
Rx_sig to Tx_via	2	N/A		
Min. Trace Length	0	<Min Length>	inch	
Max Trace Length	500 mils	<Max Length>	inch	

Notes:

1. Non-interleaved = TxTxTx or RxRxRx; Interleaved = TxRxTxRx.
2. Via stub is extra length of via from signal layer to bottom of board.
3. Refer to Chapter 2, "High-Speed Signal Trace Insertion Loss" for more details.
4. Refer to Chapter 2, "Platform Stack-up and General Design Considerations" for more details.
5. "*h*" - dielectric height between signal and reference ground plane

5.1.1 PCIe* Test Points and Probing

The inclusion of test points and probing structures has the ability to impact the loss and jitter budgets of a PCIe interconnect. This does not mean they cannot be tolerated, however. In general, test points and probe structures should not introduce stubs on the differential pairs or cause them to wildly deviate from the recommendations given throughout this section. Existing vias, pads or pins should be used wherever possible to accommodate such structures.

5.1.2 Connectors

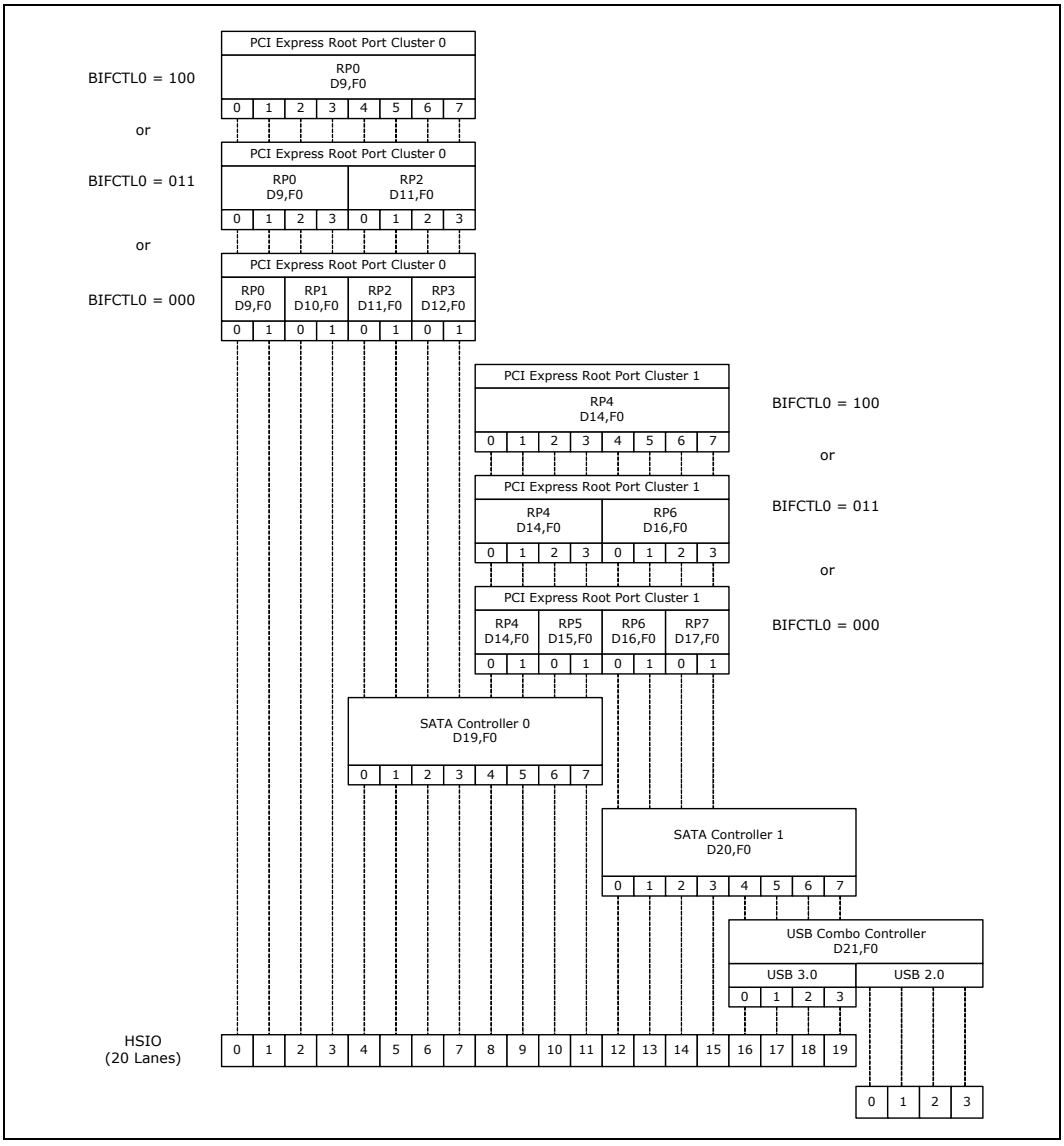
The PCI Express Card Electromechanical Specification Revision 3.0 defines the connector to use in conjunction with edge finger add-in cards. The list of issues below should be taken into account when designing with PCIe* connectors.

- For thru-hole connectors, the pins of a differential pair are offset from each other. This delta of mismatch between the pins should be directly accounted for by the PCB trace on the system board. Refer to the Length Matching section of this section for more details on length matching requirements.
- The two traces of a differential pair should both route into a connector pin field from the same layer.
- Note that the pinout names of the connector are defined with respect to the system board:
  - The transmitter differential pair of the connector shall be connected to the TX differential pair on the system board, and to the RX differential pair on the add-in card.
  - The receiver differential pair of the connector pins shall be connected to the RX differential pair on the system board, and to the TX differential pair on the add-in card.
- The connectors and the add-in cards are keyed such that smaller cards can be placed in larger connectors. A x1 card, for example, can be inserted into the x4 and x8 connectors. This is referred to as up-plugging. No known layout adjustments need to be made in order to accommodate up-plugging.
- Adjacent differential pairs on the connector are separated by two ground pins to manage the connector crosstalk. Ground pins should directly tie to the ground plane on the system board.
- PCIe connectors are designed for use with a PCIe card retention system. PCIe cards greater than 350 grams require additional card retention and support. For more details on PCIe riser card support, refer to the latest PCI Express* 3.0 438-Pin Riser Card Edge Connector Specification.

5.2 SoC Specific PCIe3 Interface Guide

The SoC supports up to sixteen PCI Express* Gen3 lanes that can be configured as up to eight independent PCIe root ports. The interface complies with PCI Express Base Specification Revision 3.0.

Figure 5-1. FIA and HSIO Structure



Note: The structures for PCIe RP bifurcation control BIFCTL0 = 001 and 010 are not shown here but are valid configurations. Most use cases are satisfied by what is shown in the figure.

- RP[3:0] is assigned as device [12:9]
- RP[7:4] is associated with device [17:14]

With BIFCTL0 = 000, PCIe RP[7:2] is MUXed with Flexible I/O SATA and support the power management port/lane staggering feature. The root ports are configurable to support a diverse set of lane assignments. The number of available lanes and Root Ports depends on the SoC SKU definition.

5.2.1 Routing PCIe* through a DIMM Connector

PCIe lanes may be routed orthogonally through up to four DDR4 DIMM connectors when necessary without degradation in PCIe or DDR solution space. PCIe traces shall maintain the same trace width and spacing guidelines for inner and outer layer routing. Reduced trace width or spacing is not required. Signals shall not be routed adjacently to DIMM connector power pins or SMBus pins. This solution is simulated but not validated by Intel.

5.3 Layout Topology Guidelines

Intel simulation results show the platforms which follow the design guides can meet PCI Express Base Specification Revision 3.0 for minimum Tx Vswing and minimum Rx eye height.

The transmit and receive directions of the link have different guidelines due to capacitive decoupling, and there are different guidelines based on whether the signals are routed on a microstrip or a stripline layer. These guidelines are provided for each link topology.

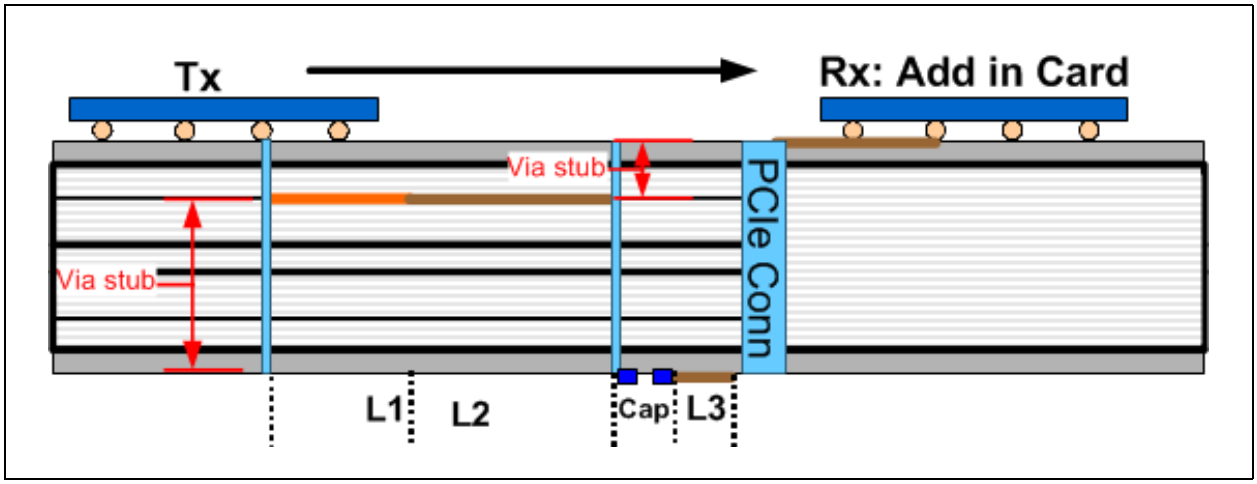
All the transmit and receive topologies are from the point-of-view of the SoC.

5.3.1 One Connector Transmit Guidelines — Internal Breakout

This section gives routing guidelines for one connector transmit with Internal breakout for internal breakout to bottom short and internal breakout to bottom.

Internal Breakout to Bottom Short Routing Guidelines

Figure 5-2. PCIE3 Transmit, One Connector, Breakout to Bottom Short



Notes:
1. L1 is the SoC pin field region. A trace is necessary on Layer 1 traveling from pad to via of 23-mils, but it is not shown in the graphic.
2. As long as the maximum length is not exceeded, the AC coupling cap can be placed anywhere along the L3 route. Simulations show optimal margins when AC coupling cap placed further from the CPU.
3. This topology is simulated and validated by Intel.

Table 5-5. PCIE3 Transmit, One Connector, Breakout to Bottom Short

Layout Guideline	L1	L2	L3	Units	Notes
Via stub (max)	80	80	0	mils	
Spacing across pairs within the same port	Breakout	3*h*	9*h*		
Min. Trace Length	L1+L2+L3 ≥ 3			Inches	
Max Trace Length	1.2	15-L1-L3	0.5	Inches	
Layer Assignment	Stripline		Bottom Microstrip		

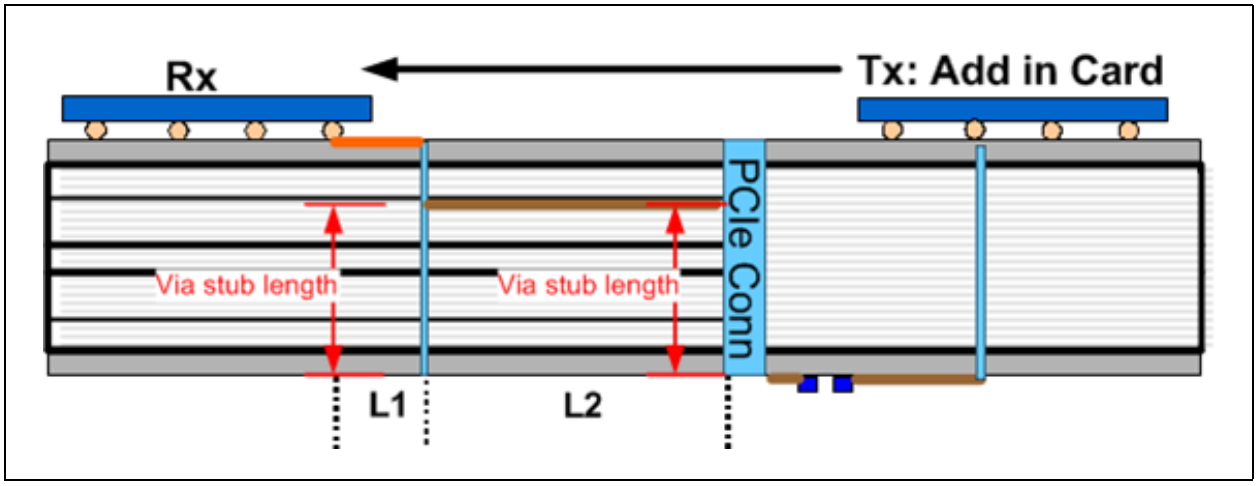
Note:
1. The maximum PCB loss on this topology for baseboard is 11.25dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers may be calculated by LossEnabler=11.25dB/ TargetLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets may be different for stripline and microstrip layers, as long as the total loss target is satisfied.

5.3.2 One Connector Receive Routing Guidelines — External Breakout

This section gives routing guidelines for one connector receive with external breakout for top breakout to same, bottom breakout to same and microstrip breakout to stripline.

Microstrip Breakout to Stripline Routing Guidelines

Figure 5-3. PCIE3 Receive, One Connector, Stripline to Microstrip Breakin



Note:
1. This topology is simulated and validated by Intel.

Table 5-6. PCIE3 Receive, One Connector, Microstrip Breakout to Stripline

Layout Guideline	L1	L2	Units	Notes
Via stub (max)	80	80	mils	
Spacing across pairs within the same port	9*h*	3*h*		
Min. Trace Length	L1+L2 ≥ 3		Inches	
Max Trace Length	1.2	15-L1	Inches	
Layer Assignment	Microstrip	Stripline		

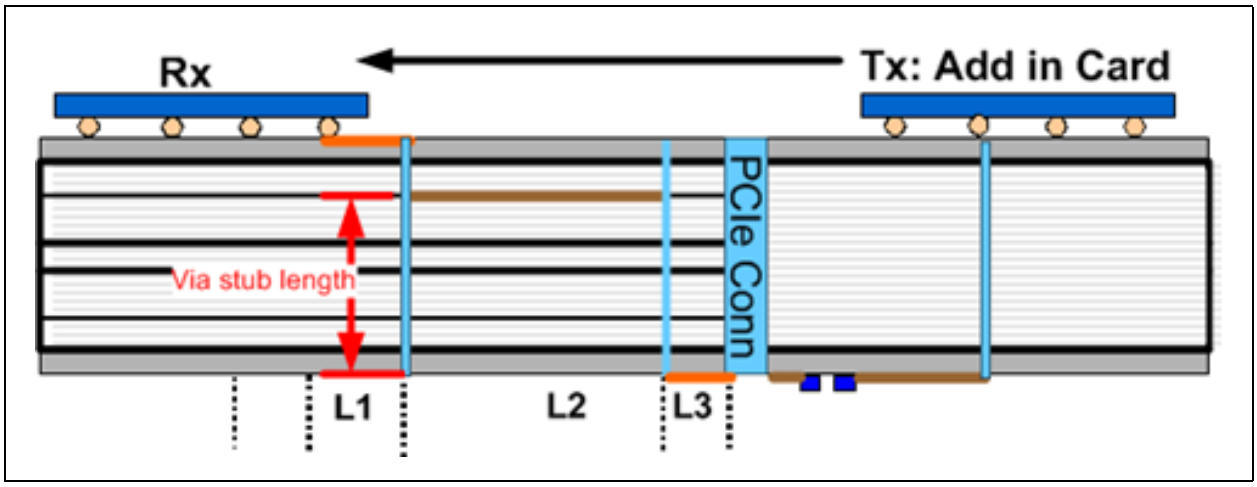
Notes:
1. The maximum length does not necessarily correspond to the "outer edge" of the design space with minimally-passing electrical performance.
2. The maximum PCB loss on this topology for baseboard is 11.49 dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers may be calculated by LossEnabler=11.49 dB/ TargetLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets may be different for stripline and microstrip layers, as long as the total loss target is satisfied.

5.3.3 One Connector Receive Routing Guidelines — Internal Breakout

This section gives routing guidelines for one connector receive with Internal breakout for internal breakout to same layer and internal breakout to top.

Internal Breakout to Same Layer Routing Guidelines

Figure 5-4. PCIE3 Receive, One Connector, Internal Breakout to Same Layer



Note:
1. This topology is simulated and validated by Intel.

Table 5-7. PCIE3 Receive, One Connector, Internal Breakout to Same Layer

Layout Guideline	L1	L2	L3	Units	Notes
Via stub (max)	80	13	0	mils	
Spacing across pairs within the same port	9*h*	3*h*	9*h*		
Min. Trace Length	L1+L2+L3 ≥ 3			Inches	
Max Trace Length	1.2	15-L1-L3	0.5	Inches	
Layer Assignment	Microstrip	Stripline	Microstrip		

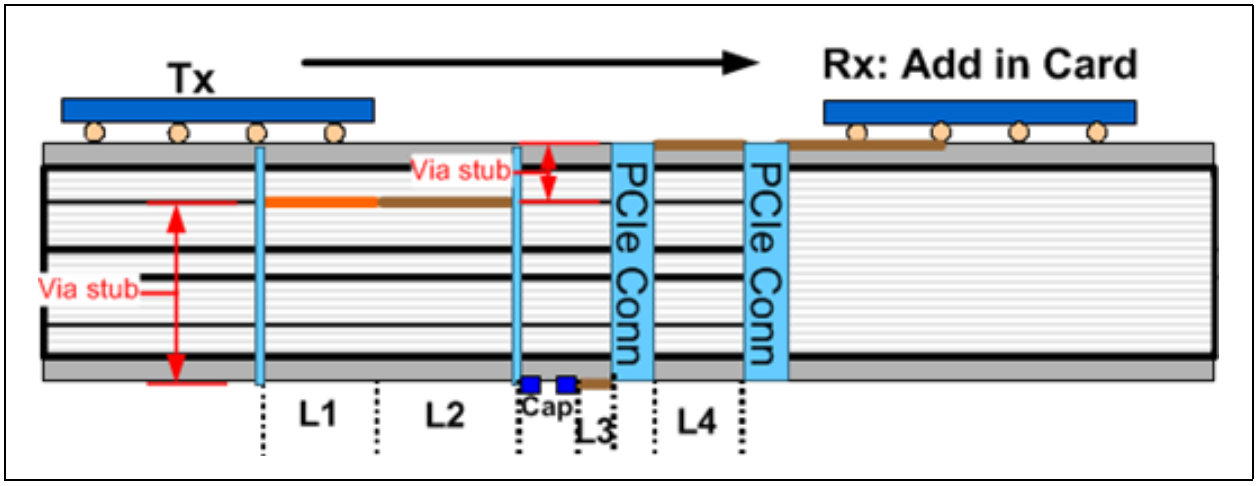
Notes:
1. The maximum length does not necessarily correspond to the "outer edge" of the design space with minimally-passing electrical performance.
2. The maximum PCB loss on this topology for baseboard is 11.25 dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers may be calculated by LossEnabler=11.25 dB/ TargetLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets may be different for stripline and microstrip layers, as long as the total loss target is satisfied.

5.3.4 Two Connector Transmit Routing Guidelines — Internal Breakout

This section gives routing guidelines for two connector transmit with Internal breakout for internal breakout to bottom short, internal breakout to bottom and internal breakout to top.

Internal Breakout to Bottom Short Routing Guidelines

Figure 5-5. PCIE3 Transmit, Two Connector, Internal Breakout to Bottom Short



Notes:
1. L1 is the SoC pin field region. A trace is necessary on Layer 1 traveling from pad to via of 23-mils, but it is not shown in the graphic.
2. As long as the maximum length is not exceeded, the AC coupling cap can be placed anywhere along the L3 route. Simulations show optimal margins when AC coupling cap placed further from the CPU.
3. This topology is simulated and validated by Intel at 3*h* space and 15” total channel length.

Table 5-8. PCIE3 Transmit, Two Connector, Internal Breakout to Bottom Short

Layout Guideline	L1	L2	L3	L4	Units	Notes
Via stub (max)	80	13	0	62	mils	
Spacing across pairs within the same port	Breakout	3*h*	9*h*	15*h*		
Min. Trace Length	L1+L2+L3+L4 ≥ 6				Inches	
Max Trace Length	1.2	15-L1-L3-L4	1.0	8	Inches	
Layer Assignment	Stripline		Bottom Microstrip	Microstrip		

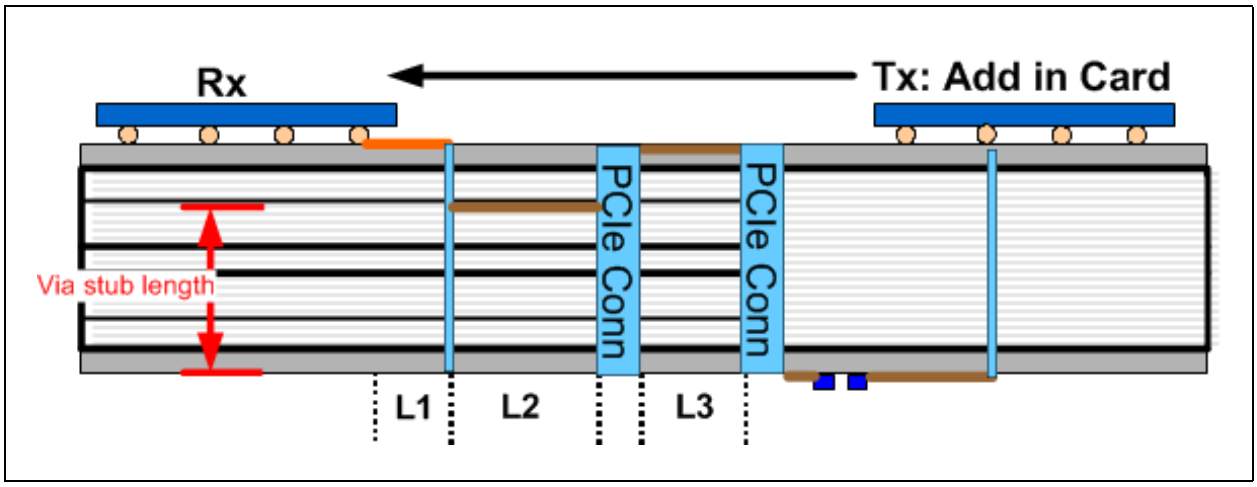
Note:
1. The maximum PCB loss on this topology for baseboard and riser is 11.57dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enabler for the baseboard of 0.701 dB/in for a total of 16 in, including a 4" riser at 0.79 dB/in, is calculated 0.701 = (11.57-riserLen*riserLoss)/ targetBaseboardLength, which is 0.701 = 8.41 dB/12in. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets may be different for stripline and microstrip layers, as long as the total loss target is satisfied.

5.3.5 Two Connector Receive Routing Guidelines - Internal Breakout

This section gives routing guidelines for two connector receive with Internal breakout for internal breakout to same and 3 via internal breakout to top.

Internal Breakout to Same Routing Guidelines

Figure 5-6. PCIE3 Receive, Two Connector, Internal Breakout to Same



Note:
1. This topology is simulated and will be validated by Intel at 3*h* space and 15" total channel length.

Table 5-9. PCIE3 Receive, Two Connector, Internal Breakout to Same

Layout Guideline	L1	L2	L3	Units	Notes
Via stub (max)	80	80	62	mils	
Spacing across pairs within the same port	9*h*	3*h*	15*h*		
Min. Trace Length	L1+L2+L3 ≥ 6			Inches	
Max Trace Length	1.2	14-L1-L3	8	Inches	
Layer Assignment	Microstrip	Stripline	Microstrip		

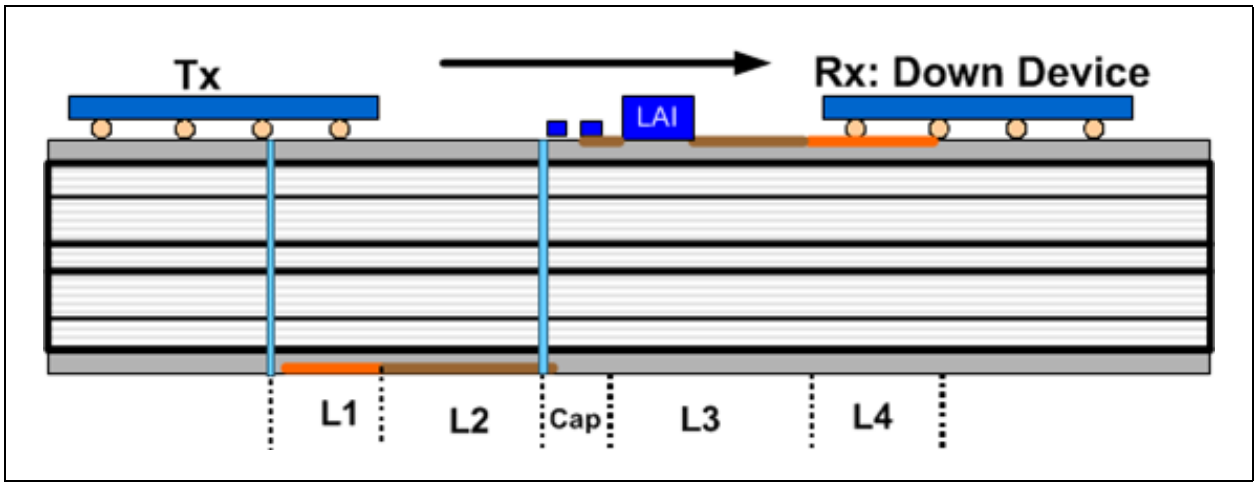
Notes:
1. The maximum length with increased spacing options do not necessarily correspond to the "outer edge" of the design space with minimally-passing electrical performance.
2. The maximum PCB loss on this topology for baseboard and riser is 11.57 dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers for the baseboard may be calculated by LossEnabler = (11.57 - riserLen*riserLoss)/baseboardLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets can differ for each layer, as long as total is met.

5.3.6 Down Device Transmit/Receive Routing Guidelines

This section gives routing guidelines for down device transmit/receive with internal breakout for transmit internal breakout to bottom, receive internal breakout to bottom and transmit/receive internal breakout to same.

Transmit Internal Breakout to Bottom Routing Guidelines

Figure 5-7. PCIE3 Transmit (Tx), Down Device, Internal Breakout to Bottom



Notes:

1. L1 is the SoC pin field region. A trace is necessary on Layer 1 traveling from pad to via of 23-mils, but it is not shown in the graphic.
2. Test point pads on the bottom layer may restrict (mechanical clearance) a breakout with 4 mil trace width. In this circumstance a constant trace width of 3.5 mils and intrapair spacing of 4.0 mils is recommended in the breakout region.
3. This topology is simulated but not validated by Intel.

Table 5-10. PCIE3 Transmit, Down Device, Internal Breakout to Bottom

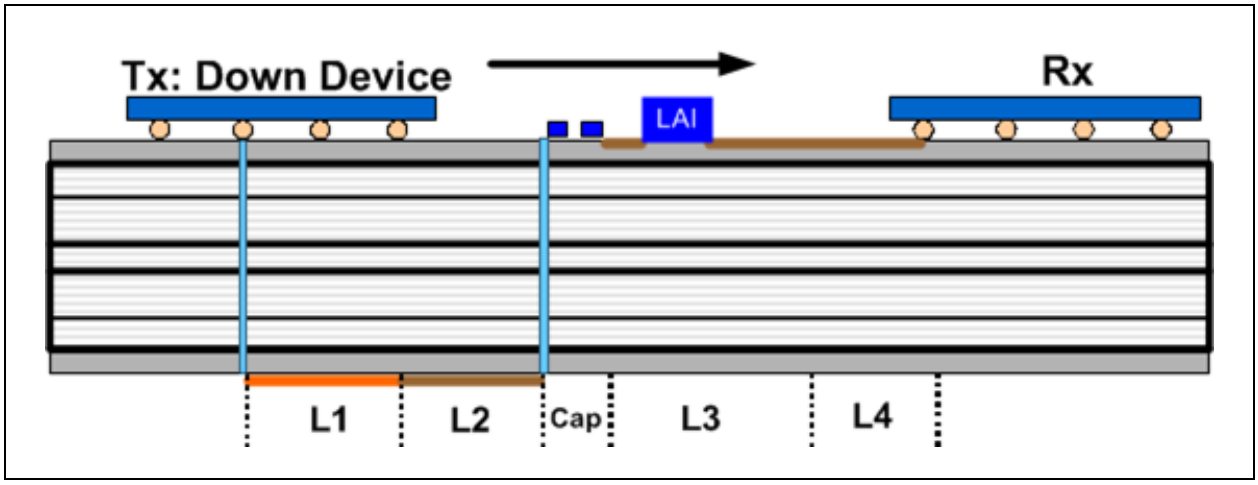
Layout Guideline	L1	L2	L3	L4	Units	Notes
Via stub (max)	0				mils	
Spacing across pairs within the same port	Breakout	9*h*	9*h*	Breakout		
Min. Trace Length	L1+L2+L3+L4 ≥ 3 and L3+L4 ≥ 1.2				Inches	
Max Trace Length	1.2	15	17-L1-L2-L4	0.5	Inches	
Layer Assignment	Bottom Microstrip		Top Microstrip			

Notes:

1. The maximum length does not necessarily correspond to the "outer edge" of the design space with minimally-passing electrical performance.
2. The maximum PCB loss on this topology for baseboard and riser is 13.43 dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers for the baseboard may be calculated by LossEnabler = 13.43 dB/TargetLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets can differ for each layer, as long as total is met.

Receive Internal Breakout to Bottom Routing Guidelines

Figure 5-8. PCIE3 Receive (Rx), Down Device, Internal Breakout to Bottom



Notes:
1. Test point pads on the bottom layer may restrict (mechanical clearance) a breakout with 4 mil trace width. In this circumstance a constant trace width of 3.5 mils and intrapair spacing of 4.0 mils is recommended in the breakout region.
2. This topology is simulated but not validated by Intel.

Table 5-11. PCIE3 Receive, Down Device, Internal Breakout to Bottom

Layout Guideline	L1	L2	L3	L4	Units	Notes
Via stub (max)	0				mils	
Spacing across pairs within the same port	Breakout	9*h*	9*h*	9*h*		
Min. Trace Length	L1+L2+L3+L4 ≥ 3 and L3+L4 ≥ 1.4				Inches	
Max Trace Length	1.2	15	17-L1-L2-L4	0.5	Inches	
Layer Assignment	Bottom Microstrip		Top Microstrip			

Notes:
1. The maximum length does not necessarily correspond to the "outer edge" of the design space with minimally-passing electrical performance.
2. The maximum PCB loss on this topology for baseboard and riser is 13.43 dB at 4 GHz, determined using the most microstrip (higher loss) as allowed. Loss enablers for the baseboard may be calculated by LossEnabler = 13.43 /TargetLength. Lower loss materials are not simulated by Intel and need to be simulated to understand crosstalk and reflection impacts. Loss targets can differ for each layer, as long as total is met.

5.4 Unused PCIe* Ports

When the PCI Express port is not implemented on the platform, please leave the signal pins non-connected.

§ §

6 Integrated 10 Gb/s Ethernet Controller

This section provides recommendations for selecting components, connecting interfaces, dealing with special pins, and layout guidance for the Integrated 10 Gb Ethernet Controller.

Some unused interfaces should be terminated with pull-up or pull-down resistors. These are indicated in reference schematics or schematic checklists as reserved pins.

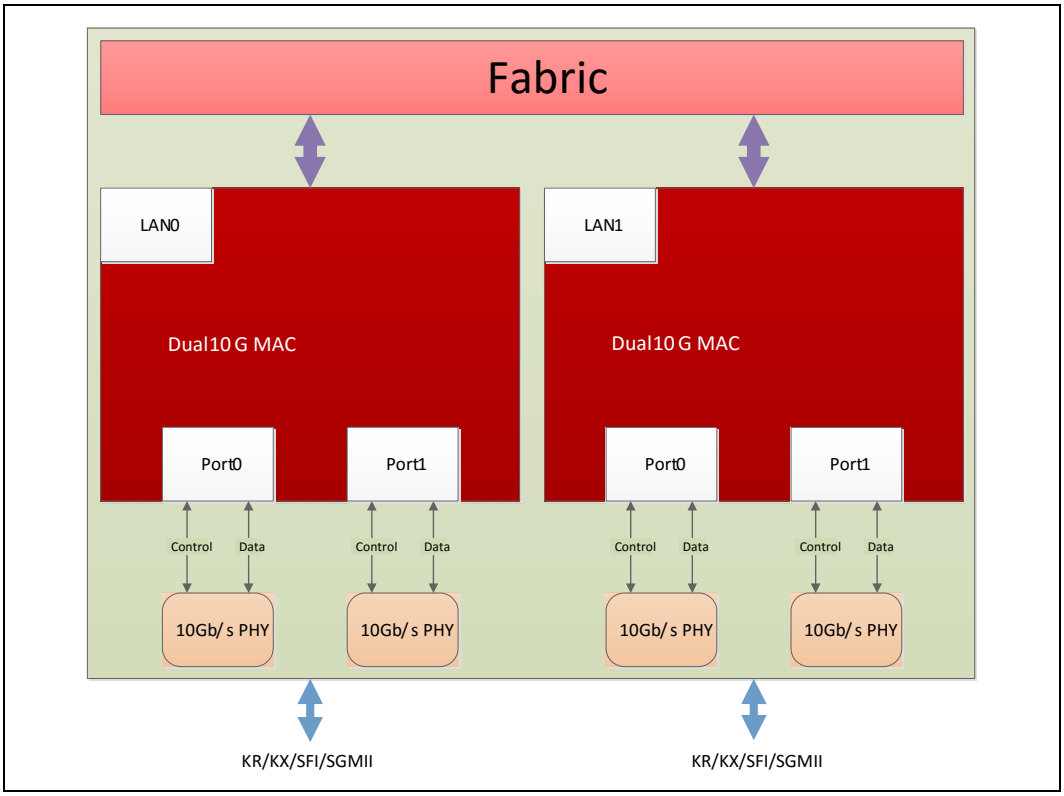
Note: Some unused interfaces must be left open. Do not attach pull-up or pull-down resistors to any balls identified as No Connect or Reserved No Connect.

6.1 Integrated 10 Gb/s Ethernet Controller Overview

The integrated 10 GbE controller contains two independent 10 GbE Media Access Controllers (MACs), SKU dependent, that support an internal XGMII Interface to the following external physical layer (PHY) device interfaces.

- LAN Controller 0 will be enabled for product SKUs that only have two ports.
- For product SKU with LAN controller 0 and LAN controller 1 if SOC Ethernet is used LAN controller 0 must be enabled.
- The Ethernet Controllers provide up to four 10 GbE MAC ports.
- Each MAC port connects over an internal XGMII path to the internal PHY. This PHY does not support a BASE-T copper connection.
- Each Ethernet MAC port supports 10 GbE, 2.5 GbE, and 1.0 GbE operation (SKU dependent). Full duplex 10/100Mb is also available.

Figure 6-1. Integrated 10 GbE Logical Block Diagram



The integrated 10 GbE controller supports 10 GbE/2.5 GbE/1 GbE/ (10/100Mb full duplex) operations on its network data interface. Auto-negotiation, when configured for 10GBASE-KR and 1000BASE-KX backplane Ethernet to automatically select between supported modes on each PHY.

LAN0 and LAN1 use two sections of the shared system SPI to configure parameters for all LAN Ports and PCI Functions including MAC Addresses, LED behaviors, receive packet filters for manageability, and wakeup capability.

Please refer to section 13.8, *Shared SPI for use with LAN0 and LAN1* of the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* for more details.

Choose the appropriate configuration for your system configuration listed in Table 6-1.

Table 6-1 lists the supported operating modes and link partners.

Note: LAN port topologies must be the same for each respective LAN, for example, Ports 0 and 1 of LAN0 must be the same Ethernet mode. LAN 0 and LAN 1, however, can support different topologies as long as care is given to the trace layout.

Table 6-1. Supported System Configurations (Sheet 1 of 2)

Connection	Speed	Electrical Interface	Third Party PHYs/Switches
Backplane	1 GbE	1000BASE-KX	Intel® FM4000/FM5000/FM6000 Ethernet switches Broadcom* BCM5684x-series switches
Backplane	10 GbE	10GBASE-KR	Intel® FM5000/FM6000 Ethernet switches Broadcom BCM5684x-series switches
Backplane	2.5 GbE	2500BASE-X[1]	Intel® FM4000/FM5000/FM6000 Ethernet switches Broadcom BCM5684x-series switches
10BASE-T [6]	10 Mb/s	SGMII (no half duplex support)	Marvell 88E1512 Marvell 88E1514 Marvell 88E1543
100BASE-TX [6]	100 Mb/s	SGMII (no half duplex support)	Marvell 88E1512 Marvell 88E1514 Marvell 88E1543
1000BASE-T [6]	1 GbE	SGMII (no half duplex support)	Marvell 88E1514 Marvell 88E1543 Marvell 88E1512
10GBASE-T	10 GbE	10GBASE-KR	Intel® X557-AT2/AT4 10 GbE PHY
1000BASE-T	1 GbE	1000BASE-KX	Intel® X557-AT2/AT4 10 GbE PHY

Table 6-1. Supported System Configurations (Sheet 2 of 2)

Connection	Speed	Electrical Interface	Third Party PHYs/Switches
SFP+ [7]	10 GbE	SFI	Native SFI support ***Note:*** Native SFI can be used to connect to cables OR SFP+ modules, and may not be used to connect to a PHY. See Table 6-3, Supported SFP+ Modules/Cables for supported cables and modules.
SFP+ [7]	1 GbE	SFI	Native SFI support ***Note:*** Native SFI can be used to connect to cables OR SFP+ modules, and may not be used to connect to a PHY. See Table 6-3, Supported SFP+ Modules/Cables for supported cables and modules.
SFP+ [7]	10 GbE	KR	Inphi CS4227 (2 port) Inphi CS4223 (4 port) See Table 6-3, Supported SFP+ Modules/Cables for supported cables and modules.
SFP+ [7]	1 GbE	KX	Inphi CS4227 (2 port) Inphi CS4223 (4 port) See Table 6-3, Supported SFP+ Modules/Cables for supported cables and modules.

Notes:
1. 2500BASE-X is not an IEEE standard. The SoC supports 2.5G rate only.
2. No support for half duplex.
3. Inphi devices required for long reach support in KR mode.
4. For supported cables and modules refer to Table 6-3, "Supported SFP+ Modules/Cables", Supported SFP+ Modules/Cables.
5. CS422X devices include integrated Rx CAPS, DO NOT include 100nF for Rx traces close to the devices.
6. The 88E1512 and 88E1514 only support two MDIO addresses (0 or 1) therefore a maximum of 2 of these PHY devices can be used with each SoC.
7. 1 GbE speed is only supported with 1000BASE-SX Optical modules.

Table 6-2. 3rd Party PHY Support

Intel Recommended/Supported 3rd Party PHYs	3rd Party Non-Supported PHYs
Design-in support	Customer owns design-in support
Driver development and validation with updates and patches as required	Customer owns driver development and validation
End-to-end tuning support	Resources for external PHY tuning are provided by the customer
Reference platforms available for software development issue replication	No reference platform support
Debug support through IPS (Intel debug tracker)	Potential low power functional impact
IEEE/MSA compliance testings support	Compliance testing is not supported

Table 6-3. Supported SFP+ Modules/Cables

Connector	Media
SFP+	Intel-branded SFP+ SR/LR dual speed (1G/10G) optical modules
	Intel-branded SFP+ DA twin-ax cables that comply with SFF-8431 v4.1 and SFF-8472 v10.4 specifications. [3]
	Third party SFP+ DA twin-ax cables that comply with SFF-8431 v4.1 and SFF-8472 v10.4 specifications. [3]
	SFP+ AoCs (Active optical cables) [3]
	Third party SFP+ SR/LR dual speed (1G/10G) optical modules
	SFP+ active copper cables
	1000BASE-SX /1000BASE-LX optical modules

Notes:
1. Support only limiting initialization active direct attach cables. No support for linear init active cables.
2. It has been observed that some modules do not have a default rate selection in SFP+ registers 110.3 and 118.3, therefore when such modules power up a driver or BMC has to configure the rate select value in order to establish link up.
3. Limited to 10G link speed (no 1G support).

Table 6-4. LAN Controller LEK Image Support Model [1] (Sheet 1 of 2)

LEK Image (Refer to Snapshot)	LAN Controller 0/1 [12]		Support Model (Both Ports)	Product POR
	Port 0	Port 1		
LEK1 [3, 7, 9]	SFI		SFI & direct attach copper cable SFI & optical module	**10G CAPABLE LAN CONTROLLER SKU ONLY** Specification compliant [2]
LEK2 [3, 7, 8, 9, 10]	KR		KR—Inphi—SFP+	**10G CAPABLE LAN CONTROLLER SKU ONLY** **Inphi CS4227 (2 port)** • PHY slice 0 must be connected to LAN x Port 0 • PHY slice 1 must be connected to LAN x Port 1 ***Note:*** Both Xs have to be either LAN controller 0 or LAN controller 1 • Only one CS4227 can be used with each SoC • MDIO address must be strapped to 0x1F **Inphi CS4223 (4 port)** • PHY slice 0 must be connected to LAN 0 Port 0 • PHY slice 1 must be connected to LAN 0 Port 1 • PHY slice 2 must be connected to LAN 1 Port 0 • PHY slice 3 must be connected to LAN 1 Port 1 • MDIO address must be strapped to 0x1F • On SFI interface use the same modules and cables as supported in LEK1
LEK3 [4, 6, 7, 8, 11]	KR		Dual-speed (10G / 1G) with auto-neg KX-1000BASE-T KR-10GBASE-T: Intel® X557-AT2/AT4 10 GbE PHY	**10G CAPABLE LAN CONTROLLER SKU ONLY** **X557-AT2 (2 port)** • PHY 0 MDIO address must be 0 and connected to LAN 0 Port 0 • PHY 1 MDIO address must be 1 and connected to LAN 0 Port 1 Or • PHY 0 MDIO address must be 2 and connected to LAN 1 Port 0 • PHY 1 MDIO address must be 3 and connected to LAN 1 Port 1 **X557-AT4 (4 port)** • PHY 0 MDIO address must be 0 and connected to LAN 0 Port 0 • PHY 1 MDIO address must be 1 and connected to LAN 0 Port 1 • PHY 2 MDIO address must be 2 and connected to LAN 1 Port 0 • PHY 3 MDIO address must be 3 and connected to LAN 1 Port 1
LEK4 [3]	SGMII		Backplane	Support clause 37, no UNDI, no PXE OPROM, no Sideband Management, Linux support only, tested with 1G Link Partner only.
LEK5 [4, 11]	SGMII		SGMII—1000BASE-T: Marvell 88E1512 [5] Marvell 88E1514 [5]	Support 10/100 and 1G full duplex only • LAN 0 Port 0 must be connected to PHY with MDIO address of 0 • LAN 0 Port 1 must be connected to PHY with MDIO address of 1 • For LAN 1 implementation please contact your Intel representative.

Table 6-4. LAN Controller LEK Image Support Model [1] (Sheet 2 of 2)

LEK Image (Refer to Snapshot)	LAN Controller 0/1 [12]		Support Model (Both Ports)	Product POR
	Port 0	Port 1		
LEK6 [4]	KR or KX via AN		Backplane	Support Clause 73 AN or Parallel detect
LEK7 [3, 10]	2500BASE-X		Backplane	Support 2.5G only
LEK8 [4, 11]	SGMII		SGMII—1000BASE-T: Marvell 88E1543	Support 10/100 and 1G full duplex only • LAN 0 Port 0 must be connected to PHY with MDIO address of 0 • LAN 0 Port 1 must be connected to PHY with MDIO address of 1 • LAN 1 Port 0 must be connected to PHY with MDIO address of 2 • LAN 1 Port 1 must be connected to PHY with MDIO address of 3

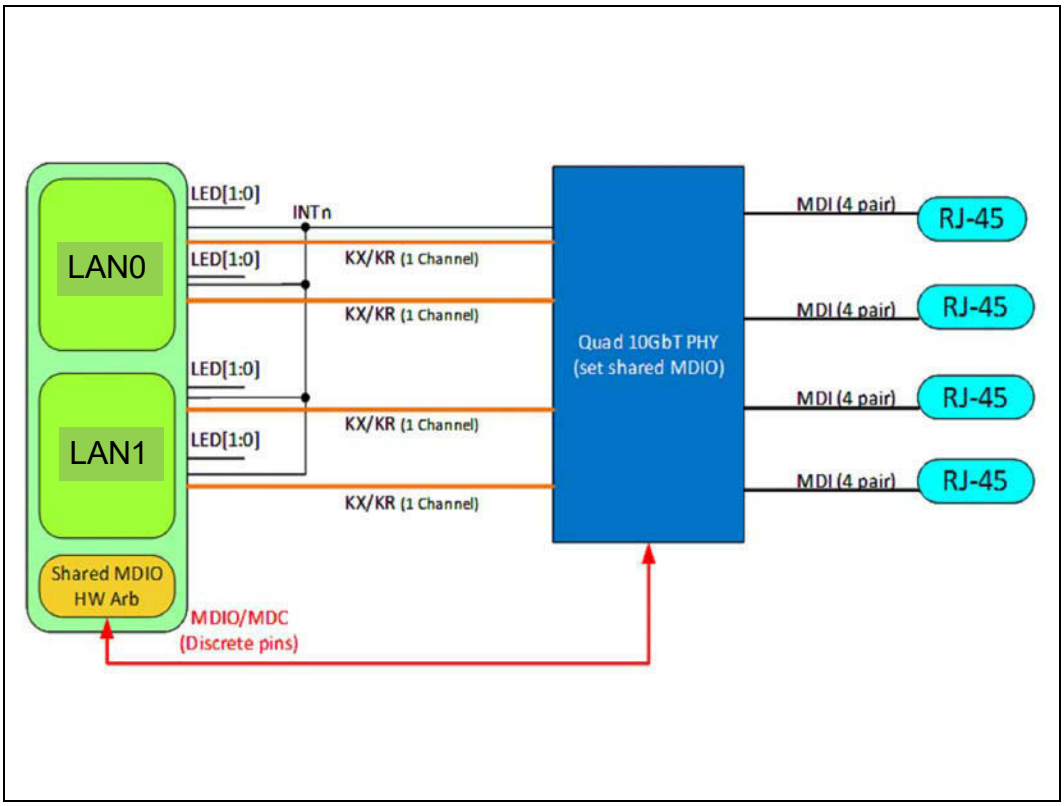
Notes:
1. LAN port topologies must be the same for each respective LAN, for example, Ports 0 and 1 of LAN0 must be the same Ethernet mode. However, LAN 0 and LAN 1 can support different topologies as long as care is given to the trace layout.
2. <= 3m cable length is suggested for Alpha LEK image, specification compliant target for QS samples with LEK image.
3. This LEK will not support Wake on LAN.
4. This LEK will provide Wake on LAN support.
5. The 88E1512 and 88E1514 only support two MDIO addresses (0 or 1) therefore a maximum of 2 of these PHY devices can be used with each SoC.
6. 100 Mb/s or 10 Mb/s are not supported.
7. This LEK should only be loaded in 10G Capable LAN Controller SKU.
8. Program the external EEPROM for Inphi and Coppervale phys off-line before installing it on the board. Lanconf and EEUpdate tools take up to 15 min to program the external EEPROM.
9. This LEK (Native SFI (LEK 1) or Inphi (LEK 2)) requires use of I2C interface. For the I2C interface to function LEK 1 or LEK 2 must be loaded on LAN Controller 0. If desired, LEK 1 or LEK 2 can be used on both LAN controllers.
10. This LEK will not support internal phy loopback.
11. This LEK will support internal phy loopback.
12. In applications utilizing only 1 LAN controller, LAN controller 0 must be enabled and used.

6.1.1 Configuration Block Diagrams

This implementation uses a 10G BASE-T PHY to enable 4 ports of 10G BASE-T via the KR support in Denverton LAN0 and LAN1. MDIO/MDC is utilized to configure the PHY at initialization for KR mode.

Please refer to Table 6-2, "3rd Party PHY Support" for the list of supported external PHYs.

Figure 6-2. 10GBASE-T Block Diagram

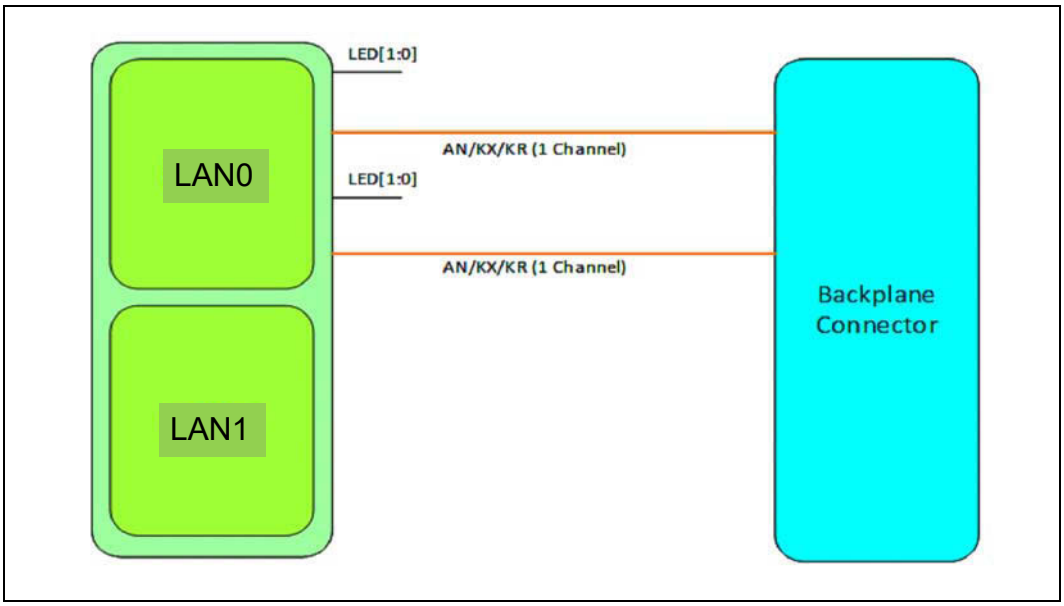


This implementation uses a KR support in the SoC LAN0 only for the connection to a supported backplane partner. Long reach KR can be achieved with the use of Inphi CS4227 (2 port) or Inphi CS4223 (4 port).

Please refer to Table 6-1, "Supported System Configurations" for the list of supported switches.

Note: 2.5G implementations will look similar. Please refer to Table 6-1, "Supported System Configurations" for list of supported 2.5G switches.

Figure 6-3. 10GBASE-KR Block Diagram

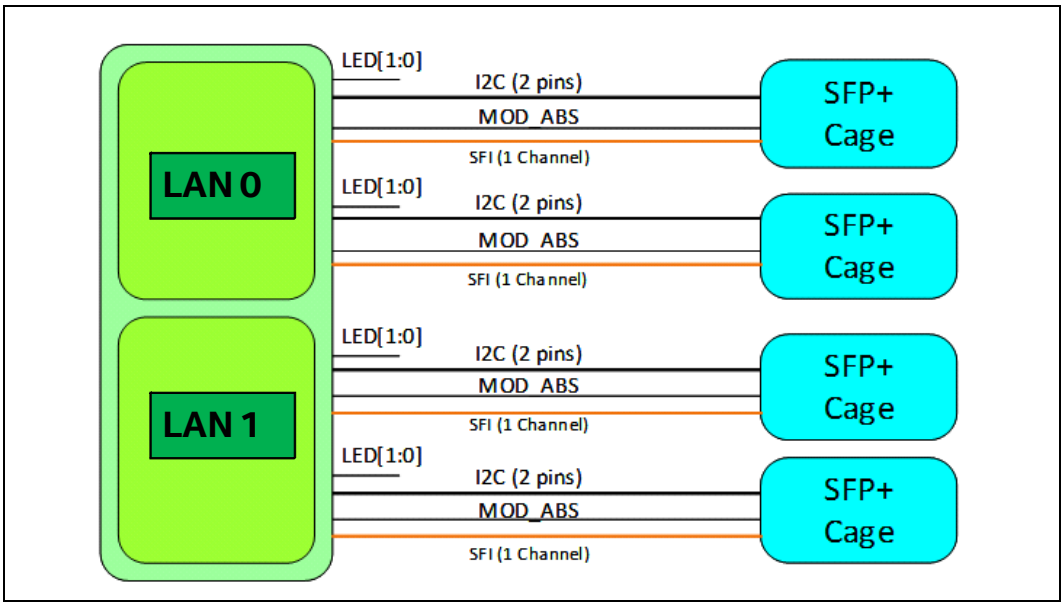


This implementation uses SFI in LAN0 and LAN1 for connection to supported SFP+ optical modules. MOD_ABS (module absence) is provided via GPIO support. I2C connectivity is needed to ensure supported optical modules are populated. Please refer to the list of supported optical modules in the Denverton Design In Slides.

Long reach SFI can be achieved with the use of Inphi CS4227 (2 port) or Inphi CS4223 (4 port)

LAN port topologies must be the same for each respective LAN, for example, Ports 0 and 1 of LAN0 must be the same Ethernet mode. LAN 0 and LAN 1, however, can support different Ethernet modes as long as care is given to the trace layout. Due to the cross-talk requirements one may not mix DAC (Direct-Attached-Cable) and Optical modules on ports 0 and 1 of the same LAN when using an SFI (native) design.

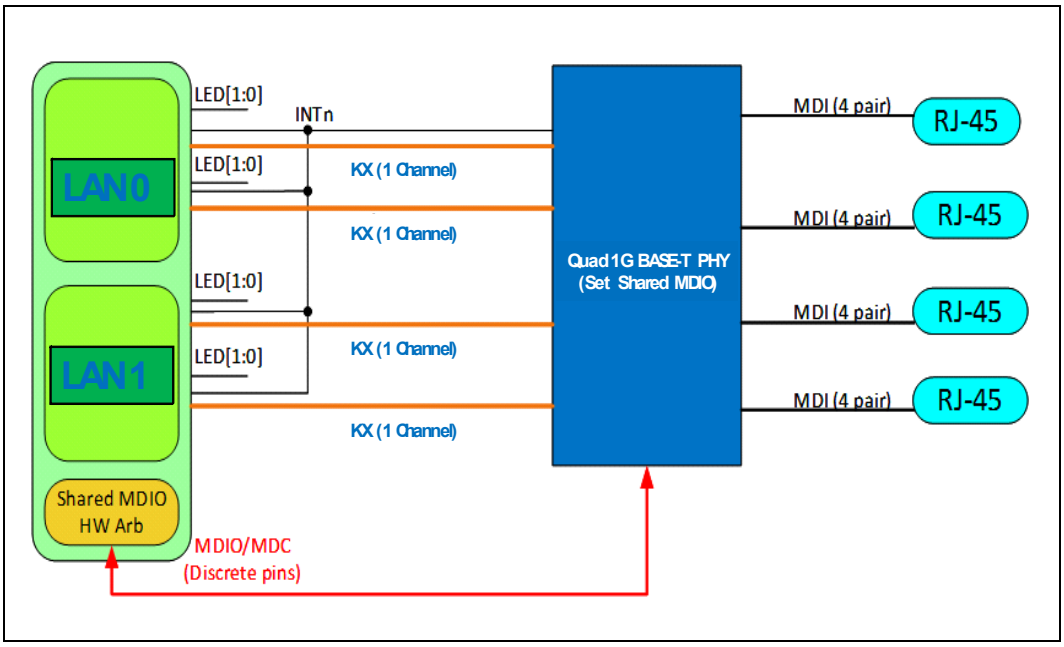
Figure 6-4. SFI+ Designs



This implementation uses a 1000 BASE-T PHY to enable 4 ports of 1000 BASE-T via the KX (or SGMII) support in Denverton LAN0 and LAN1. MDIO/MDC is utilized to configure the PHY at initialization for KX or SGMII mode.

Please refer to the list of supported external PHYs in Table 6-2, "3rd Party PHY Support".

Figure 6-5. 1000BASE-KX / SGMII Block Diagram



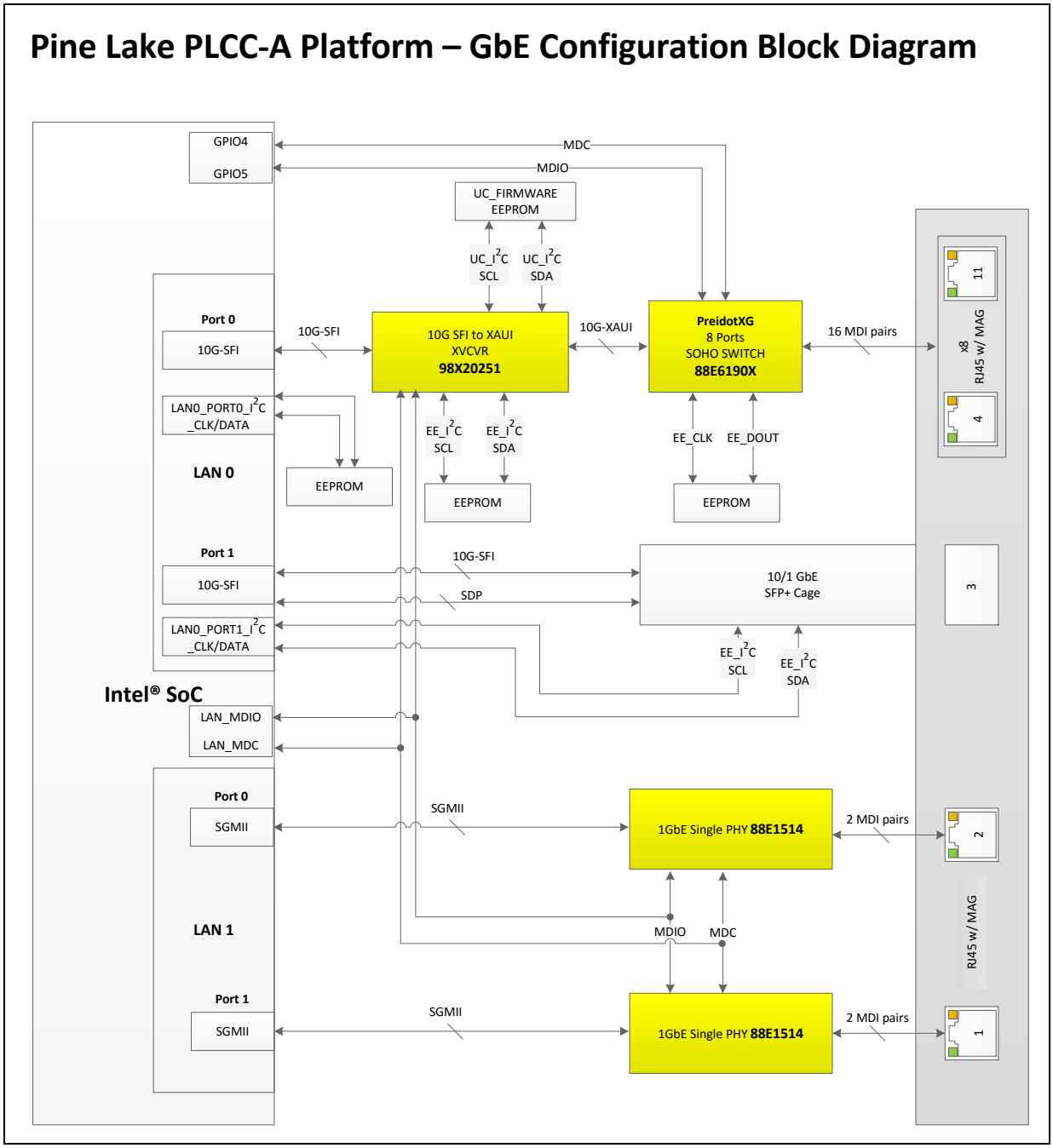
6.2 PLCC-A GbE Full Feature Platform

The platform configuration in Figure 6-6 shows that the SoC is connected to a 10GbE SFI interface to an XAUI transceiver. Then the transceiver is connected to the SOHO switch with eight GbE Base-T ports. The platform also provides an additional one SPF+ 10GbE port and two Ethernet 1GbE Base-T ports.

Table 6-5. PLCC-A GbE Topologies

SoC LAN/Port	LAN Topology	Channel Length (between LPs) Min. | Max.		Channel Loss dB/in	Number of Connectors	Type of Connection	Link Partner	Number of Repeater
LAN0/Port0	SFI	3″	5″	0.712 dB/in @ Nyquist	0	Device Down SFI to XAUI	a. 98X20251 SFItoXAUI b. 88E6190X SOHO switch with PHYs	0
LAN0/Port1	SFI	3″	5″	0.712 dB/in @ Nyquist	0	SFP+ Cage	SFP Module	0
LAN1/Port0	SGMII	Follow the *Harrisonville Platform Design Guide (PDG)*.			0	Base-T	88E1514 PHY	0
LAN1/Port1	SGMII				0	Base-T	88E1514 PHY	0

Figure 6-6. PLCC-A Platform - GbE Ethernet Configuration Block Diagram Overview



Notes:

1. This platform configuration has not been validated by Intel.
2. The SFI to XAUI transceiver is not a supported device by the LAN Enablement Kits (LEKs) provided by Intel. Therefore, to implement this solution the XAUI transceiver must present itself to the LAN port as a passive SFP+ module then LEK1 can be used to run traffic.

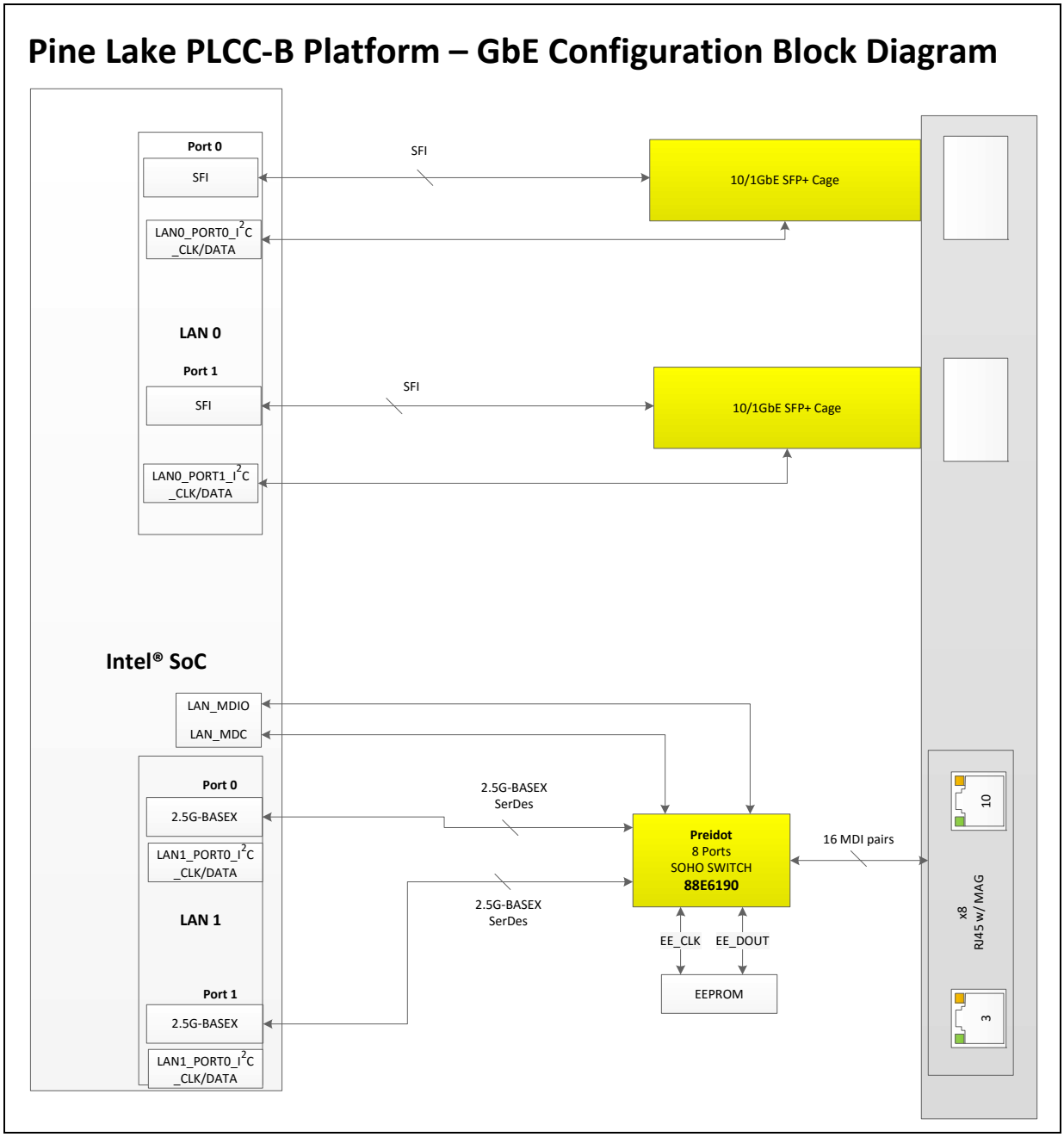
6.3 PLCC-B GbE Optimized Feature Platform

The platform configuration in Figure 6-7 shows that the SoC is connected to two 2.5GbE interfaces (total 5GbE interface) that is connected to a SOHO switch with 8 GbE Base-T ports. The platform also has an additional two Ethernet 1GbE Base-T ports.

Table 6-6. PLCC-B GbE Topologies

SoC LAN/Port	LAN Topology	Channel Length (Between LPs) Min. | Max.	Channel Loss dB/in	Number of Connectors	Type of Connection	Link Partner	Number of Repeater
LAN0/Port0	SFP+	Follow the *Harrisonville Platform Design Guide (PDG)*.		0	Native SFI	SFP+	0
LAN0/Port1	SFP+			0		SFP+	0
LAN1/Port0	2.5G BaseX			0	SOHO Switch Device Down	88E6190 SOHO Switch with PHYs	0
LAN1/Port1	2.5G BaseX			0		88E6190 SOHO Switch with PHYs	0

Figure 6-7. PLCC-B Platform - GbE Ethernet Configuration Block Diagram Overview



Notes:
1. This platform configuration has not been validated by Intel.
2. This configuration is being validated and is subject to change.

6.4 Connecting High Speed LAN Interfaces

6.4.1 High Speed Channels Lane Connections

These signals are 100 Ω terminated differential signals that are AC coupled near the receiver. It is recommended to place the AC coupling capacitors less than one inch away from the receiver, if possible. The recommended value for the capacitor should be 100 nF or as specified in the IEEE 802.3 standard. Capacitor size should be small to reduce parasitic inductance. Use X5R or X7R, ± 10% capacitors in a 0402 or 0201 package size. Do not place redundant capacitors in the path.

Table 6-7 lists the integrated LAN controllers network data interface pins.

For connectivity refer to the Intel Ethernet Network Connection X553 [Denverton] Schematic Checklist *(Document #551166)*.

Table 6-7. Network Data Interface Pin Names/Descriptions (Sheet 1 of 4)

Signal Name	Direction	Shared	Description
LAN Ports 0 and 1 - LAN Controller 0 (Virtual Root Port 0)			
LAN0_PORT0_I2C_CLK	I,O-OD	Yes	I2C Clock: The 2-wire management interface Clock used to access the management registers of an external optical module of port n. One clock pulse is generated for each data bit transferred.
LAN0_PORT0_I2C_DATA	I,O-OD	Yes	I2C Data: The Data of the 2-wire management interface used to access the management registers of an external optical module of port n. Stable during the clock high period (unless it is a start or stop condition).
LAN0_PORT0_LED[3:0]	O-OD	Yes	LED Drivers: Four LED drivers for this LAN Port.
LAN0_PORT0_SDP[3:0]	I,O	Yes	Software Defined Pins: Four general-purpose SDPs for this LAN Port can be used to support IEEE1588 auxiliary devices or input for external interrupts.
LAN0_PORT0_RX_DP LAN0_PORT0_RX_DN	I, Differential	No	PHY Differential Output: This lane is used in 10GBASE-KR, 1000BASE-KX, 2.5G, SGMII, and SFI.
LAN0_PORT0_TX_DP LAN0_PORT0_TX_DN	O, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN0_PORT1_I2C_CLK	I,O-OD	Yes	I2C Clock: The 2-wire management interface Clock used to access the management registers of an external optical module of port n. One clock pulse is generated for each data bit transferred.
LAN0_PORT1_I2C_DATA	I,O-OD	Yes	I2C Data: The Data of the 2-wire management interface used to access the management registers of an external optical module of port n. Stable during the clock high period (unless it is a start or stop condition).
LAN0_PORT1_LED[1:0]	O-OD	Yes	LED Drivers: Four LED drivers for this LAN Port.

Table 6-7. Network Data Interface Pin Names/Descriptions (Sheet 2 of 4)

Signal Name	Direction	Shared	Description
LAN0_PORT1_SDP[3:0]	O	Yes	Software Defined Pins: Four general-purpose SDPs for this LAN Port, can be used to support IEEE1588 auxiliary devices or input for external interrupts.
LAN0_PORT1_RX_DP LAN0_PORT0_RX_DN	I, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN0_PORT1_TX_DP LAN0_PORT1_TX_DN	O, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN0_RBIAS	I,O	No	Bias Resistor: External resistor bias input.
LAN Ports 0 and 1 - LAN Controller 1(Virtual Root Port 1)			
LAN1_PORT0_I2C_CLK	I,O-OD	Yes	I2C Clock: The 2-wire management interface Clock used to access the management registers of an external optical module of port n. One clock pulse is generated for each data bit transferred.
LAN1_PORT0_I2C_DATA	I,O-OD	Yes	I2C Data: The Data of the 2-wire management interface used to access the management registers of an external optical module of port n. Stable during the clock high period (unless it is a start or stop condition).
LAN1_PORT0_LED[1:0]	O-OD	Yes	LED Drivers: Four LED drivers for this LAN Port.
LAN1_PORT0_SDP[1:0]	O	Yes	Software Defined Pins: Two general-purpose SDPs for this LAN Port, can be used to support IEEE1588 auxiliary devices or input for external interrupts.
LAN1_PORT0_RX_DP LAN1_PORT0_RX_DN	I, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN1_PORT0_TX_DP LAN1_PORT0_TX_DN	O, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN1_PORT1_I2C_CLK	I,O-OD	Yes	I2C Clock: The 2-wire management interface Clock used to access the management registers of an external optical module of port n. One clock pulse is generated for each data bit transferred.
LAN1_PORT1_I2C_DATA	I,O-OD	Yes	I2C Data: The Data of the 2-wire management interface used to access the management registers of an external optical module of port n. Stable during the clock high period (unless it is a start or stop condition).
LAN1_PORT1_LED[1:0]	O-OD	Yes	LED Drivers: Four LED drivers for this LAN Port.

Table 6-7. Network Data Interface Pin Names/Descriptions (Sheet 3 of 4)

Signal Name	Direction	Shared	Description
LAN1_PORT1_SDP[1:0]	O	Yes	Software Defined Pins: Two general-purpose SDPs for this LAN Port, can be used to support IEEE1588 auxiliary devices or input for external interrupts.
LAN1_PORT1_RX_DP LAN1_PORT1_RX_DN	I, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN1_PORT1_TX_DP LAN1_PORT1_TX_DN	O, Differential	No	PHY Differential Input: This lane is used in 10G BASE-KR,1000BASE-KX, 2.5G, SGMII and SFI.
LAN1_RBIAS	I,O	No	Bias Resistor: External resistor bias input.
Signals Common to LAN Controllers 0 and 1			
LAN_MDC	I,O-OD	Yes	Management Clock: Clock output for accessing the external PHYs management registers.
LAN_MDIO	I,O-OD	Yes	Management Data: Data output for accessing the external PHYs management registers.
SMB_LAN_DATA	I,O-OD	Yes	SMBus Data: Stable during the high period of the clock (unless it is a start or stop condition).
SMB_LAN_CLK	I,O-OD	Yes	SMBus Clock: One clock pulse is generated per data bit transferred.
SMB_LAN_ALRT_N	I,O-OD	Yes	SMBus Alert: Acts as an interrupt pin of a slave device on the SMBus.
NCSI_ARB_IN	I	Yes	NC-SI Arbitration In
NCSI_ARB_OUT	O	Yes	NC-SI Arbitration Out
NCSI_CLK_IN	I	Yes	NC-SI Reference Clock Input: Synchronous clock reference for receive, transmit, and control interface. It is a 50 MHz clock ± 100 ppm.
NCSI_CRS_DV	I,O-Tri	Yes	Carrier Sense/Receive Data Valid: To Baseboard Management Controller (BMC). Indicates that the data transmitted from B to MC is valid.

Table 6-7. Network Data Interface Pin Names/Descriptions (Sheet 4 of 4)

Signal Name	Direction	Shared	Description
NCSI_RXD[1:0]	I,O-Tri	Yes	MC Receive Data: Data signals from the Denverton SoC LAN controllers to the MC
NCSI_TX_EN	I	Yes	MC Transmit Enable: Indicates received data from the MC is valid.
NCSI_TXD[1:0]	I	Yes	MC Transmit Data: Data signals from the MC to the Denverton SoC LAN controllers.

Note: LAN controllers only have one SMBus and one NC-SI bus associated with all LAN ports. Both the SMBus and NC-SI can be used by the platform board design provided that both sets of signals are configured.

6.4.2 LAN Layout/Routing Recommendation for all Design Modes

The following sections contain layout practices that help facilitate meeting the IEEE 802.3-2012 Annex 69B informative channel parameters. To determine the electrical suitability of 10GBASE-KR system channels, full pin-to-pin system channel models are required. Corresponding frequency domain electrical characteristics must be compared to the IEEE 802.3 Annex 69B recommended channel limits for 10GBASE-KR.

System channel models should include impedance and insertion loss corner cases including but not limited to copper roughness, dielectric loss, fiber weave, temperature, and moisture ingression. The channel models should include all sources of crosstalk: all nearby signal traces on the same routing layers, nearby signal traces on adjacent routing layers (when not shielded by a reference plane between the two signal layers), crosstalk among circuit board signal vias, crosstalk in the connector pin fields, and within the connectors. 10GBASE-KR system channel models must pass all of the recommended electrical limits in Annex 69B. Additional details about Annex 69B are included in this document's appendix.

Two suitable implementations of Annex 69B channel checkers follow.

• Intel Annex 69B Ethernet Board Channel Executable Simulation Kit 21-Apr-2016 *(Document #550875)* plots channel frequency domain characteristics with respect to Annex 69B limits.

• Intel® Interconnect Model Analyzer and Domain Converter (Intel® IMADC) Software, Rev. 1.3.1 *(Document #551538).*

  — The IMADC Intel Interconnect Model Analyzer and Domain Converter [Intel IMADC] Users Guide Revision 1.3 is available as Document #569227.

Annex 69B consist of the following recommended channel limits.

- Differential Insertion
- Loss
- Fitted Attenuation
- Insertion Loss Deviation (ILD)
- Return Loss
- Insertion Loss-to-Crosstalk Ratio (ICR).

System channel models that clearly pass the Annex 69B recommended channel limits with reasonable passing margin will perform with high confidence. Additional verification is not needed.

10GBASE-KR system channel models which approach the recommended Annex 69B limits are recommended to go through an additional level of checking. The 10GBASE-KR COM channel checker which is included in the IMADC (Intel® Interconnect Model Analyzer and Domain Converter (Intel® IMADC) Software, Rev. 1.3.1) utility (Document #551538) can be used as a second level check and verification.

Note: Follow all high speed guidelines in Chapter 2, "Platform Stack-up and General Design Considerations" unless otherwise noted in this chapter.

6.4.2.1 Via Design

Transitions between routing layers in a PCB requires plated through hole via structures. Standard via geometries and associated stubs have a low impedance reflection. These reflections negatively impact the channel by inducing inter-symbol-interference, which can be noted in channel responses such as Time-domain Reflectometry (TDR) profiles, ILD, and RL.

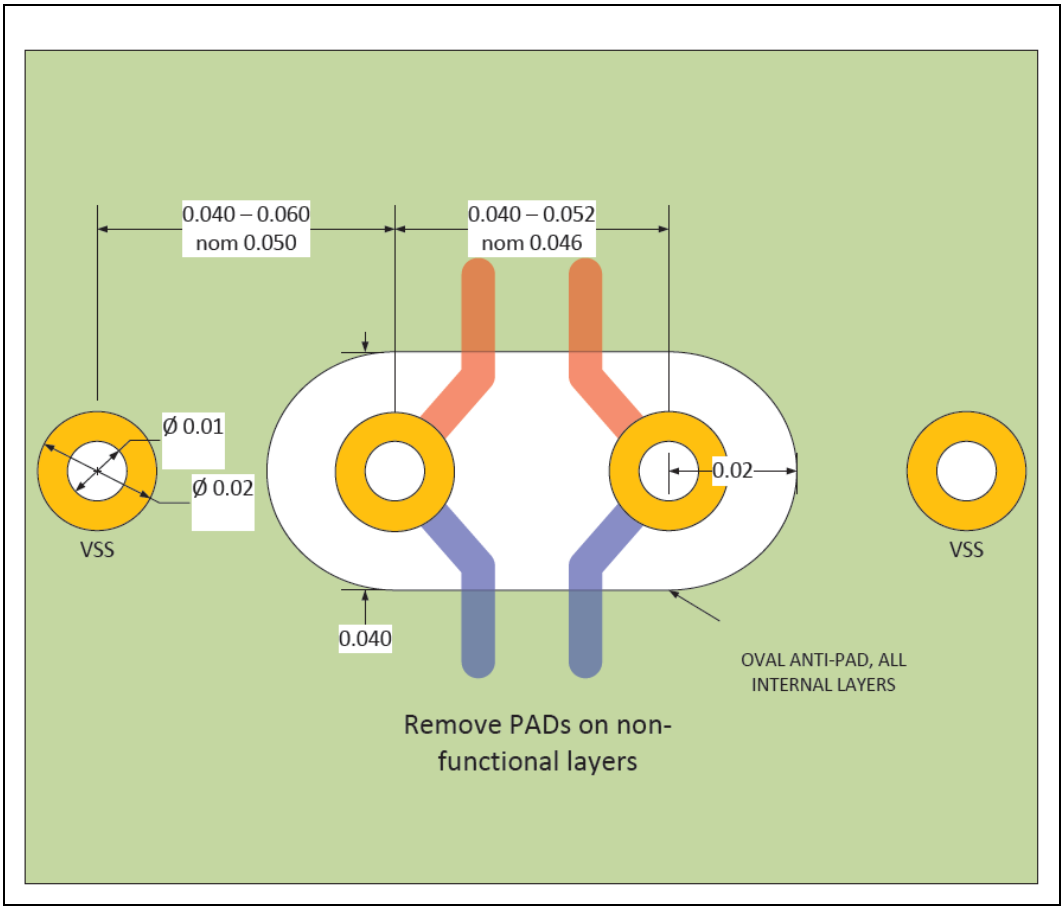
Mitigation techniques for these low impedance reflections should be used in any design, but it is more pertinent at signaling rates of 10 GT/s. The first step in constraining the impacts of via structures is to limit the stub length, which can be accomplished by routing signals from top external layers to near bottom layers and bottom external layers to near top layers. For Harrisonville platforms, the maximum allowed stub is 20 mils. However, depending on the stack up, a standard via geometry (pad and anti-pad size) with a 20 mil stub might not have an impedance response of 100 Ω ± 10%. Additional optimization steps are needed. Starting points or rules of thumb for designing vias to the desired impedance range are in Section 6.4.3, “Reference Planes”. It is always recommended to use a 3D simulation to ensure that the finalized via design meets the impedance requirements.

Additional mitigation techniques for via reflections and long via stubs include back drilling as well as more exotic drilling technologies such as laser drilling, blind, or buried vias. If attempting to mitigate a long stub by adding layers to the routing, care must be taken that the addition of several short stubs does not negatively impact the channel performance.

6.4.2.1.1 General Guidelines for 100 Ω Via

Standard via geometry for drill diameter/pad diameter/anti-pad diameter is 10 mil/20 mil/30 mil. The impedance of such vias can be low even when the stub is limited to 20 mil. As a guide for achieving higher impedances, the anti-pads should be combined in an oval and increased to 2 times the pad diameter (see Figure 6-8). The resulting via is 10 mil/20 mil/40 mil. Typically for these types of signal vias, the center-to-center distance should be between 40 to 52 mils and the center-to-center distance from each signal via to its closest adjacent return path via should also be between 40 and 60 mils. On plane layers, pairs of signal vias should share the same enlarged elliptical or oval (merged) anti-pads.

Figure 6-8. 10GBASE-KR Via



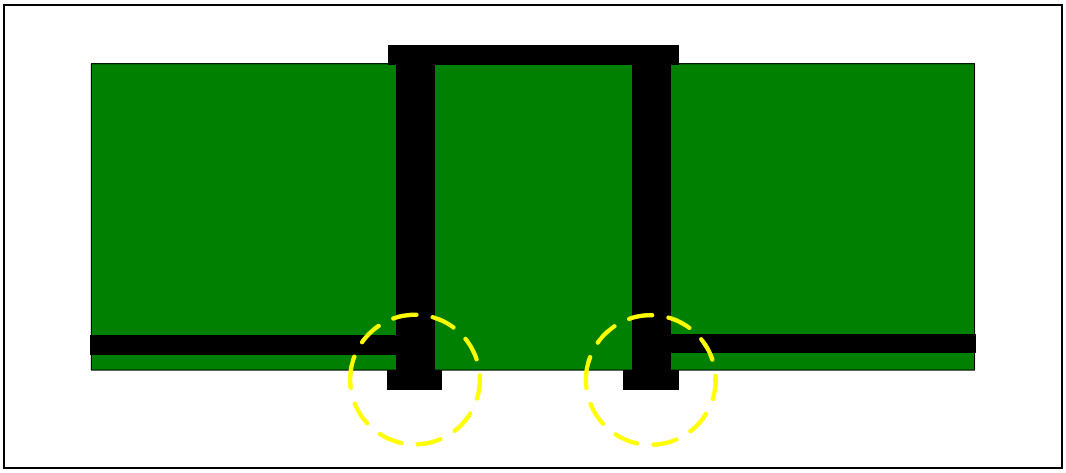
Long via stubs increase channel return loss and insertion loss deviation. It is recommended to limit via stub length to less than 20mils especially on multiple connector topologies. Longer via stubs may be tolerated if the overall channel performance is within IEEE 802.3-2012 Annex 69B frequency domain masks.

Use vias to optimize signal integrity.

Figure 6-9 shows correct via usage.

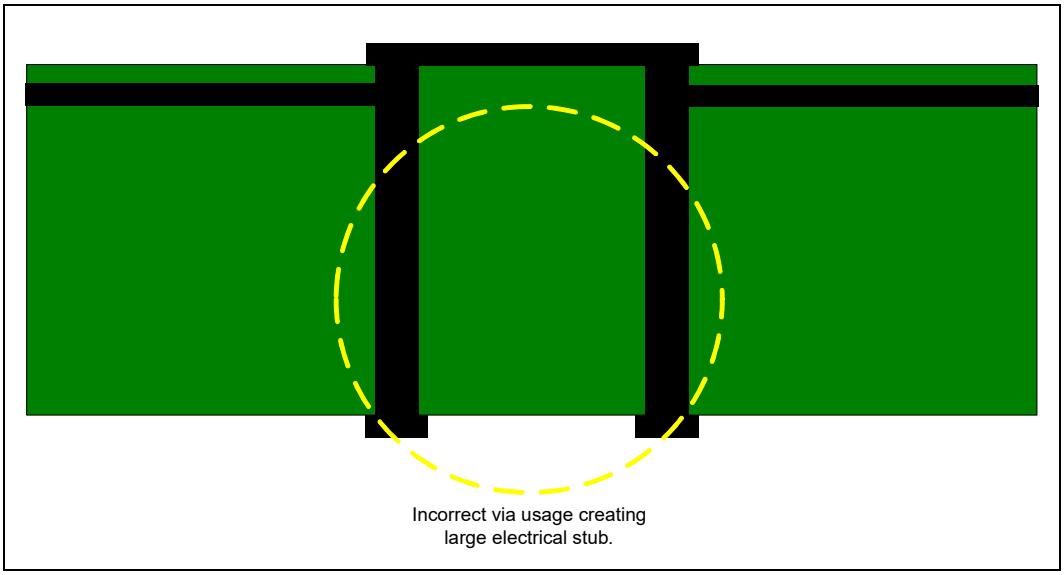
Figure 6-10 shows the type of topology that should be avoided.

Figure 6-9. Correct Via Usage (Stubs < 20 mils)



Any via stubs on the SerDes differential signal traces are recommended to be less than 20 mils in length.

Figure 6-10. Incorrect Via Usage



It is required to remove signal via pads on unconnected metal layers.

See Figure 6-11 and Figure 6-12.

Figure 6-11. For Signal Vias to Have Pads on the Unused Metal Layers (Undesirable)

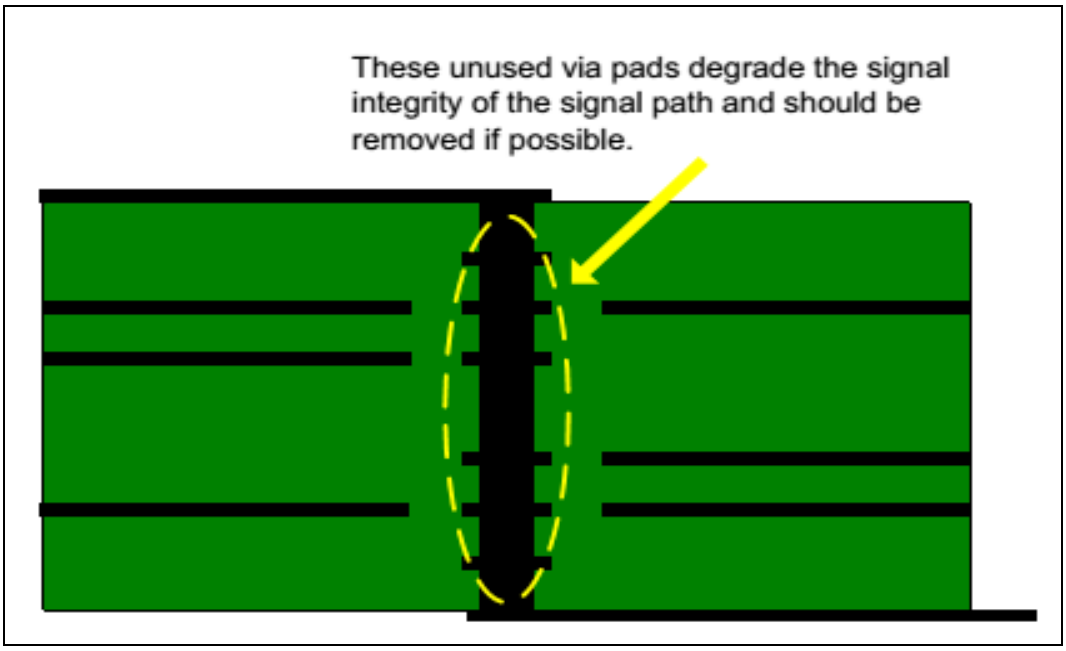
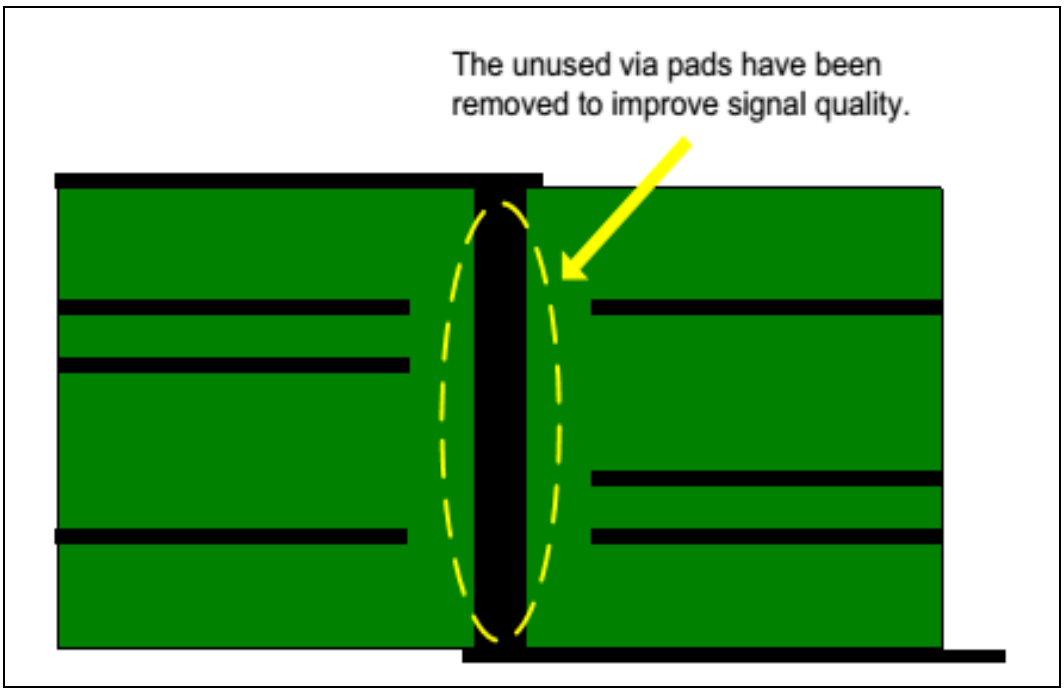
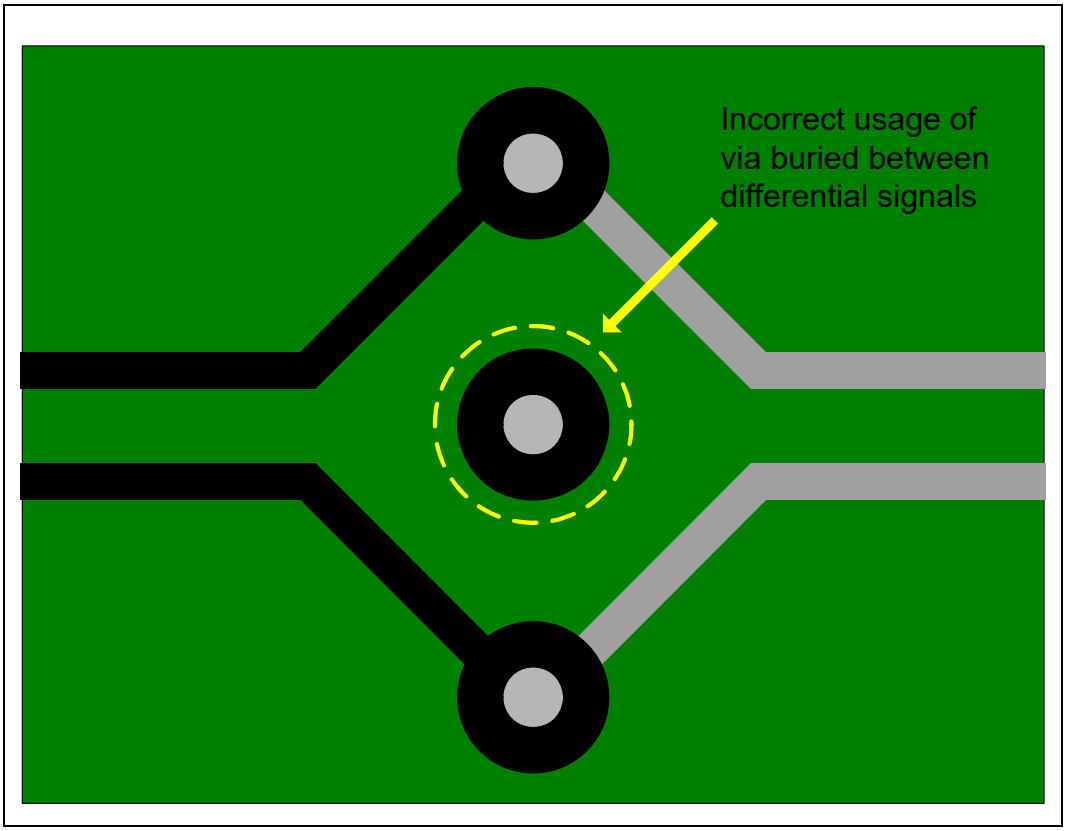


Figure 6-12. Signal Via Improved by Removing Unused Metal Layer Pads



Place ground vias adjacent to signal vias used for the high-speed interface. Do NOT embed vias between the high-speed signals, but place them adjacent to the signal vias (see Figure 6-13). This helps to create a better ground path for the return current of the AC signals, which also helps address impedance mismatches and EMC performance.

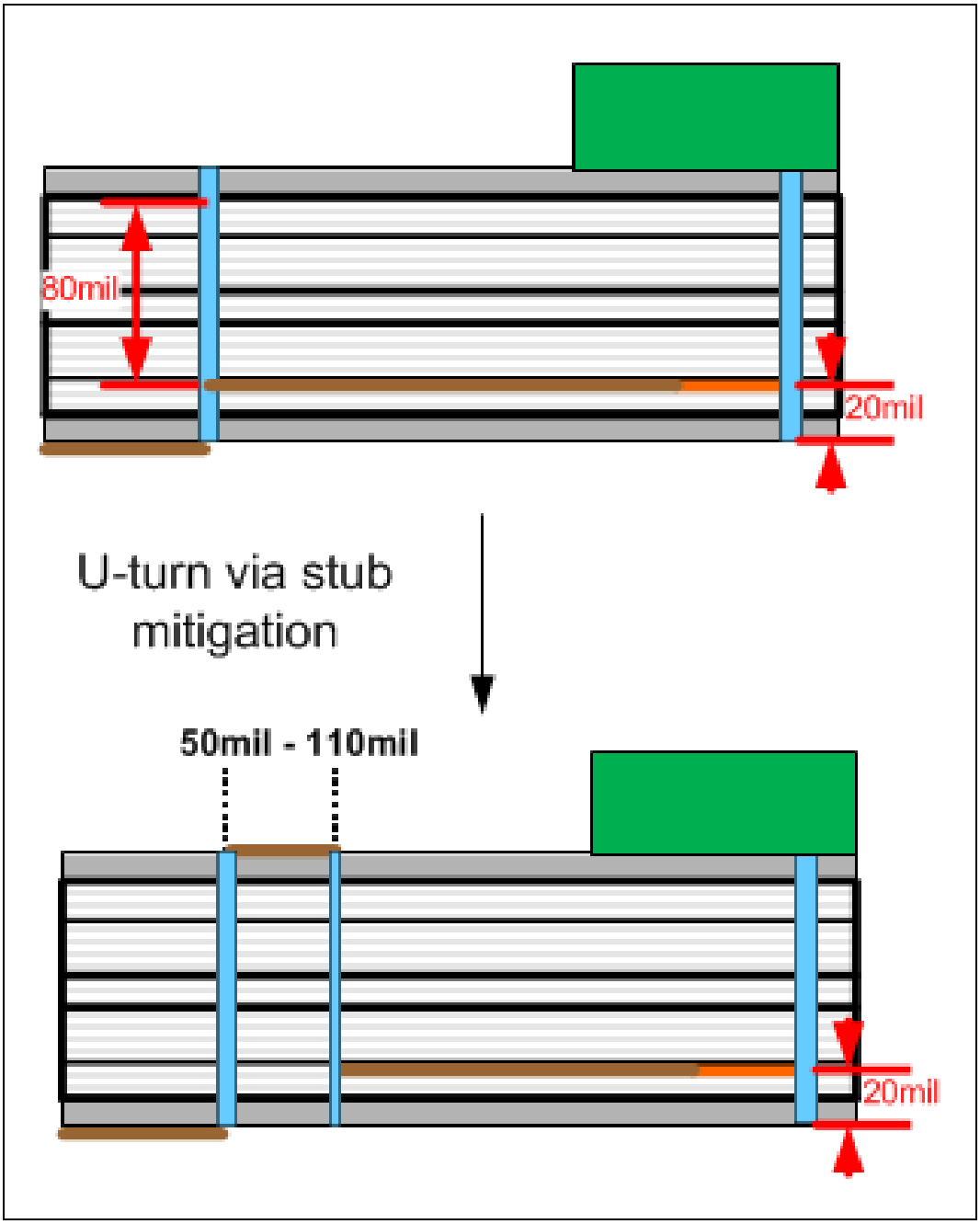
Figure 6-13. No Vias Between High-Speed Traces in the Same Differential Pair



A useful via mitigation technique when routing from the top most layer to the bottom most layer cannot be achieved is referred to here as the u-turn via. Although not as beneficial as backdrilling or exotic drilling techniques, the u-turn via requires placing an additional via in the path near a via with a long stub then connecting these vias with external layer routing. The distance between these vias should be constrained from 50mil to 110mil.

Figure 6-14 shows this technique visually.

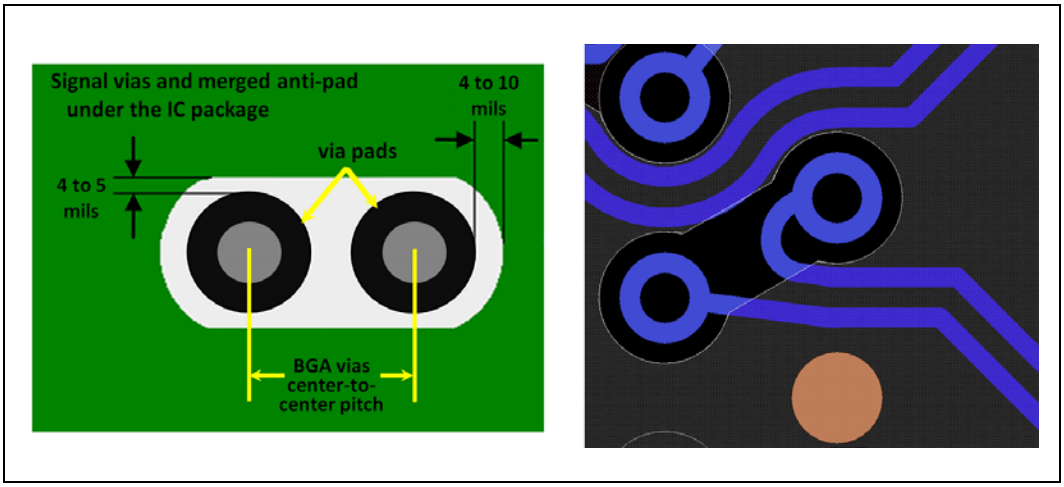
Figure 6-14. U-Turn Via



6.4.2.1.2 Signal Via Anti-pad Voiding under the BGA

Under an IC BGA package, where BGA solder-pads and break-out trace routes may be crowded together, signal via anti-pad clearance might not be able to be 10 mils in all directions. In cases like that, a partially improved shared elliptical anti-pad is a reasonable compromise. Here are two example illustrations:

Figure 6-15. Voiding Recommendations under the BGA



6.4.2.1.3 Transmission Line Impedance

Common industry practice for 10GBASE-KR implementation is to target transmission line impedance of 100 Ω ± 10%. To align with industry and link partner design guidance, the Harrisonville platform is also recommending target transmission line impedance of 100 Ω ± 10%. It should be noted that the underlying assumptions are that the loss targets, impedance variation targets, via stub limits, and via impedance are being followed.

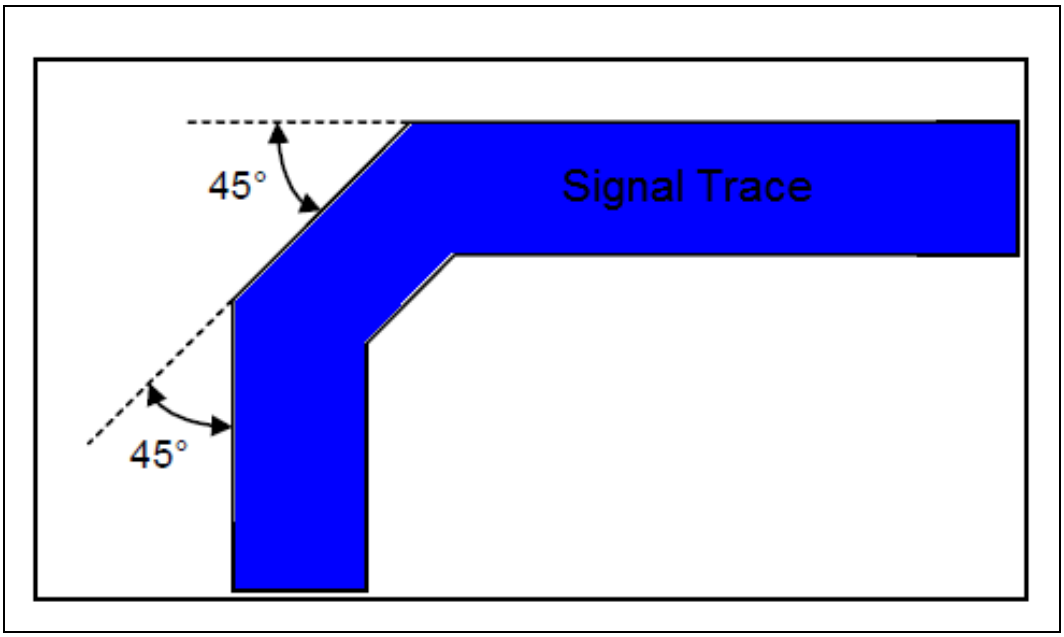
The 10GBASE-KR interface on the Harrisonville platform could support lower nominal differential impedance targets for differential traces and for differential vias, as long as the entire end to end channel continues to perform well with respect to all of the IEEE 802.3-2012 Annex 69B informative channel parameters across manufacturing variations. However, if you are only designing one of the boards in a multi-board 10GBASE-KR signal path and you do not have simulation models for all the other boards and their connectors in the same signal path (as needed to check end-to-end channel conformance) and/or if one or more of the other boards in the channel might later be revised or be replaced, then it is strongly recommended to adhere to 100 Ω ± 10% as the nominal impedance target.

6.4.2.1.4 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Minimize vias (signal through holes) and other transmission line irregularities.

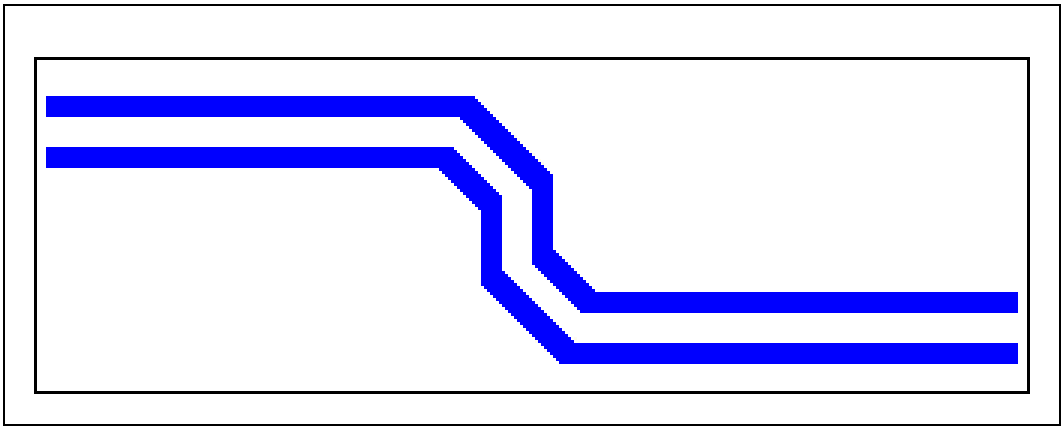
Do not make 90° bends. Bevel corners with turns based on 45° angles. Radius type bends can also be used.

Figure 6-16. Use two 45-degree Angle Bends Instead of One Sharp 90-degree Angle Bend



Symmetry: The traces within each differential pair should be symmetric and in-pair trace-to-trace separation distance should be consistent; except near LAN IC pins and connector pins breakout areas and except where traces within a differential pair need to be corrected for in-pair length mismatch (see Figure 6-17).

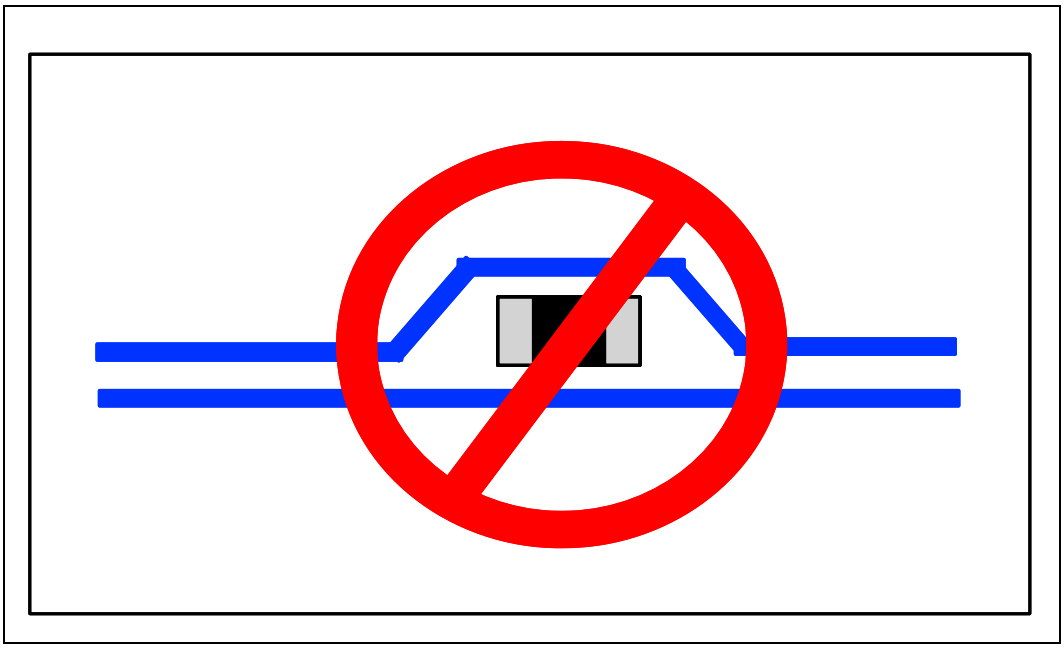
Figure 6-17. Differential Traces Symmetry and Consistent In-pair Separation Example



Make traces as symmetric as possible within each differential pair.

Try to match the pairs at pads, vias and turns. Establish rules carefully if using the auto-router in the CAD. Asymmetry (see Figure 6-18) contributes to signal skew, and decreases the Rx eye opening.

Figure 6-18. Differential Traces Not Symmetric AND Separation is not Consistent Example

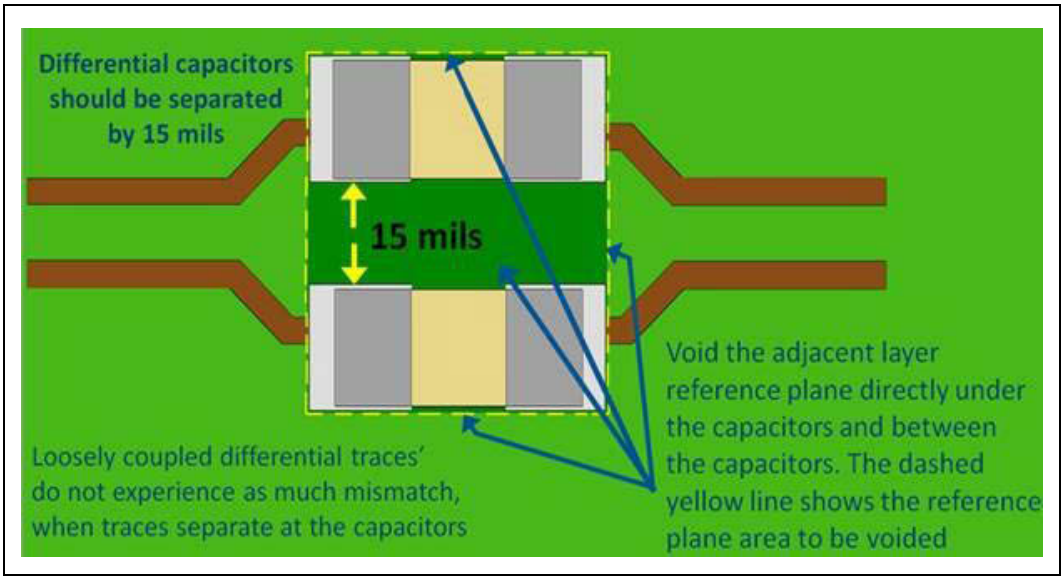


6.4.2.1.5 DC Blocking Capacitors

In cases where there is a via and an AC coupling capacitor on the same trace, the signal trace between the via and the AC coupling capacitors on the high-speed interface, there is an intrinsic impedance mismatch because of the required capacitors.

To reduce shunt capacitance from the AC capacitors' solder-pads to the reference plane beneath the solder-pads, Intel recommends that designers void the reference plane that is directly under the capacitor (see Figure 6-19). The reference plane void should have the same shape as the capacitor and its solder pads. The size of the reference plane void should be slightly larger than the size of the capacitor and it's solder pad. If you have access to a 3-dimensional field solver, it can and should be used to determine the optimal size and shape for the reference plane void under each capacitor. To prevent noise problems, be careful not to route any traces across the capacitor-shaped voids in the reference plane.

Figure 6-19. Capacitor GND Plane Voiding



6.4.2.1.6 High Density Connector (HDC) Pin Out Considerations

To mitigate crosstalk in an HDC, manage the pin assignments carefully. Transmit pairs and receive pairs should be kept in like groups and signal via pins should be separated from other signal pin pairs to minimize coupling. Figure 6-21 shows ground pins between adjacent pairs of signal pins which should significantly reduce the pair-to-pair crosstalk.

Figure 6-21 shows a representative pin assignment that allows more efficient use of the connector pins and has adequate isolation. The "MISC" pins represent static or low speed signals which have lower risk of coupling.

Figure 6-20. High-Isolation KR Connector Footprint

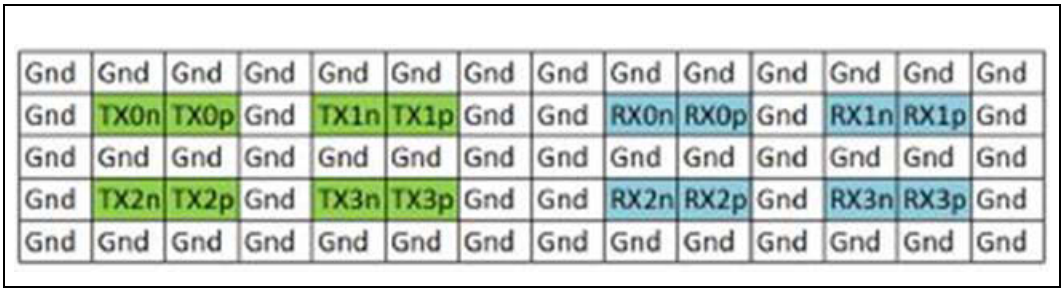
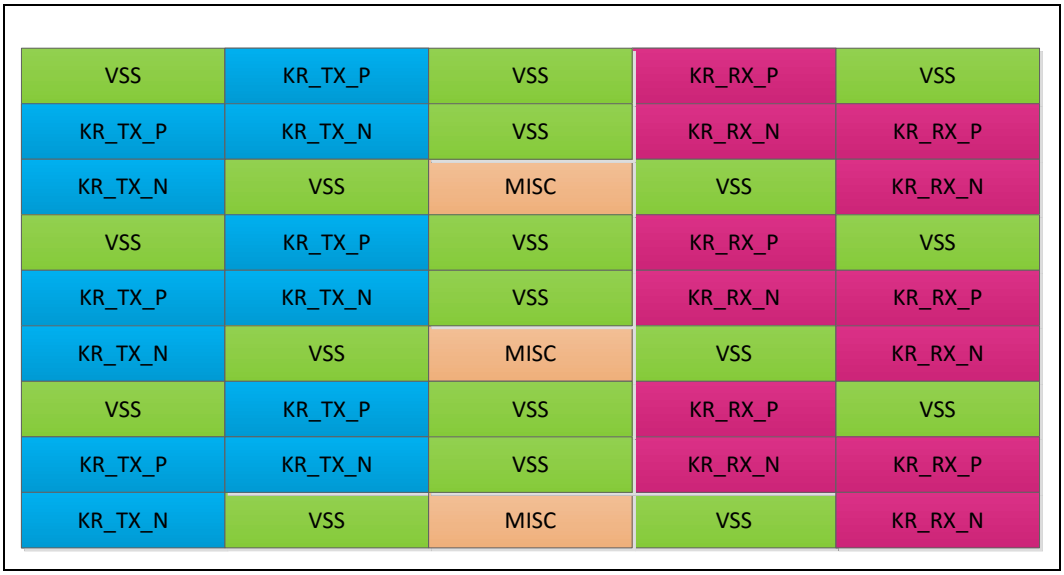


Figure 6-21. High Density KR Connector Footprint



6.4.3 Reference Planes

Do not cross plane splits with the high-speed LAN differential signals. This causes impedance mismatches and negatively affects the return current paths for the board design and layout. Refer to Figure 6-23.

Traces should not cross power or ground plane splits if at all possible. Traces should stay seven times the dielectric height away from plane splits or voids. If traces must cross splits, capacitive coupling should be added to stitch the two planes together in order to provide a better AC return path for the high-speed signals. To be effective, the capacitors should be have low ESR and low equivalent series inductance.

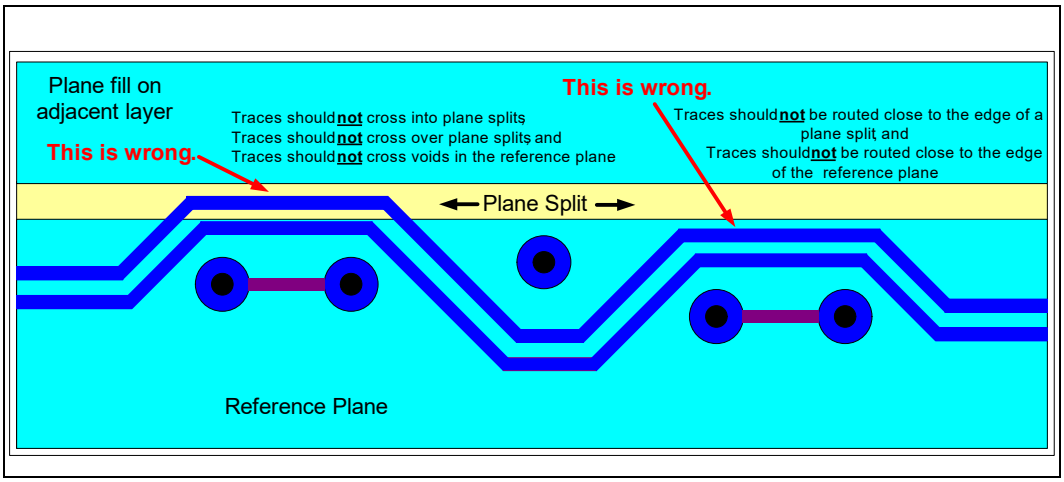
Note: Even with plane split stitching capacitors, crossing plane splits is extremely high risk.

High Speed differential SerDes traces should be kept away from plane splits, voids, and the edge of the reference plane by seven times the thinnest adjacent dielectric height; if the differential traces are near the board edge, differential impedance becomes imbalanced.

Use a quiet reference plane, preferably ground. If the differential traces are placed between a power and ground plane, use an offset stripline structure (like 1H/3H; 1H/4H; 1H/5H, etc.) with the differential traces closer to the ground plane.

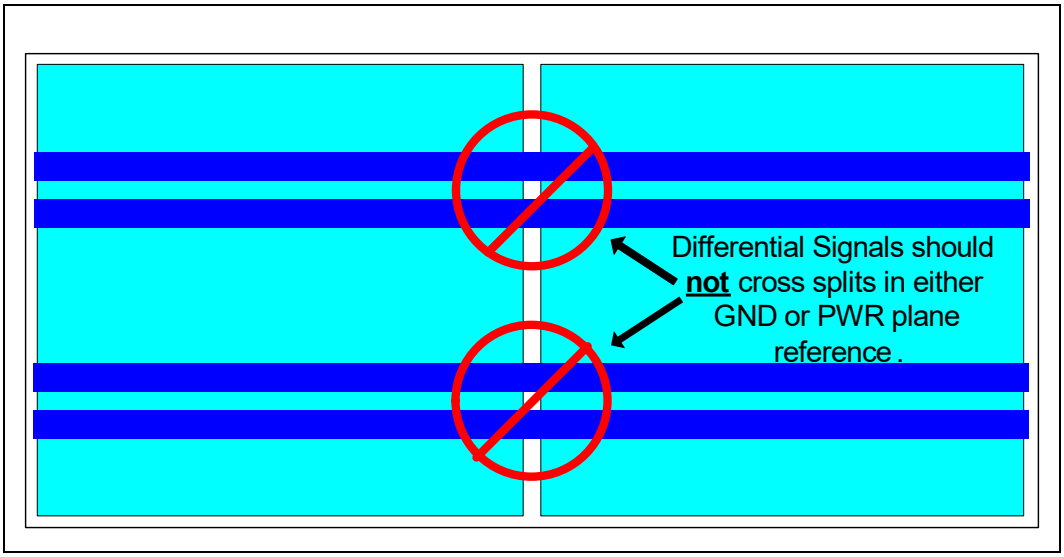
Traces should be routed over a continuous reference plane with no interruptions (see Figure 6-22 and Figure 6-23). If there are vacant areas on a reference plane, the signal conductors should not cross the vacant area. Routing near or over plane voids causes impedance imbalance and/or impedance mismatch, which increases receive sensitivity to noise and might increase the systems' radiated EMI.

Figure 6-22. Reference Plane



Note: Do not route traces over reference plane splits and voids. Also, do not route close to the edge of the reference plane.

Figure 6-23. Do NOT Permit SerDes Traces to Cross Reference Plane Splits



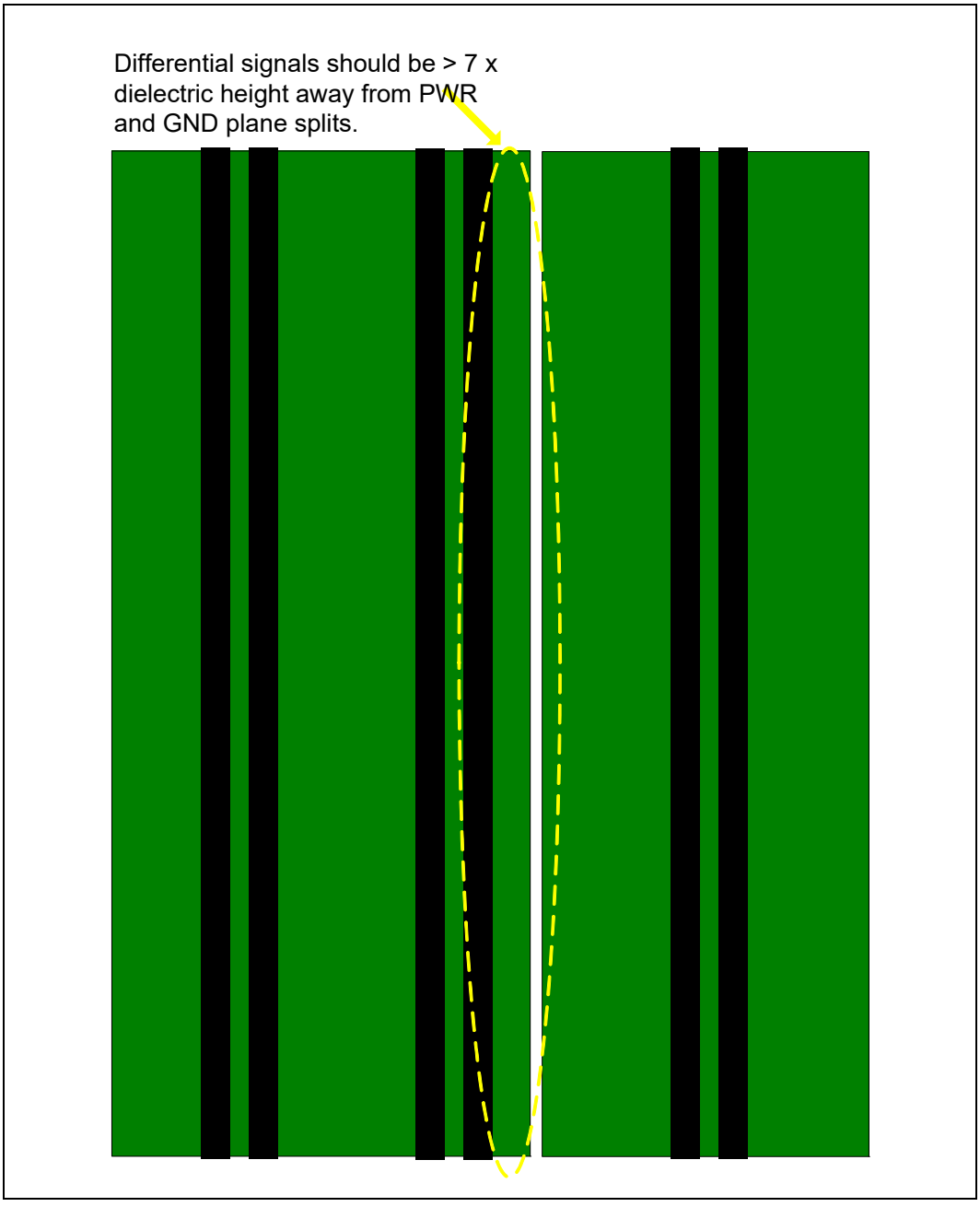
Differential traces should not cross plane splits. If the SerDes traces must cross a plane split, then the ~4.7 nF, X7R or X5R 0402 size SMT capacitors must be used to connect the two reference planes. Coupling capacitors across the plane split must be located symmetrically on either side of the differential pair and must be within 40 mils of the location where the differential traces cross the plane split.

Keep Rx and Tx separate. This helps to minimize crosstalk effects since the Tx and Rx signals are NOT synchronous. This is the more natural routing method and occurs without much designer attention.

Intel recommends that the high-speed signals stay at least seven times the dielectric height away from any power or ground plane split (see Figure 6-24). This improves impedance balance and return current paths.

If a high-speed signal needs to reference a power plane, then ensure that the height of the secondary (power) reference plane is at least three times the height of the primary (ground) reference plane.

Figure 6-24. Traces Should Stay Seven Times the Dielectric Height Away From Plane Splits or Voids



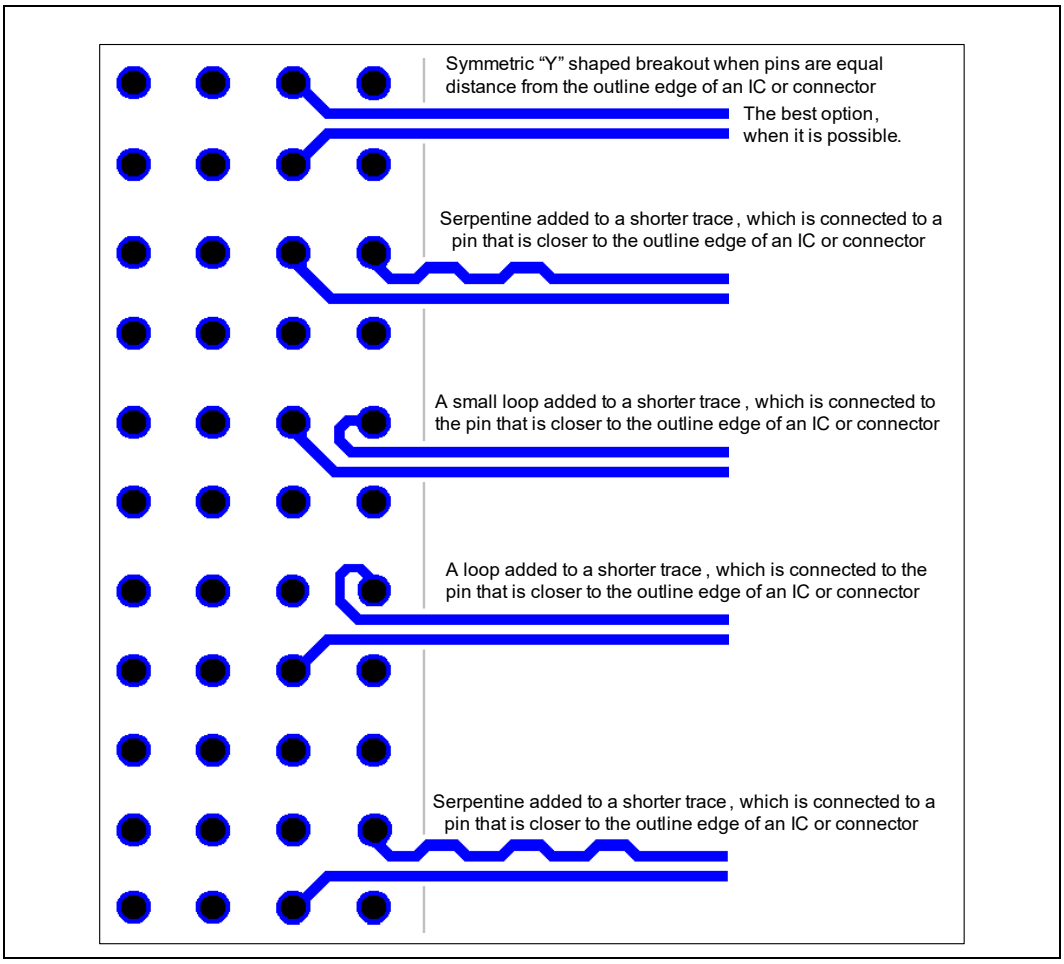
6.4.4 Connector and IC Break-Out Signal Routing and Correcting for In-Pair Skew

Breakout areas are the areas that are usually within 250 mils to 500 mils of LAN IC pins or connector pins.

At the connector and IC pins, it is often difficult to maintain the desired symmetry and in-pair length matching. Sometimes asymmetric trace length compensation is required. Small loops at or near the pins and/or meander lines might be used. For examples that show how this should be done, see Figure 6-25.

It is sometimes necessary to route the in-pair traces closer together in the break-out area and/or within the pin-field of the device or the connector. This is acceptable to do, but the trace widths should be made narrower, to maintain 100 Ω differential impedance in the breakout area. Use a differential trace impedance calculator to determine width and separation.

Figure 6-25. Ways to Match Trace Lengths of Differential Pairs Into or Out of a Device's Pin-field (Break-out Region)



Serpentines (meander lines) can also be used to compensate for in-pair skew that develops when the traces in a differential pair need to make two or more consecutive left turns or two or more consecutive right turns. Skew compensation should happen near the source of the skew; following the source of the skew, in the direction of the signal flow). Where possible, prevent any skew from developing; however, when a skew is not avoidable, then use a serpentine (meander-line) to compensate.

6.4.4.1 Connector Notes

Some right-angle connectors create an in-pair signal skew, because half of the differential signal has a physically longer path through the connector than the other half of the differential signal.

- When using a connector that causes differential signal skew, board designers are responsible to know how much skew is caused by the connector, and then to compensate for that skew by adjusting the differential trace lengths on the circuit board.
  - An application note or Datasheet from the connector vendor might document the amount of connector-caused skew and how to compensate for the connector skew.
  - It might be necessary to contact an Applications Engineer (AE) or Technical Marketing Engineer (TME), who works for the connector manufacturer or connector vendor, to obtain the desired information.
  - Make sure that the connector caused in-pair signal skew is not also being compensated on the mating board. Fully correcting for the same source of skew and the same quantity of connector skew on two mating circuit boards would create an equal but opposite amount of skew in the differential in-pair signal path. Do not make a double compensation mistake. Check the trace routing on the mating board.

6.4.5 Dielectric Weave Compensation

Because the dielectric weave can cause different propagation velocity on each of the traces within one differential pair, Intel recommends using one or more trace routing techniques that can minimize signal skewing caused by the weave:

- Instead of routing traces parallel to either X or Y axis, traces should be routed at an angle to the weave, and the angle should be between 11 and 45 degrees. Routing both traces within each differential pair at an angle, with respect to the dielectric weave, minimizes the signal skew within each differential pair.
- The center-to-center pitch of the traces within the differential pairs can be matched to the weave pitch of the dielectric material. If you plan to uses a woven glass/epoxy dielectric material, check with the material supplier to find out the glass weave pitch prior to doing final differential trace routing.
- Traces can be routed to include a series of 45 degree bends, with bends separated by several tenths of an inch, to shift the traces in steps by a few millimeters each time. There should be an equal number left turns and right turns along the length of the traces. Trace segments between each pair of bends should be different lengths (if they are all the same length it could create an undesirable resonance in the line).
- If differential traces must be straight and orthogonal to the outline of the circuit board for most of their routed lengths, then rotate CAD artwork by 15°, with respect to the weave of the circuit board dielectric weave.

6.4.6 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. Routing over a void in the reference plane causes impedance mismatches and usually increases radiated noise levels. Noisy logic grounds should NOT be located near or under high-speed signals or near sensitive analog pin regions of the LAN silicon. If a noisy ground area must be near these sensitive signals or IC pins, ensure sufficient decoupling and bulk capacitance in these areas. Noisy logic and switching power supply grounds can sometimes affect sensitive subsystems such as analog to digital conversion, operational amplifiers, etc.

All ground vias should be connected to every ground plane; and similarly, every power via should be connected to all equally potential power planes. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible while still meeting the relevant electrical requirements. Because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling and simulation software.

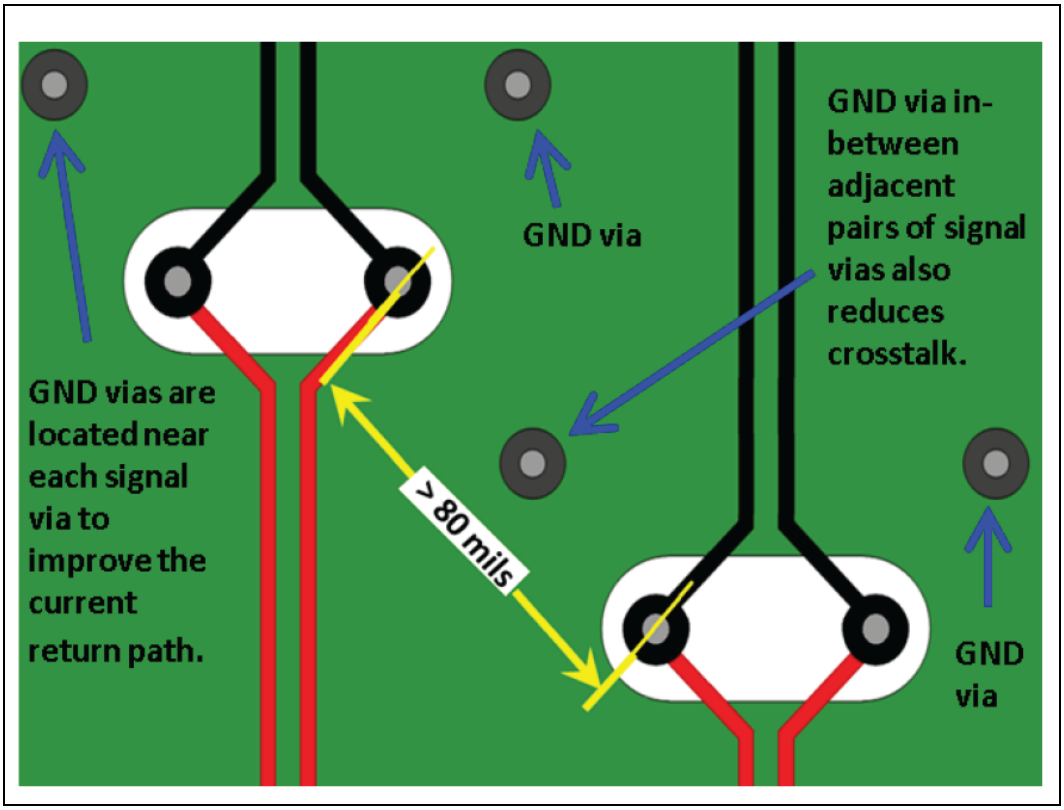
6.4.7 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and locating decoupling capacitors at or near power inputs to bypass to the signal return. This will significantly reduce EMI radiation.

These guidelines reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. Routing signals over power or ground voids increases inductance and increases radiated EMI levels.
- Use distance and/or extra decoupling capacitors to separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- Do not route high-speed signals near switching regulator circuits.
- There should not be any test-point vias or test-point pads on KR and SFI+ traces.
- It’s acceptable to put ground fill or thieving on the trace layers, but preferably not closer than 50 mils to the differential traces and the connector pins.
- If differential traces must be routed on another layer, then the signal vias should carry the signal to the opposite side of the circuit board (to be near the top of the circuit board); AND if the high-speed signals are being routed between two connectors on the same board, then before the signal traces reach the second connector, they must return to the original signal layer (before reaching the connector pin). This strategy keeps via stubs short without requiring back drilling.
- Each time differential traces make a layer transition (pass through a pair of signal vias), there must be at least one ground via located near each signal via. Two ground vias near each signal via might be better. See Figure 6-26.

Figure 6-26. Good Ground Vias for Signal Return Paths – One Return Path Via Per Signal Via



6.4.8 LAN Controller SFI Channel Design Guidelines

This section describes the general design guidelines and outlines the options for implementation of various SFP+ configurations.

6.4.9 SFI Interface Routing

The Pine Lake Platform PLCC-A uses the SFI interface routing to connect the SFI to the XAUI transceiver. Refer to Figure 6-6. The SFI interface uses the microstrip routing.

Figure 6-27. SFI Interface Microstrip Routing

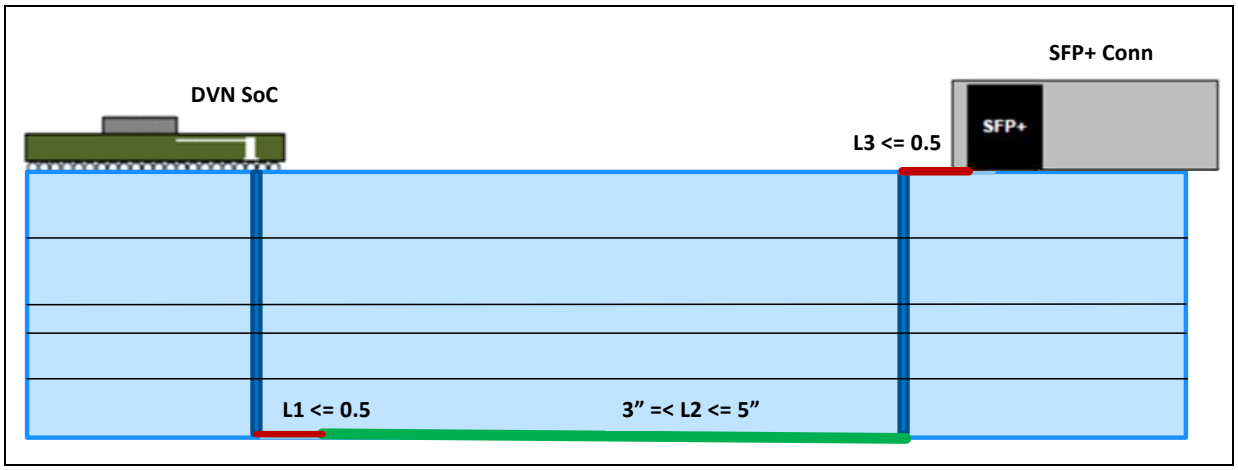


Table 6-8. PLCC-A - Routing Guidelines for SFI Channels

Layout Guideline	Breakout	Microstrip		Units	Notes
Transfer Rate	10.3125			Gb/s	
Interleaved or Non-Interleaved	Non-interleaved preferred				1
Reference Plane	Ground Referenced				
No. of Via Transitions	2				2
Via Stub Length (Maximum)	20	0		mils	4, 5
Max. IL Target @ 4 GHz	0.75			dB/inch	
Layer Assignment		External Layers			
Differential Trace Impedance	Breakout Region	93 ± 10%		Ω	3
Differential Via Impedance	100 ± 10%			Ω	5
Inter-Pair Spacing Like Pairs (Tx to Tx or Rx to Rx)	Breakout Region	24h		mils	6
Spacing to Other Signals (Tx to Rx)	Breakout Region	24h (Route on Separate Layers Recommended)		mils	6
Minimum Channel Length	-	3		inch	8
Maximum Allowed Differential Skew Mismatch	5			mils	9
Maximum Channel Length (Surface Mount)	<=0.5	5 - Breakout	5 - Breakout	inch	7

Notes:

1. The Rx signals should be restricted to internal routing only, but if microstrip routing is absolutely necessary, then the pair-to-pair spacing of 24h or wider should be used to reduce cross-talk.
2. Intel recommends to keep layer transitions to a minimum. A max. of two vias are recommended for a board.
3. See Stack-Up Reference in Stack-up Section.
   a. Trace widths > 4.5 mils are preferred. Thick dielectrics and wider traces can decrease PWB loss. Note that tight impedance tolerances especially on an external layer may add cost to your stack-up.
   b. Intra-pair separation should be < 3.5w, where w is the trace width. For thin dielectrics, 2w to 3.5w intra-pair separation may be required to be able to achieve 93 Ω nominal to have reasonable trace widths. The *SFF-8431 Specification* recommends 7% differential coupling for transmission lines.
4. The via stub is the remaining barrel of the via from the signal layer to the bottom of the board.
5. Intel recommends that layer transition vias (outside the BGA area) be designed to a 100 Ω differential (assuming a 30ps rise time) using a 3D solver. In Section 6.4.3, "Reference Planes", reasonable "rule of thumb" guidelines for obtaining a 100 Ω differential are given. Note that failing to remove pads on unused layers will be detrimental to via performance.
6. The "h" is the dielectric height between the signal and the nearest reference ground plane.
7. Long microstrip routing is not recommended due to greater performance variation vs. routing length. e.g., material properties of solder mask and silk screen printing, increased impedance tolerance, reduced noise tolerance, increased risk for EMI, impedance mismatch from external component placement.
8. Short routing from the SoC to the SFP+ connector may cause normative return loss violations in SFF-8431.
9. Refer to Chapter 2, "Platform Stack-up and General Design Considerations" for more details.

Note: Intel recommends that the board design comply with the following recommendations:

- The cross-talk requirement for microstrip signals should be -40 dB or better from dc to Nyquist.
- The cross-talk requirement for mixed media type (i.e., optical and copper) is -50 dB or better from dc to Nyquist.
- SFI traces should be routed on a single layer. Use of multiple layer transitions will cause Tx compliance failures.
- Impedance discontinuities should be designed within 100 mils of each other. The capacitor, for example, should be placed within 100 mils of the via transition.

6.4.9.1 Integrated LAN Controllers SFP+ Layout Guidelines

SFP+ connections are implemented using the following layouts. Both single height and dual stack connectors are allowed.

Figure 6-28. SFP+ Surface Mount Cage Stripline Topology

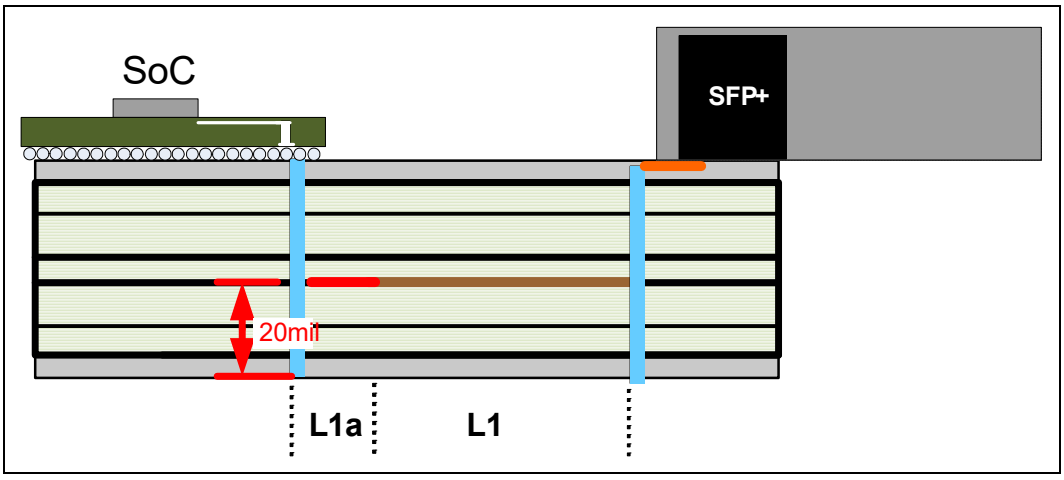


Figure 6-29. SFP+ Through Hole Mount Cage Stripline Topology

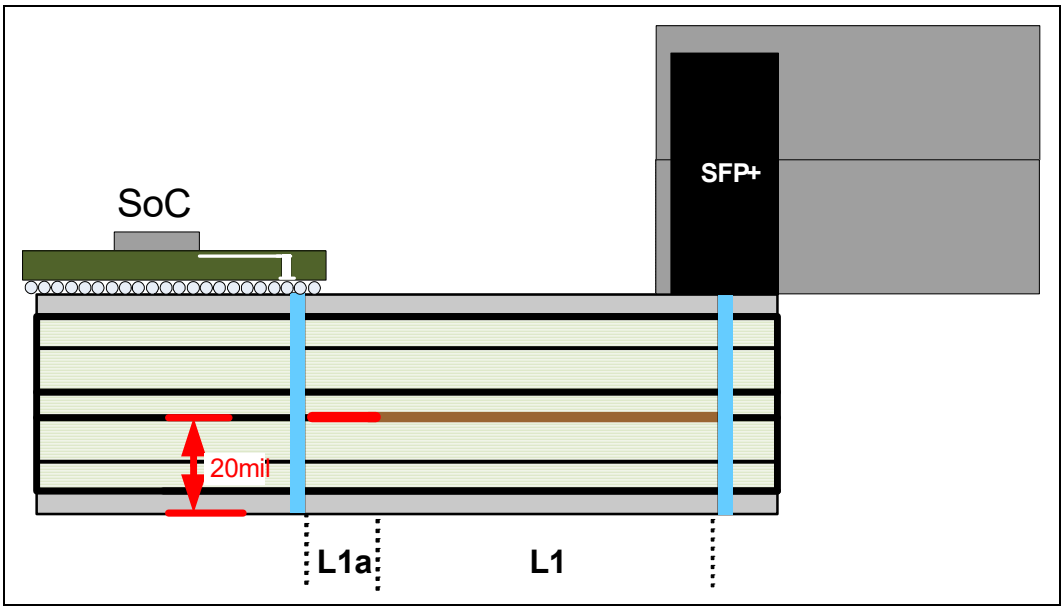


Table 6-9. Routing Guidelines for SFI Channels

Layout Guideline	Breakout	Stripline	Microstrip	Units	Notes
Transfer Rate	10.3125			Gb/s	
Interleaved or Non-Interleaved	Non-Interleaved				1
Reference Plane	Ground Referenced				
No. of Via Transitions	2				2
Via Stub Length (Maximum)	20			mils	4, 5
Max IL Target @ 4 GHz	0.65			dB/inch	10
Layer Assignment		Internal Layers	External Layers		
Differential Trace Impedance	Breakout Region	93 ± 10%	93 ± 10%	Ω	3
Differential Via Impedance	100 ± 10%			Ω	5
Inter-Pair Spacing Like Pairs (Tx to Tx or Rx to Rx)	Breakout Region	5h	12h Tx Only	mils	6
Spacing to Other Signals (Tx to Rx)	Breakout Region	7h (Route on Separate Layers Recommended)	Not Recommended	mils	6
Minimum Channel Length	-	3		inch	8
Maximum Allowed Differential Skew Mismatch	5			mils	9
Maximum Channel Length (Surface Mount)	<=0.5	6 - Breakout	6 - Breakout	inch	7

Notes:

1. The use of micro-strip routing is recommended only for Tx signals. Inter-leaved routing is not allowed on external layers. The Rx signals should be restricted to internal routing only, but if microstrip routing is absolutely necessary then the pair to pair spacing of 24h or wider should be used to reduce cross-talk.
2. It is recommended to keep layer transitions to a minimum. Routing on two layers is highly discouraged except to break-in to a surface mount connector. In this case, the routing should be kept less than 0.5.
3. See Stack-Up Reference in Section 2.2, "General Signal Design Considerations".
   a. Trace widths > 4.5 mils are preferred. Trace widths < 3.5 mils can be adequate, provided the insertion loss requirements and impedance tolerances are met across HVM. Thick dielectrics and wider traces can decrease PWB loss. Note that tight impedance tolerances especially on external layer may add cost to your stack up.
   b. Intra-pair separation should be < 3.5w, where w is the trace width. For thin dielectrics, 2w to 3.5w intra-pair separation may be required, to be able to achieve 93Ω nominal, and to still have reasonable trace widths. The SFF-8431 specification recommends 7% differential coupling for transmission lines.
4. Via stub is the remaining barrel of the via from signal layer to bottom of board.
5. It is recommended that layer transition vias (outside the BGA area) be designed to 100 Ω differential (assuming a 30 ps rise time) using a 3D solver. In Section 6.4.2.1.1, "General Guidelines for 100 Ω Via", reasonable "rule of thumb" guidelines for obtaining a 100Ω differential are given. Note that failing to remove pads on unused layers will be detrimental to via performance.
6. "h" - dielectric height between signal and the nearest reference ground plane.
7. Long microstrip routing is not recommended due to greater performance variation vs. routing length. Ex: Material properties of solder mask and silk screen printing, increased impedance tolerance, reduced noise tolerance, increased risk for EMI, impedance mismatch from external component placement.
8. Short routing from the LBG to the SFP+ connector may cause normative return loss violations in SFF-8431
9. Reference Chapter 2, "Platform Stack-up and General Design Considerations" for more details.
10. If 0.75dB/inch at 4 GHz is used expect a maximum length adjustment of 0.87. A 6" maximum length, for example, will decrease to about 5.2".

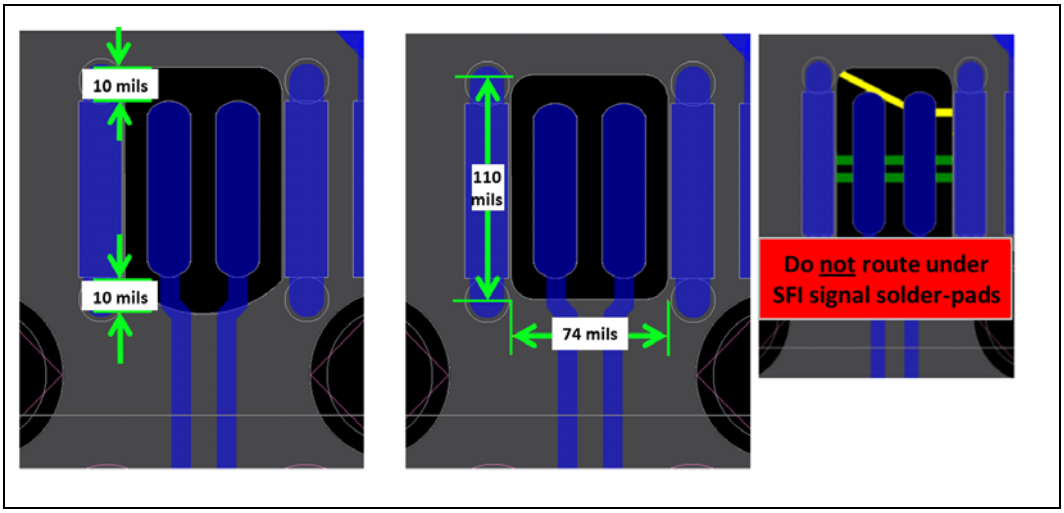
Note: It is highly recommended that the board design comply with the following recommendations

- Cross-talk requirement for microstrip signals should be -40dB or better from dc to Nyquist.
- Cross-talk requirement for mixed media type (i.e. optical and copper) is -50dB or better from dc to Nyquist.
- SFI traces should be routed on a single layer. Use of multiple layer transitions will cause Tx compliance failures. If surface layer routing (microstrip) is used for less than 0.5" to break-in to a surface mount connector, the traces are still considered to be on a single layer.
- Impedance discontinuities should be designed within 100 mils of each other. The capacitor, for example, should be placed within 100 mils of a via transition.

6.4.9.2 SFP+ Surface Mount Connector Pad Design Guidelines

Voiding Recommendations for surface mount SFP+ connectors.

Figure 6-30. SFP+ Native SFI Implementation



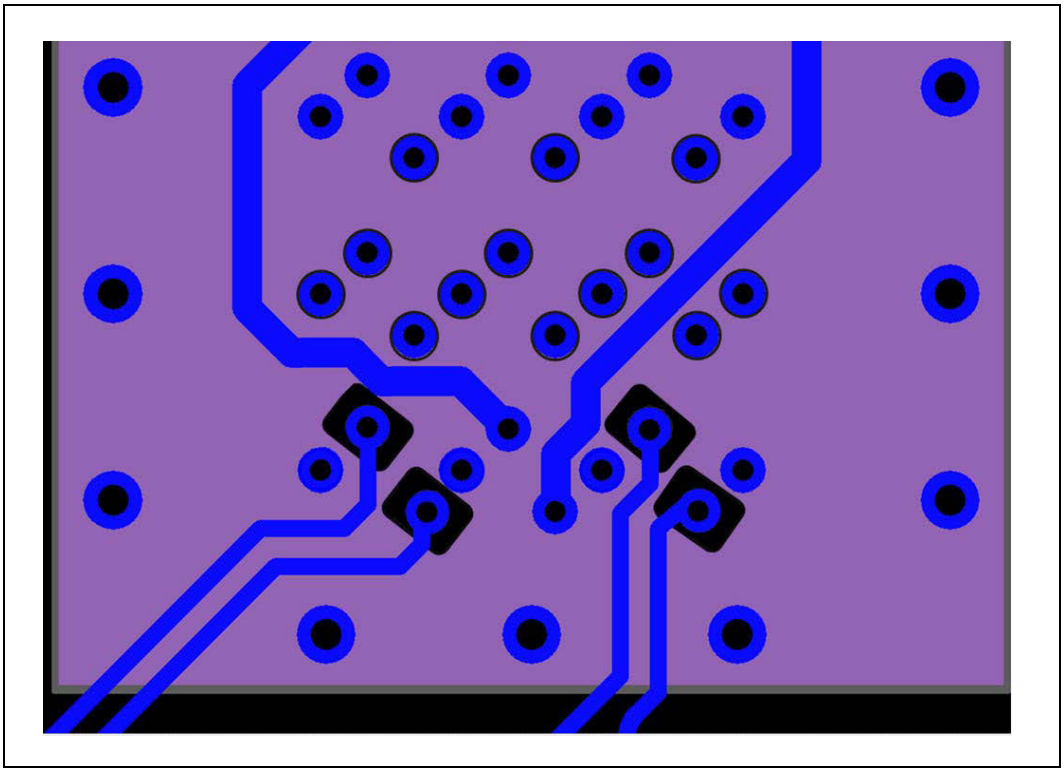
- If surface mount SFP+ connectors are used, the reference plane area directly under each pair of SFP+ module connector signal pin solder-pads must be voided as shown in figure below.
- Avoid sharp corners.
- Void multiple layers, at least 2 layers (20 mils or more to the reference plane). >=40 mils vertical clearance is recommended.
- Do not route any signals under plane voids.
- Add one GND via at each end of the surface mount SFP+ connectors ground pin solder pads.
- Simulations show that added another ground via at the opposite end of each ground pin solder pad eliminates undesirable resonance at 16 GHz (third harmonic of the SFI fundamental frequency).

6.4.9.3 SFP+ PTH Pad Design Guidelines

An important criteria for the reference plane voids is that the plated-through hole (PTH) differential impedance should be ~100 Ω differential. For SFP+ PTH connectors, the signal pins PTH pads should have an average of >=10 mils clearance to the reference planes, under the connector. Without >=10 mils clearance between signal pin pads and the reference planes, the signal pins will have excessively low impedance. The reference plane voids may be round, oval, rectangular, or another shape.

Use connector vendor validated and recommended PTH anti-pads or anti-pads similar to Figure 6-31.

Figure 6-31. Voiding Recommendations for SFP+ PTH Connectors

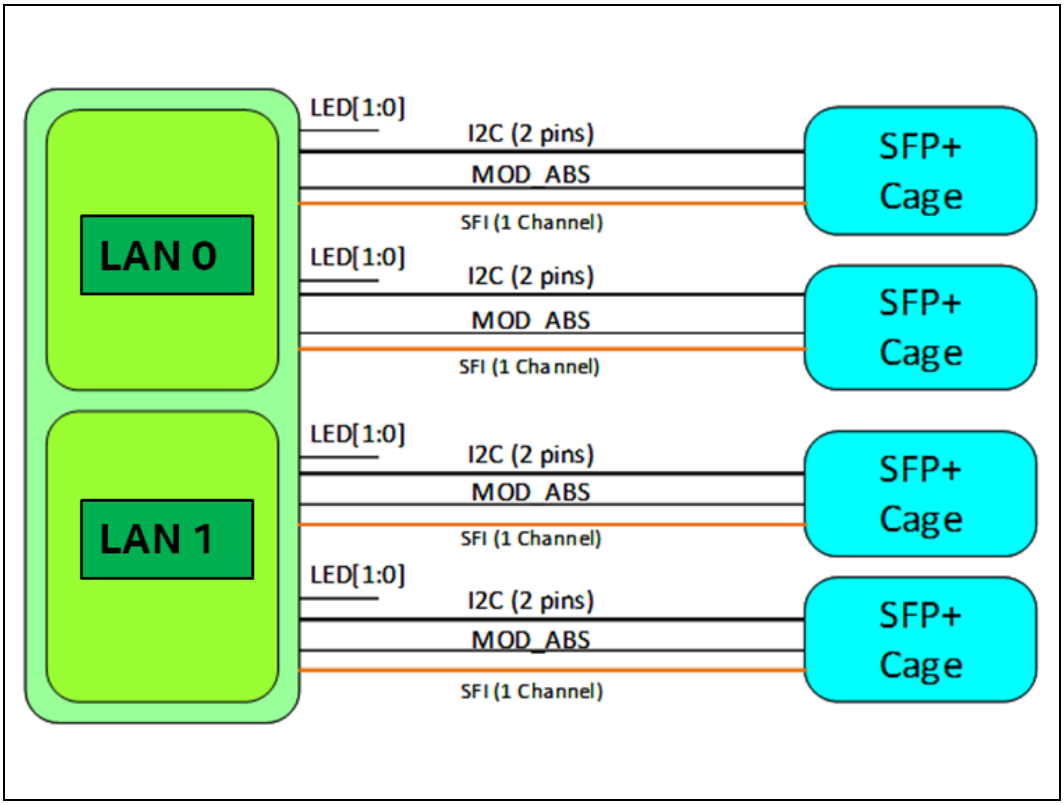


6.4.9.4 SFI+ Connectivity Configurations

The following diagrams illustrate the high and low speed digital signals used when connecting PCH to SFP+ modules.

6.4.9.4.1 SFP+ Connectivity Configurations Native SFI

Figure 6-32. SFP+ Native SFI Implementation



6.4.9.4.2 Low Speed Signal Configuration for SFP+ Modules

The strapping for the SFP+ cage signals are outlined below and essential for proper operations of the Ethernet controller and the module.

Table 6-10. Low Speed Signal Configuration for SFP+ Modules

Low Speed Signals (SFP+ Module)	Pull-up / Pull-down
TX_Fault	Pull-up to V_{CC}_Host for range between 4.7 kΩ to 10 kΩ
TX_Disable	Pull-down to GND for range between 4.7 kΩ to 10 kΩ
RS0	Pull-down for signaling rate less than 4.25 GBd. (for more details please refer to Spec. SFF-8431)
RS1	Pull-down for signaling rate less than 4.25 GBd. (for more details please refer to Spec. SFF-8431)
RX_LOS	Can be N/C

6.4.10 1000BASE-KX/2500BASE-X/10GBASE-KR Layout Recommendations

This section provides recommendations for routing the high-speed interface. These layout guidelines can also be applied to 1000BASE-KX and 2500BASE-X.

- For SGMII channel design use IEEE802.3 Annex 69B for 1000BASE-KX

The following section contains layout practices that helps facilitate meeting the IEEE 802.3-2012 Annex 69B informative channel parameters. Any of the following guidelines may be violated if the entire pin-to-pin channel can be shown to have adequate margin to the channel parameter limits (found in Appendix A, "10GBASE-KR Annex 69B Informative Channel Parameters") across simulated HVM corners.

6.4.11 10GBASE-KR Channel Design Guidelines

6.4.11.1 Summary of 10GBASE-KR Layout Guidelines

Table 6-11. Length Assumptions for 10GBASE-KR Topology

Layout Guideline	Breakout	Stripline	Microstrip	Units	Notes
Transfer rate	10.3125			Gb/s	
Interleaved or non-interleaved	Non-interleaved				1
Reference plane	Ground referenced				
No. of via transitions	2				2
Via stub length (max)	20			mils	4, 6
Max IL target @ 4 GHz	0.48			dB/inch	
Layer assignment		Internal layers	External layers		3
Differential trace impedance	Breakout region	100 ± 10%	100 ± 10%	Ω	
Differential via impedance	100 ± 10%			Ω	6
Inter-pair spacing like pairs (Tx-to-Tx or Rx-to-Rx)	Breakout region	5*h*	12*h*	mils	7
Spacing to other signals (Tx-to-Rx)	Breakout region	7*h* (route on separate layers recommended)	15*h* (route on separate layers recommended)	mils	7
Maximum Allowed Differential Skew Mismatch per Board (Figure 7-33)	5			mils	12
Maximum Allowed Differential Skew Mismatch pin-to-pin	15			mils	12
Min. trace length	-	3	3	inch	9
Max channel length	<=0.25	28 - Breakout	28 - Breakout	inch	8, 9

Notes:

1. Non-interleaved = TxTxTx or RxRxRx; Interleaved = TxRxTxRx.
2. It is recommended to keep layer transitions to a minimum. Assuming a 3-connector topology, two vias are assumed on every board except the switch card.
3. For the majority of reference stack-ups on PCBs where the PCH resides, Intel has determined that a lower impedance target of 93 Ω (± 10%) can be used for 10GBASE-KR routing to accommodate >=4.5 mil trace widths, which are generally more manufacturable (easier to maintain ± 10% impedance tolerances) than <4.5 mil trace widths. See Stack-Up reference in Section 2.2, "General Signal Design Considerations".
   a. Intel is not recommending that other boards in the 10GBASE-KR signal path use 93 Ω routing.
   b. The 10GBASE-KR link partner manufacturer should be engaged with 10GBASE-KR routing decisions.
   c. 100 Ω ± 10% tolerance 10GBASE-KR traces are also supported for these PCH board applications even if the traces are narrower than 4.5 mils, provided the traces also meet the insertion loss requirements.
   d. For 93 Ω to 100 Ω differential traces, intra-pair separation will typically be 2w to 3.5w - where w is the trace width- to achieve target impedance and still have reasonable trace widths.
4. Via stub is the remaining barrel of the via from signal layer to the bottom of the board.
5. See PCB Loss requirements in Chapter 2, "Platform Stack-up and General Design Considerations".
   a. For boards with maximum routing length of less than 2 inches to 3 inches, the standard material loss found in Chapter 2, "Platform Stack-up and General Design Considerations" should be considered to help mitigate non-attenuated reflections from electrically close components.
6. It is recommend that layer transition vias be designed to 100 Ω differential (assuming a 30 ps rise time) using a 3D solver. In Section 6.4.3, "Reference Planes", reasonable rule of thumb guidelines for obtaining a 100 Ω differential are given. Note that failing to remove pads on unused layers is detrimental to via performance.
7. *h* - dielectric height between signal and the nearest reference ground plane.
8. Long microstrip routing is not recommended due to greater performance variation vs. routing length. Example: Material properties of solder mask and silk screen printing, reduced noise tolerance, increased risk for EMI, impedance mismatch from external component placement.
9. KR trace routing on boards not containing a Tx or Rx device should have routing > 3 inches. Boards that have a Tx or Rx device and have low loss material are recommended to keep routing > 2 inches.
10. Maximum physical lengths can be increased or decreased as long as the overall channel specification limits shown in Appendix A, "10GBASE-KR Annex 69B Informative Channel Parameters" are not violated.
11. All guidelines in Chapter 2, "Platform Stack-up and General Design Considerations", General High-Speed Signal Guidelines should be followed. These KR section rules take precedent over (override) general HSD rules in all cases where there are conflicts.
12. Reference Chapter 2, "Platform Stack-up and General Design Considerations" for more details.

6.4.11.2 Topology of 10GBASE-KR with Three Connectors

Table 6-12. Length Assumptions for 10GBASE-KR (Entire Channel)

Layout Guideline	L1a	L1	L2	L3	L4	L5	L5a	Total	Units
Layer Assignment	Stripline								
Max Length	0.25	3.0	14	8	0.5	4.25	0.25	28	inch
Min Length	0	1.5	3	3	0	3.5	0.25	10	inch

Figure 6-33. 10GBASE-KR Tx Topology

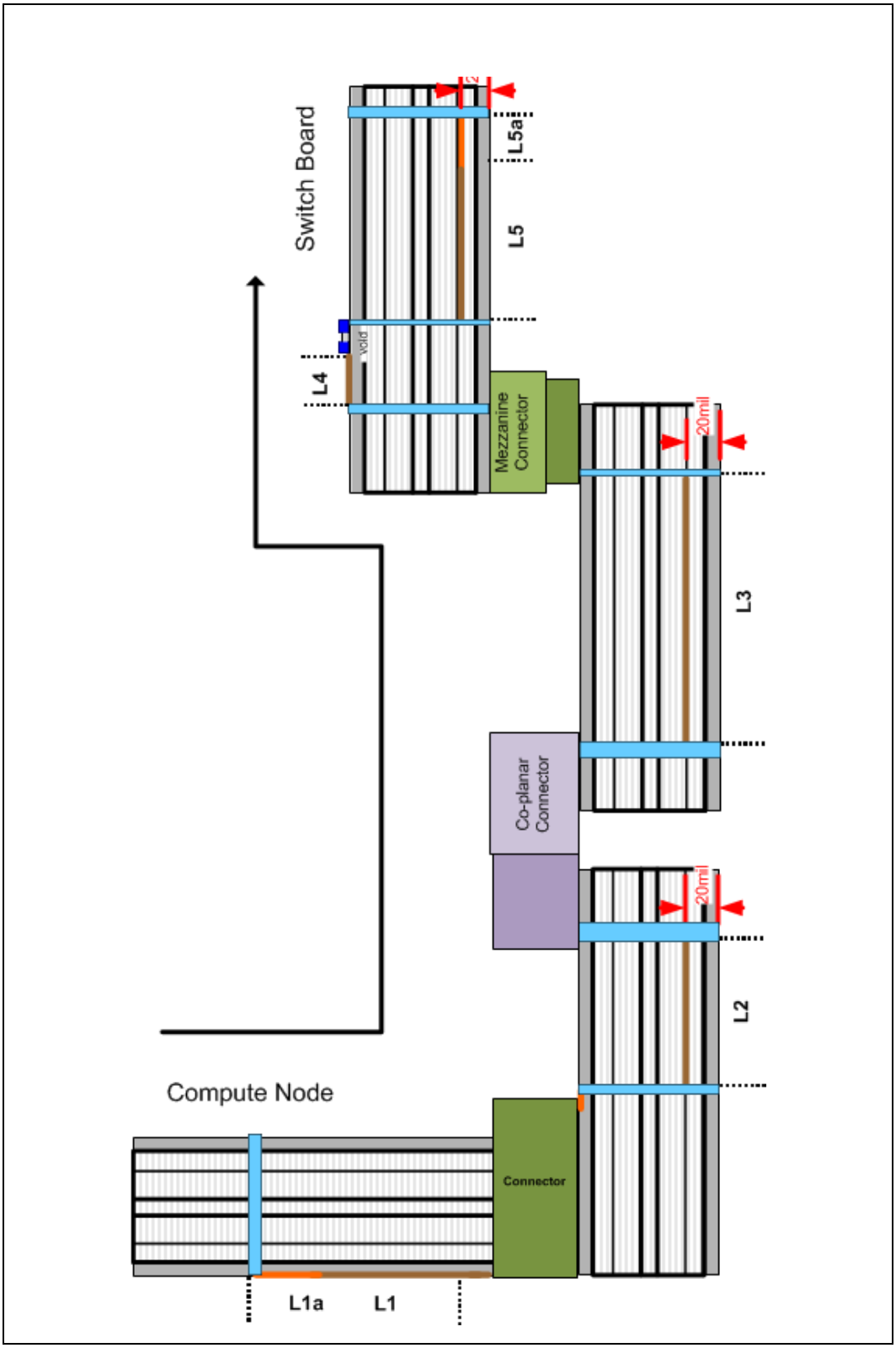
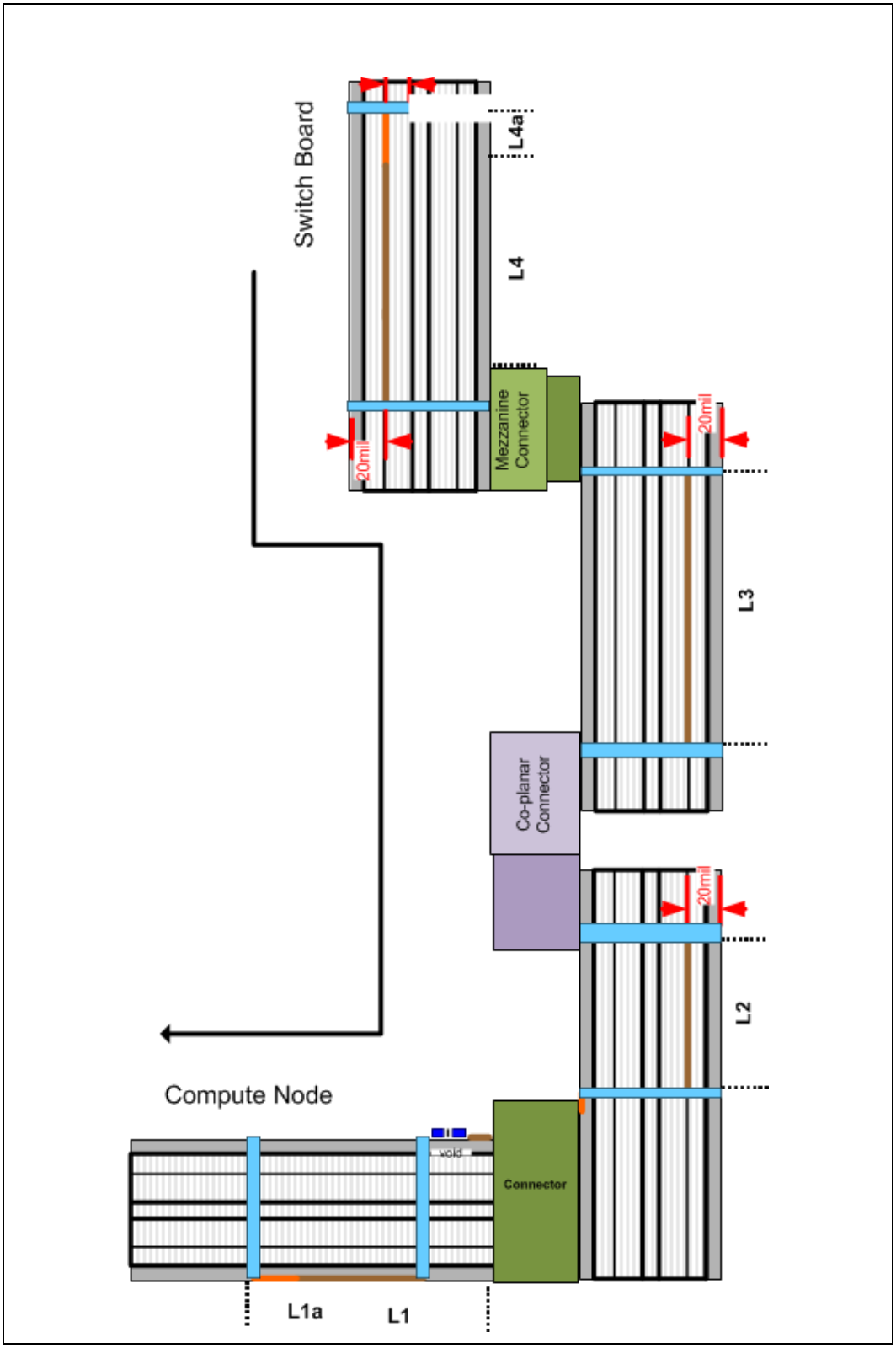


Figure 6-34. 10GBASE-KR BASE Rx Topology



6.5 Sideband Signals

The following sideband interfaces are available for the integrated LAN controller:

- Shared SPI (Serial Peripheral Interface) Flash NVM (Refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* section 13.8 for more details.)
- SMBus
- Network Controlled Side-band Interface (NC-SI)
- Software-definable Pins (SDPs)
- Management Data Input/Output (MDIO)/LED Interface
- I^2C

Refer to Table 6-7, "Network Data Interface Pin Names/Descriptions" for the sideband signal names.

6.6 Connecting Manageability Interfaces

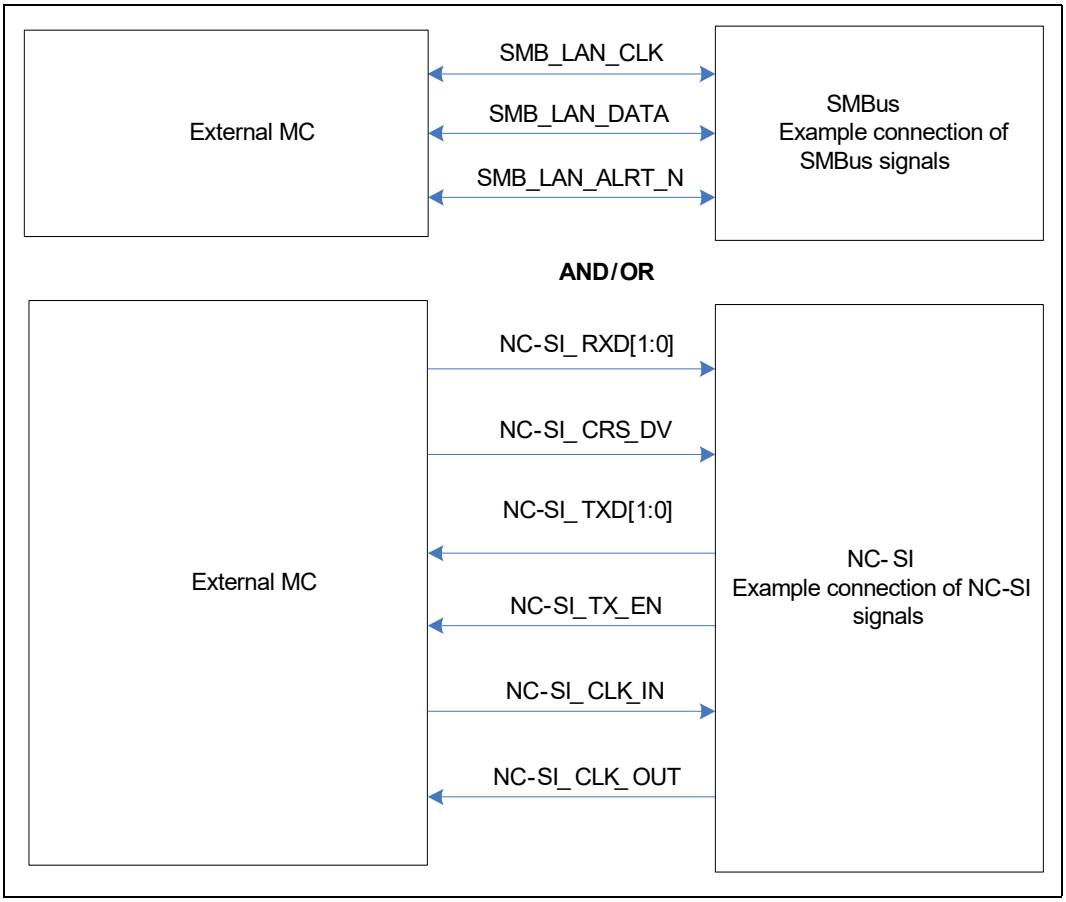
SMBus and NC-SI are interfaces for pass-through and configuration traffic between the Management Controller (MC) and the integrated LAN controller.

The integrated LAN controller can be connected to an external MC. It operates in one of two modes:

- SMBus mode
- NC-SI mode

The clock-out (if enabled) is provided in all power states (unless the device is disabled).

Figure 6-35. External MC Connections with NC-SI and SMBus



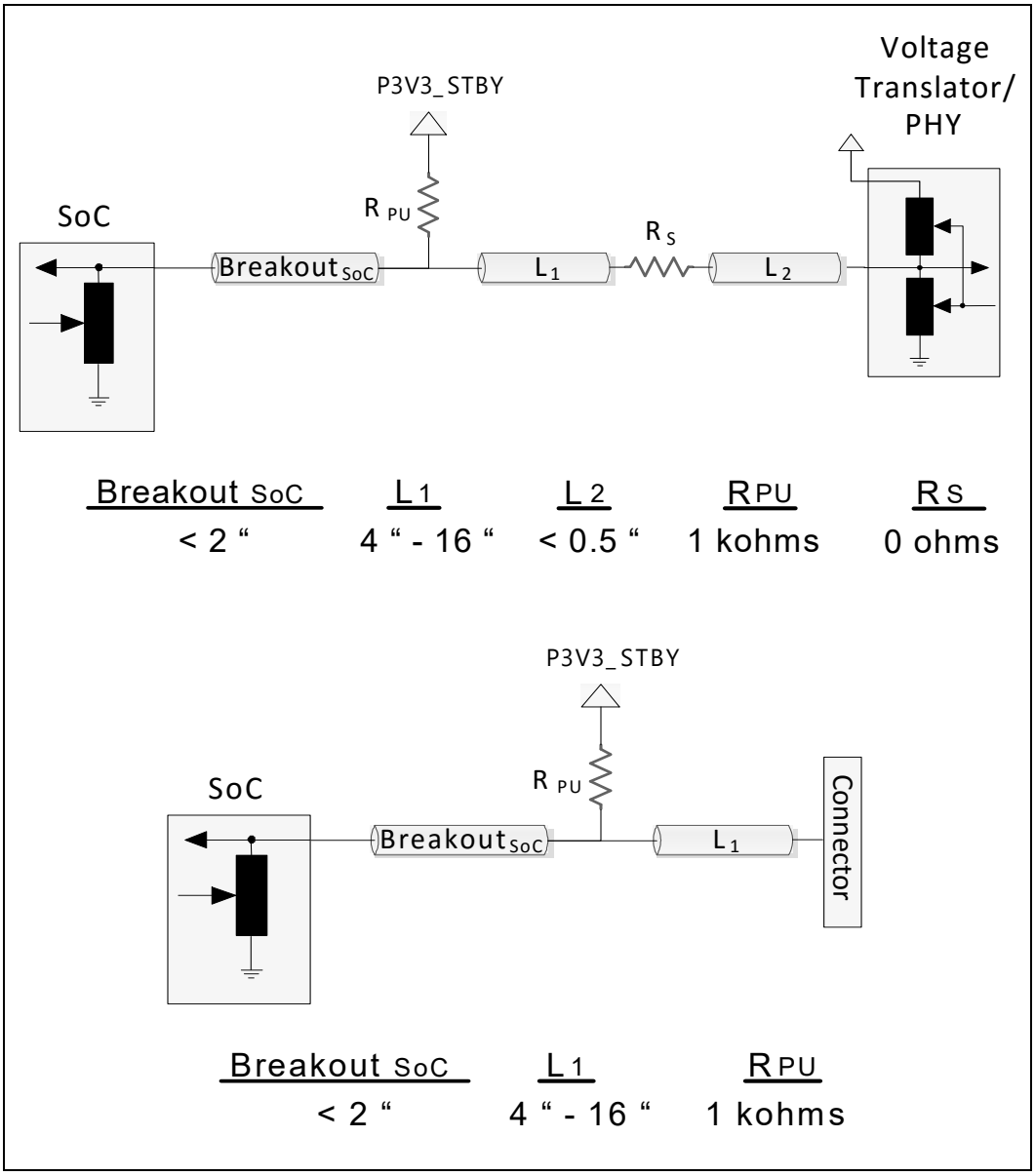
6.6.1 Connecting the SMBus Interface

To connect the SMBus interface to the chipset or the MC; connect the SMB_LAN_DATA, SMB_LAN_CLK and SMB_LAN_ALRT_N signals to the corresponding pins of the chipset/MC. These pins require pull-up resistors to the 3.3V supply rail.

Note: If the interface is not used, the previously mentioned pull-up resistors on the SMBus data, clock, and alert signals must be in place.

Intel recommends that the SMBus be connected to the chipset or MC for the Flash recovery solution. If the connection is to a MC, it is able to send the Flash release command. When enabled, the SMBus interface can be configured to support both slow and fast timing modes. See Chapter 11, "System Management Bus Interfaces" Interface for routing guidelines.

Figure 6-36. Routing Illustration for a SMBUS Point-to-Point Clock, Data, and Alert to a Device Down and to a Connector (SMB_LAN_CLK, SMB_LAN_DATA, and SMB_LAN_ALRT_N).



The 0 Ω resistors in the different topologies should be populated if the buffer impedance of the driving device is below the transmission line impedance (50 Ω). The resistor value should be chosen so the buffer impedance plus the resistor value match the transmission line impedance. The purpose is to reduce Overshoot/Undershoot.

Table 6-13. SMBUS Point-to-Point Clock, Data, and Alert to a Device Down and to a Connector (SMB_LAN_CLK, SMB_LAN_DATA, and SMB_LAN_ALRT_N) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			4000	16000	GND
L2	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%	4000	18500	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-14. SMBUS Point-to-Point Clock, Data, and Alert to a Device Down and to a Connector (SMB_LAN_CLK, SMB_LAN_DATA, and SMB_LAN_ALRT_N) Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.2 Connecting the NC-SI Interface

The NC-SI interface is a connection to an external MC. It operates as a single interface with an external MC where all traffic (other than header redirection) between the integrated LAN controller and the MC flows through the interface.

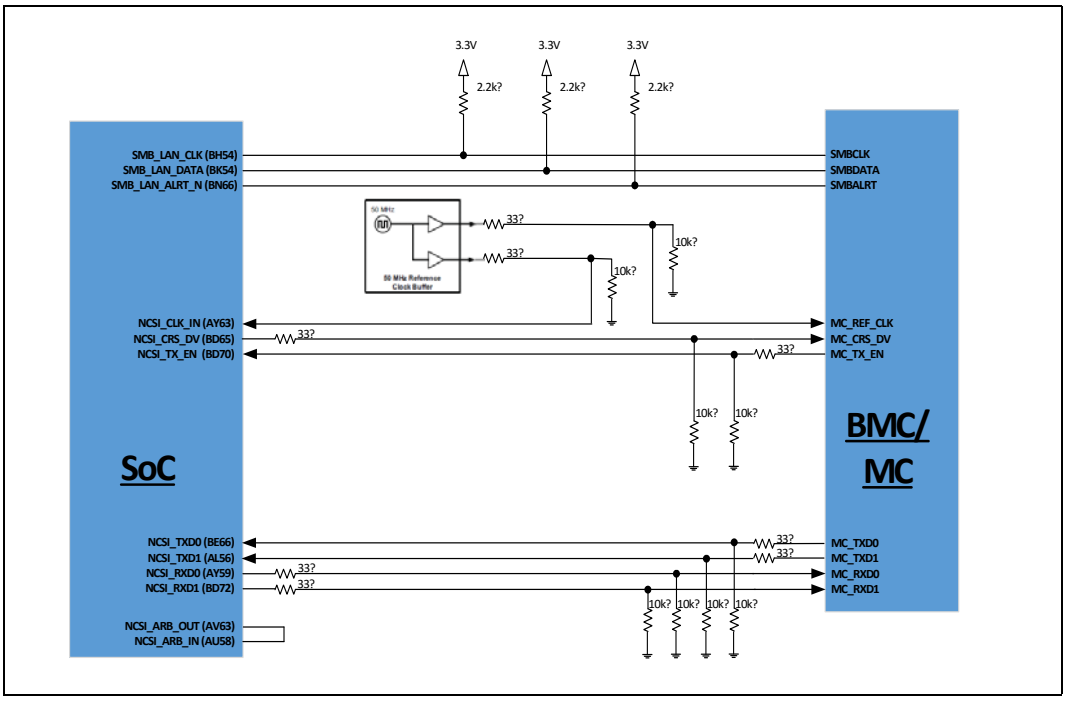
An external MC is required to meet the requirements called out in the latest NC SI specification as it relates to this interface.

The NC-SI signaling interface is a single ended signaling environment.

6.6.2.1 Single-Drop Reference Design

The following reference schematic (provides connectivity requirements for single and multi-drop applications. This configuration only has a single connection to the MC. The network device also supports multi-drop NC-SI configuration architecture with hardware arbitration support from the MC.

Figure 6-37. NC-SI Connection Schematic: Single-Drop Configuration



6.6.2.2 NC-SI Clock Layout Design

Figure 6-38. Routing Illustration NC-SI Clock

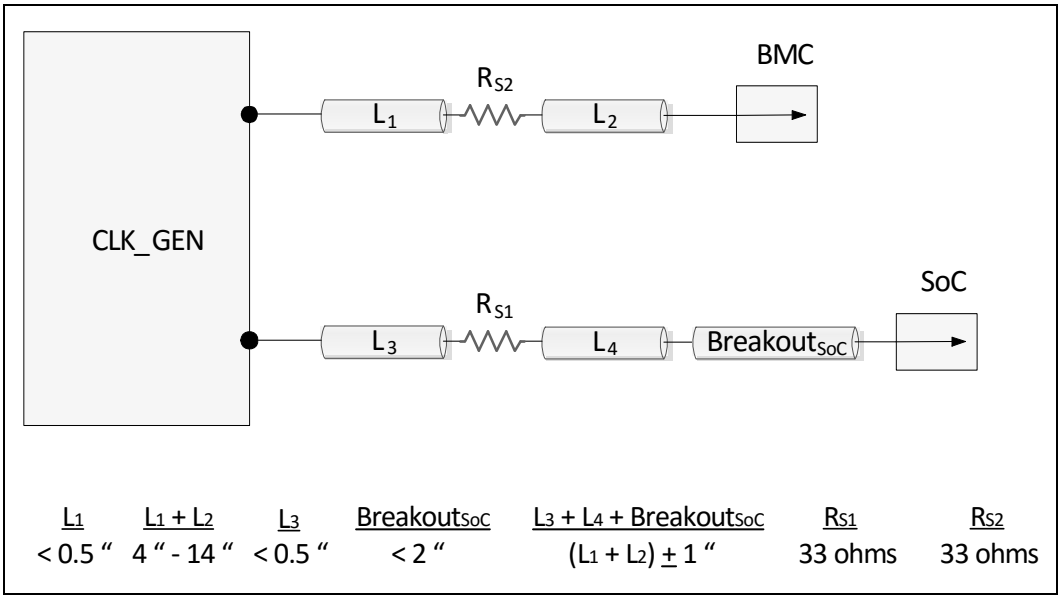


Table 6-15. NC-SI Clock Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	500	GND
L2	all			0	500	GND
(L1 + L2)	all			4000	14000	GND
(L3 + L4 + $Breakout_{SoC}$)	all			(L1 + L2) -1000	(L1 + L2) +1000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-16. NC-SI Clock Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.2.3 NC-SI Transmit (NCSI_TXD0, NCSI_TXD1, NCSI_TX_EN) Layout Design

In this application the transmit signals are the inputs to the SoC. See Figure 6-36 above.

Figure 6-39. Routing Illustration NC-SI Transmit (NCSI_TXD0, NCSI_TXD1, NCSI_TX_EN)

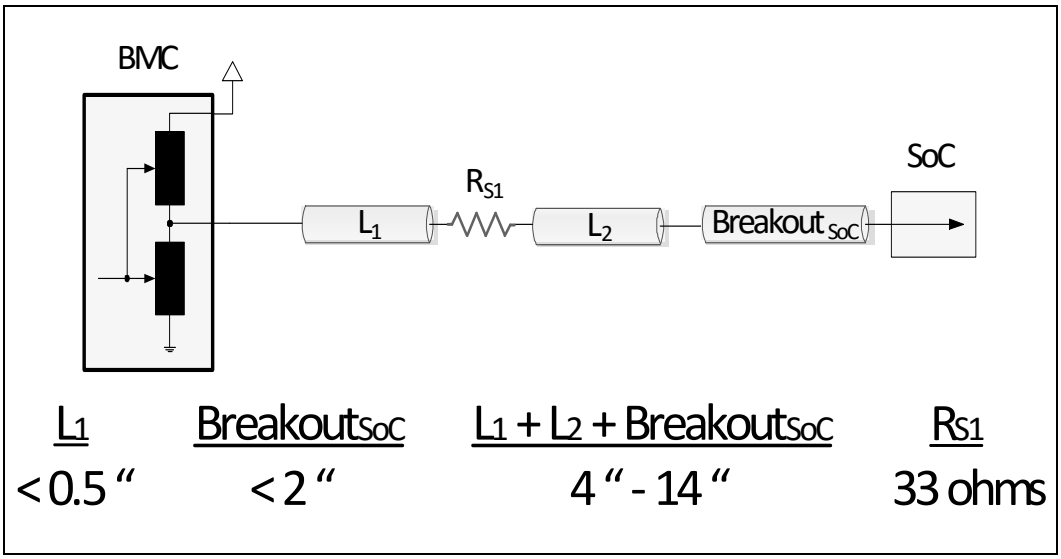


Table 6-17. NC-SI Transmit (NCSI_TXD0, NCSI_TXD1, NCSI_TX_EN) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
(L1 + L2 + $Breakout_{SoC}$)	all			4000	14000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-18. NC-SI Transmit (NCSI_TXD0, NCSI_TXD1, NCSI_TX_EN) Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.2.4 NC-SI Receive (NCSI_RXD0, NCSI_RXD1, NCSI_CRS_DV) Layout Design

In this application the receive signals are the outputs from the SoC. See Figure 6-34 above.

Figure 6-40. Routing Illustration NC-SI Receive (NCSI_RXD0, NCSI_RXD1, NCSI_CRS_DV) Layout Design

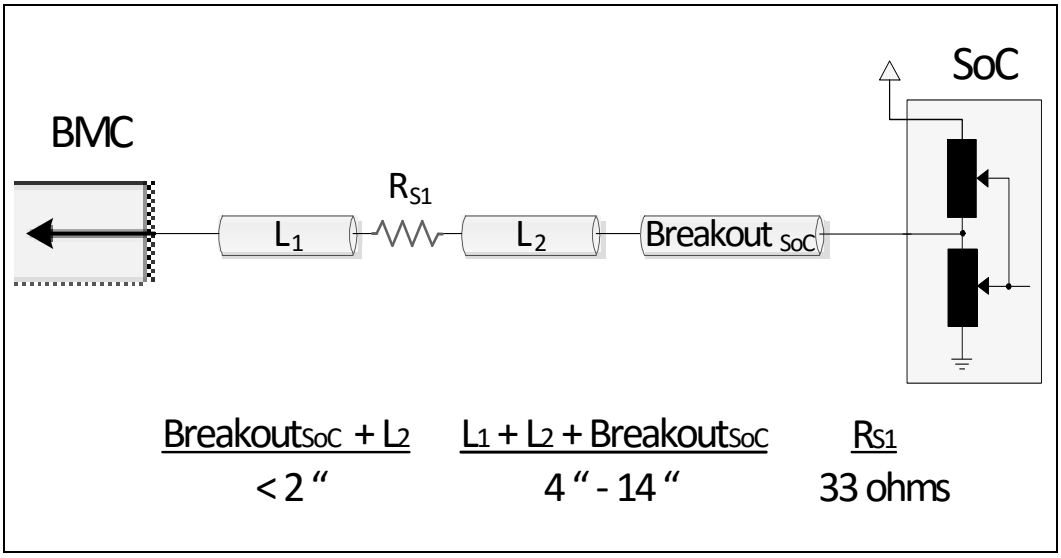


Table 6-19. NC-SI Receive (NCSI_RXD0, NCSI_RXD1, NCSI_CRS_DV) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%			GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L2	all			0	2000	GND
(L1 + L2 + $Breakout_{SoC}$)	all			4000	14000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-20. NC-SI Receive (NCSI_RXD0, NCSI_RXD1, NCSI_CRS_DV) Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

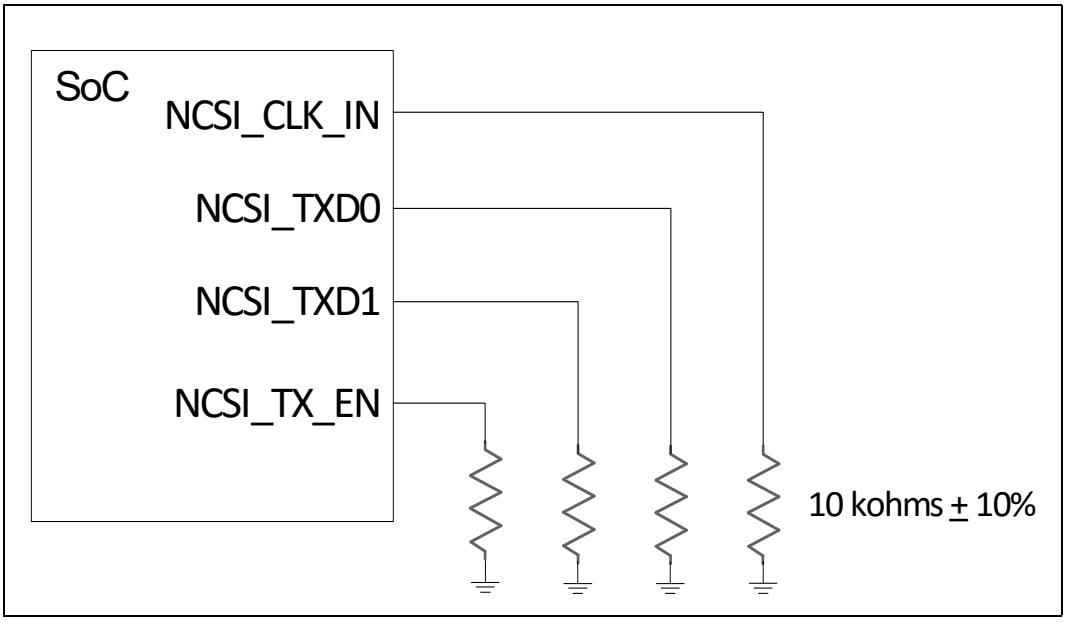
6.6.2.5 NC-SI Layout Multi-drop Requirements

Note: A new issue has been observed with the NCSI Multi-Drop configuration, resolution is currently included in the *Intel® Atom™ Processor C3000 Product Family Specification Update - NDA (Document ID #572409).*

6.6.2.5.1 Unused NC-SI Interface

If the NC SI interface is not use, connect the LAN_NCSI_CLK_IN, LAN_NCSI_TXD0, LAN_NCSI_TXD1, and LAN_NCSI_TX_EN pins to ground through 10 KΩ resistors.

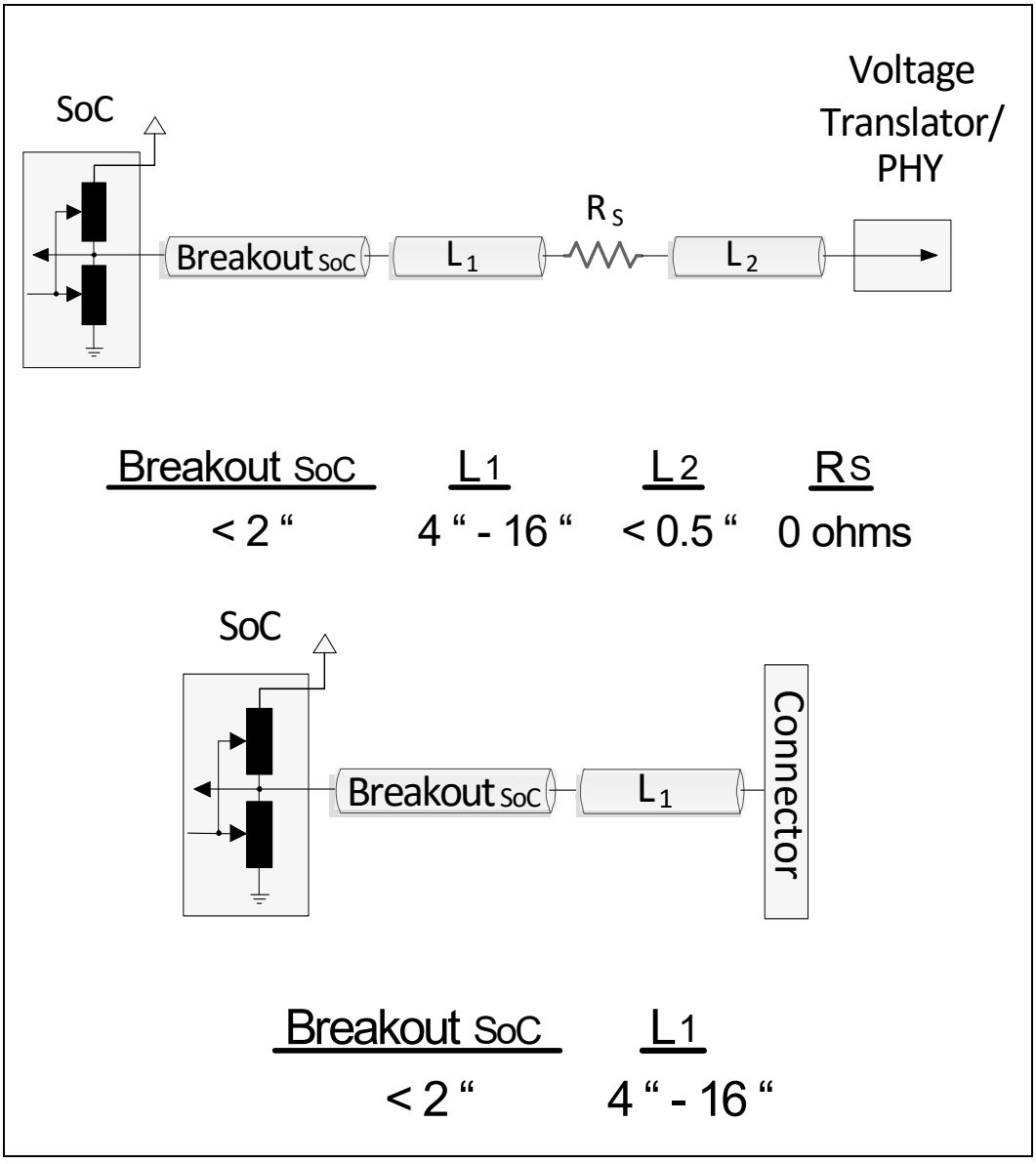
Figure 6-41. NC-SI Unused Connection



6.6.3 Connecting the MDIO Interface

The integrated LAN controllers implement a MDIO interface that controls and manages PHY devices (master side). This interface provides the Media Access Controller (MAC) and software with the ability to monitor and control the state of the external 3rd party PHY.

Figure 6-42. MDC (LAN_MDC) Point-to-Point to Device Down and the MDC (LAN_MDC) Point-to-Point to a Connector Design



The 0 Ω resistors in the different topologies should be populated if the buffer impedance of the driving device is below the transmission line impedance (50 Ω). The resistor value should be chosen so the buffer impedance plus the resistor value match the transmission line impedance. The purpose is to reduce Overshoot/Undershoot.

Table 6-21. MDC (LAN_MDC) Point-to-Point to Device Down and the MDC (LAN_MDC) Point-to-Point to a Connector Layout Recommendations

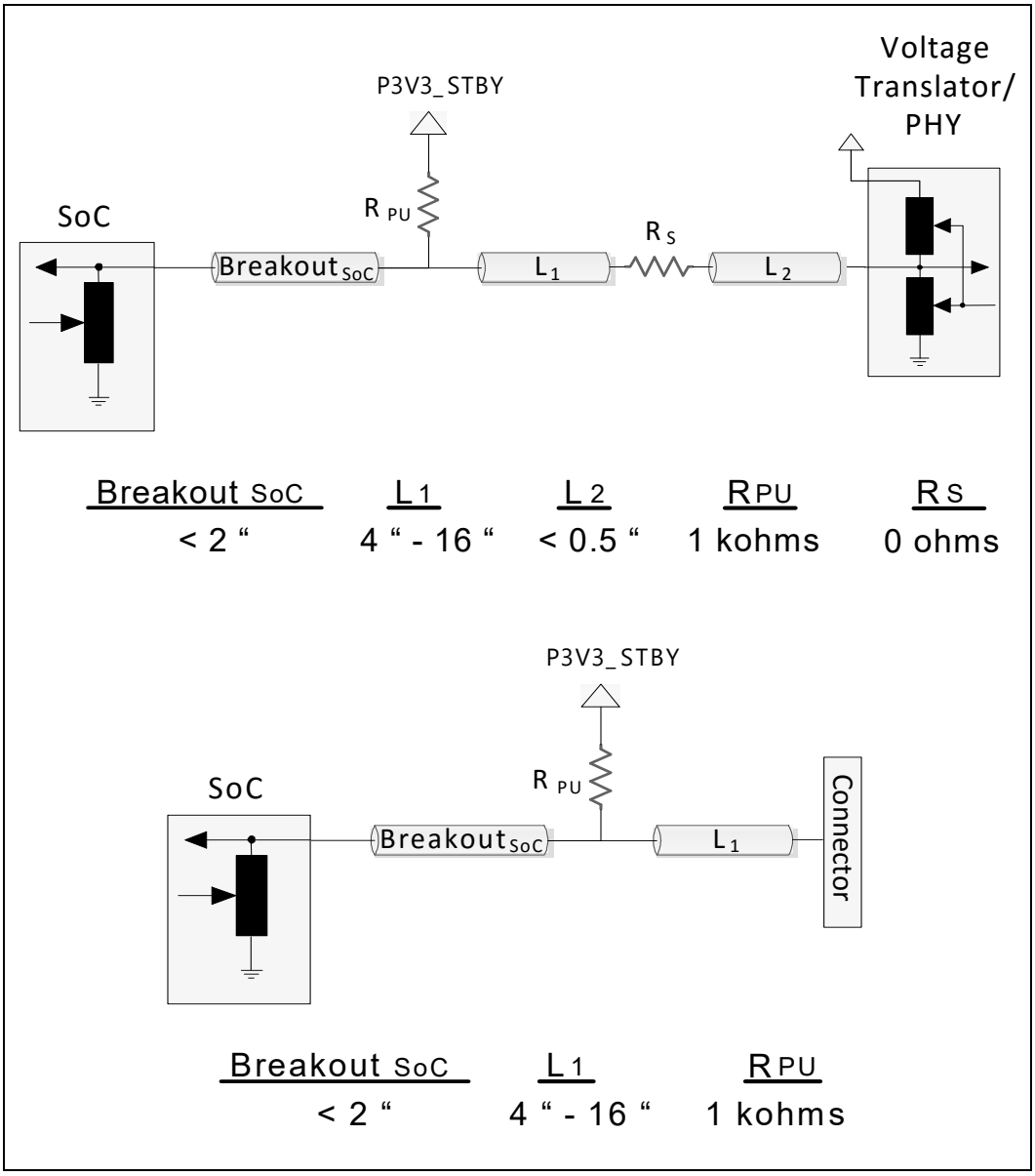
Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			4000	16000	GND
L2	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%	4000	18500	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.
4. The topology supports a maximum transfer rate of 25 MHz.
5. Length match MDIO to MDC signals to within 1".

Table 6-22. MDC (LAN_MDC) Point-to-Point to Device Down and the MDC (LAN_MDC) Point-to-Point to a Connector Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 6-43. Routing Illustration for a MDIO (LAN_MDIO) Point-to-Point to a Device Down and for a MDIO (LAN_MDIO) Point-to-Point to a Connector.



The 0 Ω resistors in the different topologies should be populated if the buffer impedance of the driving device is below the transmission line impedance (50 Ω). The resistor value should be chosen so the buffer impedance plus the resistor value match the transmission line impedance. The purpose is to reduce Overshoot/Undershoot.

Table 6-23. MDIO (LAN_MDIO) Point-to-Point to a Device Down and for a MDIO (LAN_MDIO) Point-to-Point to a Connector Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			4000	16000	GND
L2	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%	4000	18500	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.
4. The topology supports a maximum transfer rate of 25 MHz.
5. Length match MDIO to MDC signals to within 1".

Table 6-24. MDIO (LAN_MDIO) Point-to-Point to a Device Down and for a MDIO (LAN_MDIO) Point-to-Point to a Connector Layout Recommendations: Trace Spacing (Mils)

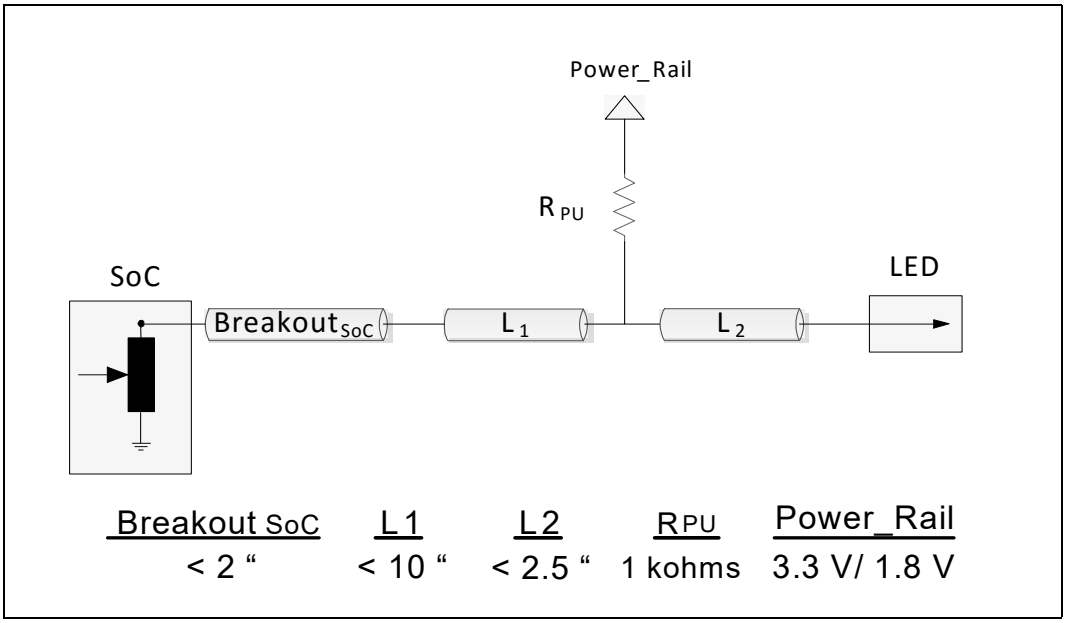
Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.4 Connecting the LED Interface

The LED interface provides output drivers for connectivity to external LED circuits per port. Each of the LED outputs can be individually configured to select the particular event, state, or activity which is indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indications.

Table 6-31, "SDP Assignment during Ethernet Mode of Operation" lists the MDIO/LED interface required for integrated LAN controllers.

Figure 6-44. LED Interface Point-to-Point to a Device Down (LAN0_PORT0_LED[3:0], LAN0_PORT1_LED[1:0], LAN1_PORT0_LED[1:0], and LAN1_PORT1[1:0]) Connections



The power rail pull-up resistor is chosen according to the signal voltage level of the SoC and the power rail availability at the different platform power states to avoid current leakages.

Table 6-25. LED Interface Point-to-Point to a Device Down (LAN0_PORT0_LED[3:0], LAN0_PORT1_LED[1:0], LAN1_PORT0_LED[1:0], and LAN1_PORT1[1:0]) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	GND
L2				0	2500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-26. LED Interface Point-to-Point to a Device Down (LAN0_PORT0_LED[3:0], LAN0_PORT1_LED[1:0], LAN1_PORT0_LED[1:0], and LAN1_PORT1[1:0]) Layout Recommendations: Trace Spacing (Mils)

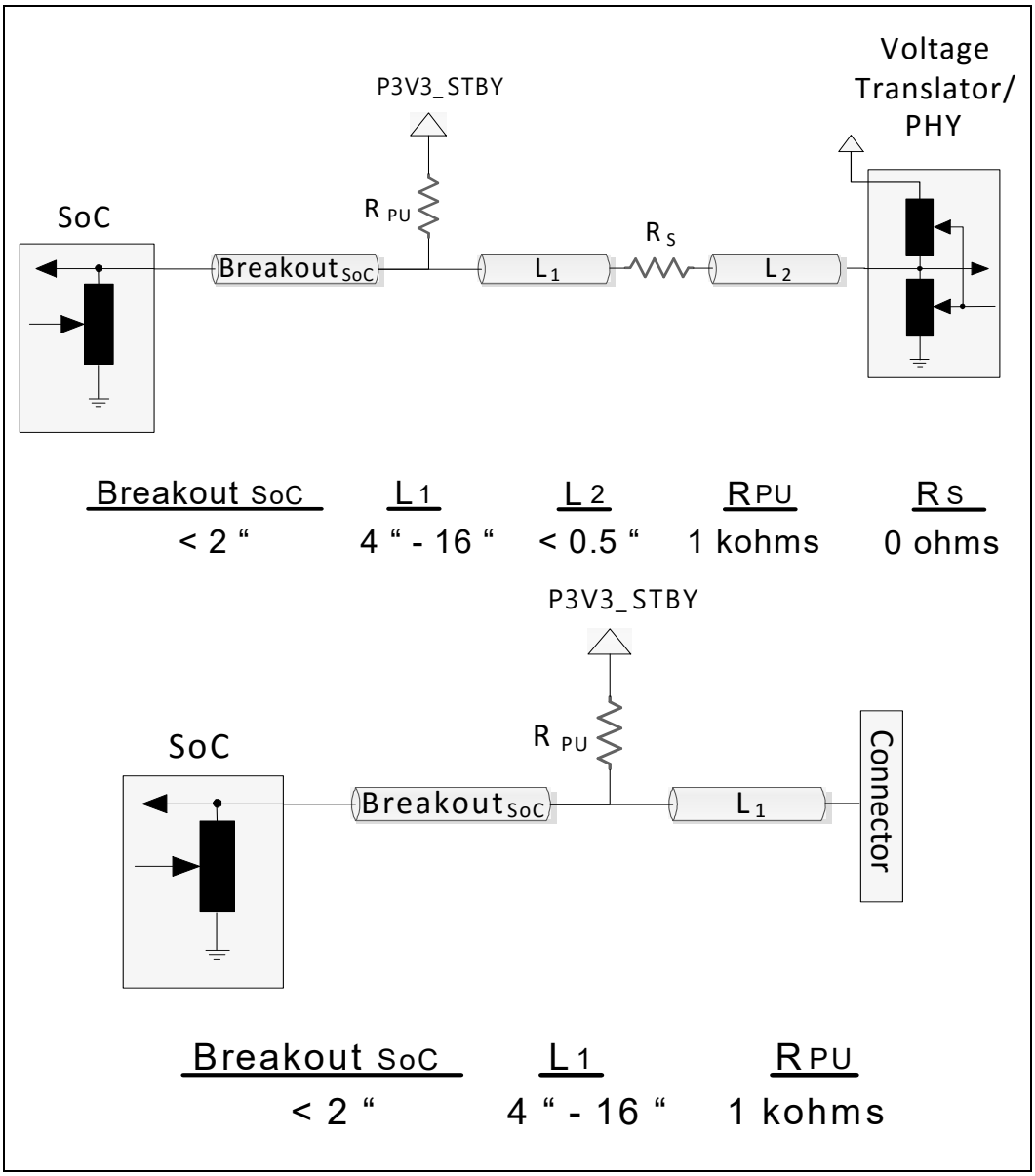
Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.5 Connecting the I2C Interface

The integrated LAN controllers implement two serial management interfaces known as I2C. These management interfaces are used to control and manage external optical modules such as SFP+. The interface provides the MAC and software with the ability to monitor and control the state of an optical module.

Table 6-31, "SDP Assignment during Ethernet Mode of Operation" lists the I2C interface required for integrated LAN controllers.

Figure 6-45. Routing Illustration for a I2C Point-to-Point Clock and Data to a Device Down and to a Connector (LANx_PORTx_I2C_CLK and LANx_PORTx_I2C_DATA).



The 0 Ω resistors in the different topologies should be populated if the buffer impedance of the driving device is below the transmission line impedance (50 Ω). The resistor value should be chosen so the buffer impedance plus the resistor value match the transmission line impedance. The purpose is to reduce Overshoot/Undershoot.

Table 6-27. I²C Point-to-Point Clock and Data to a Device Down and to a Connector (LANx_PORTx_I2C_CLK and LANx_PORTx_I2C_DATA) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			4000	16000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-28. I²C Point-to-Point Clock and Data to a Device Down and to a Connector (LANx_PORTx_I2C_CLK and LANx_PORTx_I2C_DATA) Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

6.6.6 SDPs - General Purpose I/O

The integrated LAN controllers have four (LAN0, Ports 0 and 1) or two (LAN1, Ports 0 and 1) software-defined pins (SDP pins) per port that can be used for miscellaneous hardware or software-controllable purposes. These pins and their function are bound to a specific LAN port. The use, direction, and values of SDP pins are controlled and accessed by the Extended SDP Control (ESDP) register. To avoid signal contention, following power-up, both pins are defined as input pins.

Some SDP pins have specific functionality:

- The default direction of the SDP pins is loaded from the SDP Control word in the NVM.
- The lower SDP pins (SDP0-SDP1) can also be configured for use as External Interrupt Sources (GPI).

To act as GPI pins, the desired pins must be configured as inputs and enabled by the GPIE register. When enabled, an interrupt is asserted following a rising-edge detection of the input pin (rising-edge detection occurs by comparing values sampled at the internal clock rate, as opposed to an edge-detection circuit). When detected, a corresponding GPI interrupt is indicated in the EICR register.

Note: An SDP configured as output can also generate interrupts, but this is not a recommended configuration.

Figure 6-46. Routing Illustration for a Software Defined Pin (SDP) I/O CMOS Signal (LAN0_PORTx_SDP[3:0] and LAN1_PORTx_SDP[1:0])

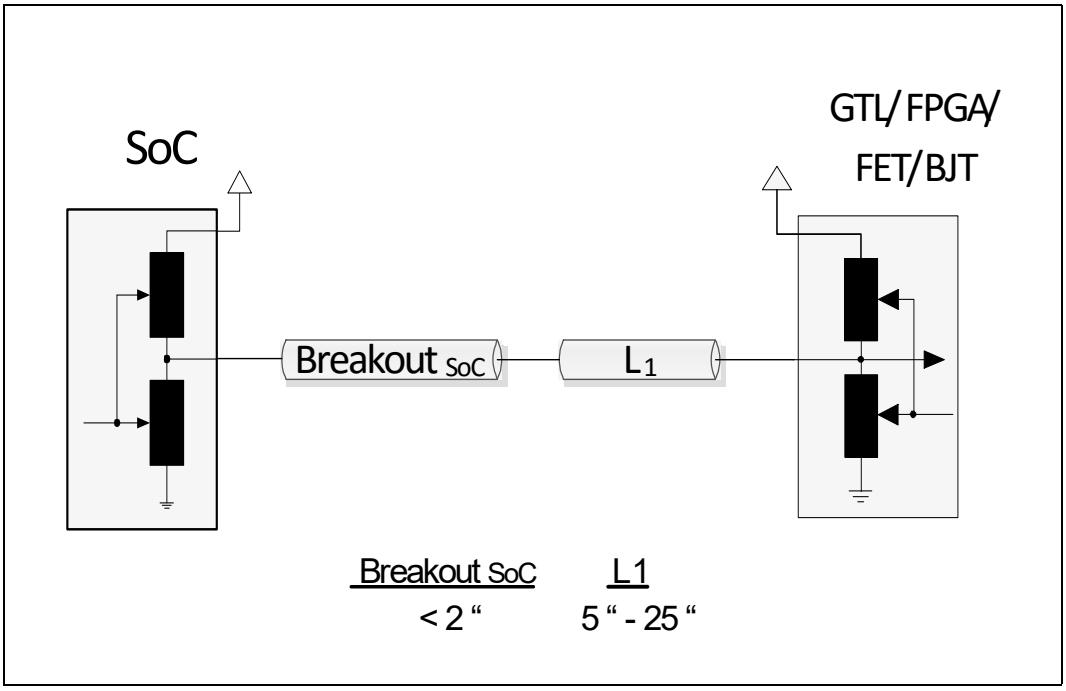


Table 6-29. Software Defined Pin (SDP) I/O CMOS Signal (LAN0_PORTx_SDP[3:0] and LAN1_PORTx_SDP[1:0]) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 6-30. Software Defined Pin (SDP) I/O CMOS Signal (LAN0_PORTx_SDP[3:0] and LAN1_PORTx_SDP[1:0]) Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

The SDPs will take on different roles during different modes of Ethernet operation based on the settings of the GPIE register.

Table 6-31 shows the modes that SDPs and a few other miscellaneous I/O will take on during various Ethernet modes. As a reminder, these modes are set in the shared NVM section for each LAN controller (LAN0 and LAN1).

Table 6-31. SDP Assignment during Ethernet Mode of Operation

Pins	2x10G SFP+	4x10G SFP+	10G-BASE-T with x557	4x10G with Cortina	4 x KR/KX Backplane	1G-BASE-T with Marvel 1512/1514 [2]	1G-BASE-T with Marvell 1543
LAN0_PORT0_SDP0	(SFP+_0) MOD_ABS	(SFP+_0) MOD_ABS	P0_INT_N	(SFP+_0) MOD_ABS	NA	LED2_INTn of PHY0	INTn
LAN0_PORT0_SDP1	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT0_SDP2	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT0_SDP3	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT1_SDP0	(SFP+_1) MOD_ABS	(SFP+_1) MOD_ABS	P1_INT_N	(SFP+_1) MOD_ABS	NA	LED2_INTn of PHY1	INTn
LAN0_PORT1_SDP1	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT1_SDP2	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT1_SDP3	NA	NA	NA	NA	NA	NA	NA
LAN1_PORT0_SDP0	NA	(SFP+_2) MOD_ABS	P2_INT_N	(SFP+_2) MOD_ABS	NA	LED2_INTn of PHY0 [3]	INTn
LAN1_PORT0_SDP1	NA	NA	NA	NA	NA	NA	NA
LAN1_PORT1_SDP0	NA	(SFP+_3) MOD_ABS	P3_INT_N	(SFP+_3) MOD_ABS	NA	LED2_INTn of PHY1 [3]	INTn
LAN1_PORT1_SDP1	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT0_LED0	LED0_0	LED0_0	LED0_0	LED0_0	LED0_0	LED0_0	LED0_0
LAN0_PORT0_LED1	LED0_1	LED0_1	LED0_1	LED0_1	LED0_1	LED0_1	LED0_1
LAN0_PORT0_LED2	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT0_LED3	NA	NA	NA	NA	NA	NA	NA
LAN0_PORT1_LED0	LED1_0	LED1_0	LED1_0	LED1_0	LED1_0	LED1_0	LED1_0
LAN0_PORT1_LED1	LED1_1	LED1_1	LED1_1	LED1_1	LED1_1	LED1_1	LED1_1
LAN1_PORT0_LED0	NA	LED2_0	LED2_0	LED2_0	LED2_0	NA	LED2_0
LAN1_PORT0_LED1	NA	LED2_1	LED2_1	LED2_1	LED2_1	NA	LED2_1
LAN1_PORT1_LED0	NA	LED3_0	LED3_0	LED3_0	LED3_0	NA	LED3_0
LAN1_PORT1_LED1	NA	LED3_1	LED3_1	LED3_1	LED3_1	NA	LED3_1
LAN0_PORT0_I2C_DATA	SDA_0	SDA_0	NA	SDA_0	NA	NA	NA
LAN0_PORT0_I2C_CLK	SCL_0	SCL_0	NA	SCL_0	NA	NA	NA
LAN0_PORT1_I2C_DATA	SDA_1	SDA_1	NA	SDA_1	NA	NA	NA
LAN0_PORT1_I2C_CLK	SCL_1	SCL_1	NA	SCL_1	NA	NA	NA
LAN1_PORT0_I2C_DATA	NA	SDA_2	NA	SDA_2	NA	NA	NA
LAN1_PORT0_I2C_CLK	NA	SCL_2	NA	SCL_2	NA	NA	NA
LAN1_PORT1_I2C_DATA	NA	SDA_3	NA	SDA_3	NA	NA	NA
LAN1_PORT1_I2C_CLK	NA	SCL_3	NA	SCL_3	NA	NA	NA
LAN_MDIO	NA	NA	Px_MDIO	SDA	NA	MDIO	MDIO
LAN_MDC	NA	NA	Px_MDC	SCL	NA	MDC	MDC

Notes:
1. IEEE 1588 functionality will not be available during 4x10G SFP+ mode.
2. Connect the Marvell 1512/1514 to the respective LAN SDP pin and LED pins e.g. if another Marvell 1512/1514 phy is connected to LAN0_Port1 connect its LED2/INTn pin to LAN0_Port1_SDP0 and use LEDs LAN0_PORT1_LED0 and LAN0_PORT1_LED1.
3. For design connecting Marvell 1512/1514 to DNV LAN Controller 1.

6.6.7 LAN Reference Clock and Bias Circuit

A 1 KΩ ± 0.1% resistor needs to be connected between the VCCKRLCPLL (1.05V) and LANx_RBIAS pins. To reduce noise coupled onto this reference signal and the IR-drop place the bias resistor close to the integrated LAN controller. Keep traces as short as possible. It is preferable to mount the resistor to the bottom side with one terminal to VCCKRLCPLL and the second terminal to the LANx_RBIAS ball.

Figure 6-47. LAN Reference Clock and Bias Circuit

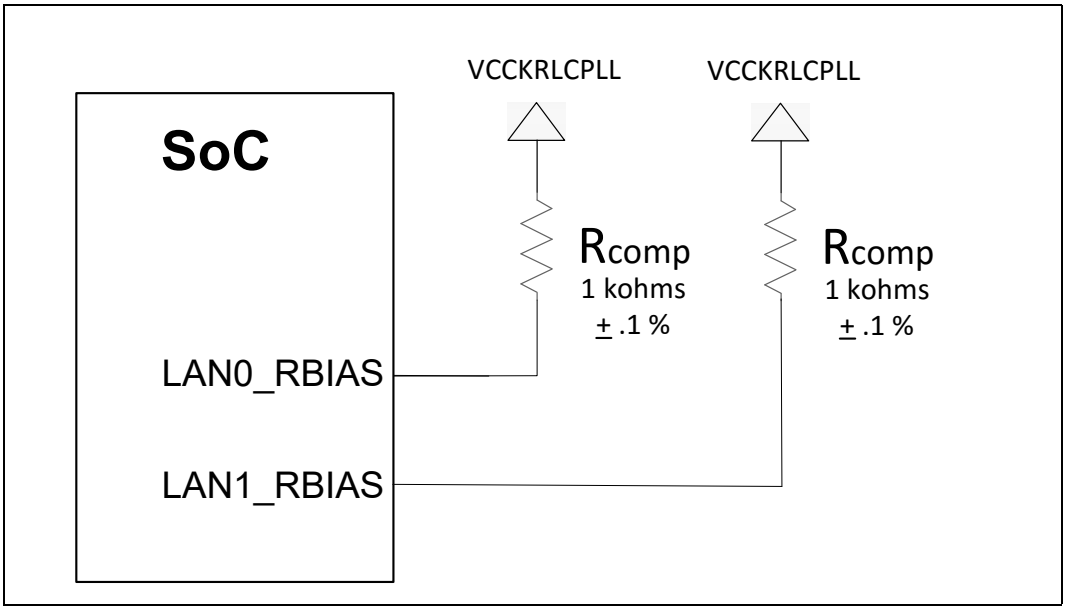


Table 6-32 lists the integrated LAN controller clock and RBIAS interface.

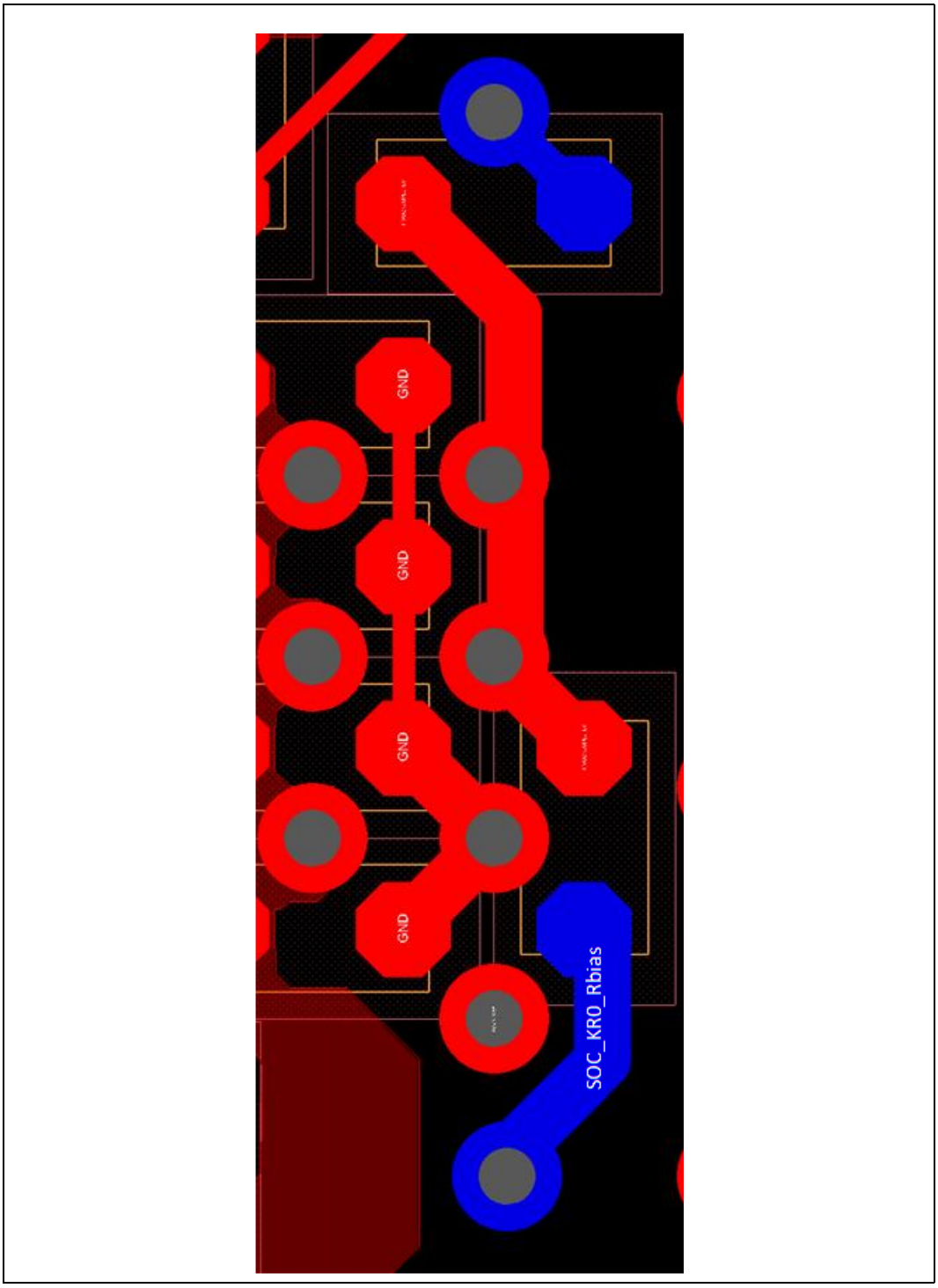
Table 6-32. Clock/R_{BIAS} Pinouts

Pin Name	Type	Internal Pup/Pdn	External Pup/Pdn	Name and Function
LAN0_RBIAS LAN1_RBIAS	IN			External resistor bias input.
CLK_X1_PAD CLK_X2_PAD	A-INOUT			External reference clock input/crystal oscillator input.

Table 6-33. LAN_RBIAS R_{BIAS} Routing Guidelines

Signal Name	Max DC Capacitance	Max DC Resistance	Recommended Trace Width	Recommended Spacing to other metal	Layer	Total Length	Notes
SOC_KR0_Rbias SOC_KR1_Rbias	3pF	0.1 Ω	5 mils	6.5 mils	Microstrip	860mil	
SOC_KR0_Rbias SOC_KR1_Rbias	3pF	0.1 Ω	6.5 mils	5 mils	Microstrip	600mil	
SOC_KR0_Rbias SOC_KR1_Rbias	3pF	0.1 Ω	10 mils	5 mils	Microstrip	480mil	

Figure 6-48. LAN Reference Clock and Bias Circuit



Notes:
1. Signal Name: SOC_KR0_Rbias
2. Microstrip Routing Length: 50mil
3. Microstrip Routing Width: 10mil

§ §

7 Serial ATA

The SATA signals in Table 8-1 are a subset of the HSIO 20 lanes (SKU dependent) available for PCIe* Gen3, SATA, and USB 3.0. How the signals in Table 8-1 are associated with the 20 HSIO Lanes, the supported shared patterns, and the HSIO configuration control are described in Chapter 10, "Flexible I/O Adapter (FIA) Overview" of the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4.*

Note: The signal names below align with the SoC pins HSIO_RX_DP[19:4], HSIO_RX_DN[19:4], HSIO_TX_DP[19:4], and HSIO_TX_DN[19:4]. Figure 10-2 in Chapter 10 of the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* shows the relationship of function (PCIe, SATA, or USB) to HSIO lane.

The SoC has two independent integrated SATA3 host controllers (SKU dependent). Each controller supports DMA operation up to 8 ports and supports data transfer rates up to 6 Gbps (600 MBps). Legacy data transfer rates of 3 Gbps and 1.5 Gbps are supported as well. Two modes of operation are enabled for controllers: RAID and AHCI modes. Serial General Purpose Input Output (SGPIO) support is added in this generation following the SFF 8485 specification.

Note: The routing guidelines contained in this chapter assume the stackups shown in Chapter 2, "Platform Stack-up and General Design Considerations". A particular trace width and spacing provided in this chapter will meet the target impedance requirements when implemented on a reference stackup. Platform designers may have to adjust trace width and/or spacing to meet impedance/crosstalk requirements if using a different stackup.

Note: Legacy and Native IDE are not supported in this generation.

Table 7-1. Serial ATA Signals

Signal name	Direction	Shared	Description
SATA CONTROLLER 0			
SATA0_TX_DP[7:0] SATA0_TX_DN[7:0]	O, Differential	Yes	
SATA0_RX_DP[7:0] SATA0_RX_DN[7:0]	I, Differential	Yes	
SATA0_SLD	O	Yes	SGPIO load.
SATA0_SCLK	O	Yes	SGPIO clock.
SATA0_SDOUT	O	Yes	SGPIO data out.
SATA0_LED_N	O-OD	Yes	Open collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor is required.
SATA_PDETECT[1:0]	I	Yes	
SATA CONTROLLER 1			
SATA1_TX_DP[7:0] SATA1_TX_DN[7:0]	O, Differential	Yes	
SATA1_RX_DP[7:0] SATA1_RX_DN[7:0]	I, Differential	Yes	
SATA1_SLD	O	Yes	SGPIO load.
SATA1_SCLK	O	Yes	SGPIO clock.
SATA1_SDOUT	O	Yes	SGPIO data out.
SATA1_LED_N	O-OD	Yes	Open collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor is required.

7.1 General SATA Routing Guidelines

Use the following general routing and placement guidelines when laying out a new design:

1. All serial ATA signals must be ground referenced. Use stitching capacitors when changing reference planes. Use proper placement of the stitching capacitors to minimize adverse effects on EMI and signal quality. Only one reference plane crossing is allowed.
2. Route all traces over continuous ground planes with no interruptions. Avoid crossing over anti-etch. Any discontinuity or split in the ground plane will cause signal reflections.
3. A maximum of three vias per SATA trace (via count includes a through-hole connector counts as an effective via) is allowed. If a layer change is necessary, ensure that the trace matching for either the transmit or receive pair occurs within the same layer. Use via with the shortest via stub as possible.
4. **DO NOT** route the SATA traces under the power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate the clocks.
5. **DO NOT** place stubs, test points, and test vias on the route to minimize reflection. Utilize the vias and connector pads as test points instead.
6. For testability, routing the TX and RX pairs for a given port on the same layer and close to each other helps ensure the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of the RX pair layout quality is approximated by using the results from testing the TX pair signal quality.
7. Length matching within each differential pair is done on a segment-by-segment basis at the point of discontinuity. Total length mismatch must not be more than 5 mils. Examples of segments include the breakout areas, the routes running between two vias, the routes between an AC coupling capacitor and a connector pin, and so forth. The points of discontinuity are the via, the capacitor pad, or the connector pin.
8. **DO NOT** serpentine to match the RX and TX traces; there is **NO** requirement to match the RX and TX traces. In addition, **DO NOT** serpentine to meet the minimum length guidelines on RX and TX.
9. Keep the SATA traces 20 mils from any vias on the motherboard.

10. In certain systems (such as a closed-box, small-form factor system) where a short, low-loss cable is to be used exclusively, use longer trace lengths to optimize SATA signal quality at the device receiver (RX connector specification). Careful simulation and/or studies on prototypes of signal quality are required to balance this trade-off effectively.
11. Keep traces at least 90 mils away from the edge of the plane. This helps prevent the coupling of the signal onto the adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.
12. Maintain parallelism between SATA differential signals with the trace spacing to achieve 85 Ω ± 10% on stripline and 85 Ω ± 15% on microstrip differential impedance. Deviations will occur due to package breakout and routing to the connector pins. Minimize these deviations.
13. Use an impedance calculator to synchronize the trace width and spacing required for the specific board stackup which may vary from those used in this design guide. Keep in mind that the impedance target is 85 Ω ± 15% on microstrip.
14. To prevent crosstalk and achieve optimal signal quality use a minimum spacing of 7h for stripline and 9h for microstrip between SATA signal pairs and other signal traces: h is the dielectric thickness. For spacing within the same signal bundle the minimum pair-to-pair spacing is 5h for stripline and 7h for microstrip for TX to TX signals. The minimum for RX to RX signals within the same bundle is 7h for stripline and 9h for microstrip.
15. RX signals breakout on the top layer. The main routing can be on the top, bottom, or internal layers depending on topology and type of connector used. When routing on internal layers use the layer creating the minimum via stub length. TX and TX signal break out should not be interleaved or on different layers. Keep a minimum for TX to RX pair-to-pair spacing of 9h form stripline and 13h for microstrip to reduce near-end crosstalk.

The minimum length from the SoC to the SATA connector is not less than 2.0 inches.

7.2 SATA Gen3 Routing Requirements

7.2.1 Routing Topology

The serial ATA interface has a point-to-point topology as shown in Figure 7-1. Only one SATA port is shown in Figure 7-1. The following sections detail the routing requirements and trace guidelines for SATA Gen3 (6 Gb/s).

Figure 7-1. Serial ATA Topology

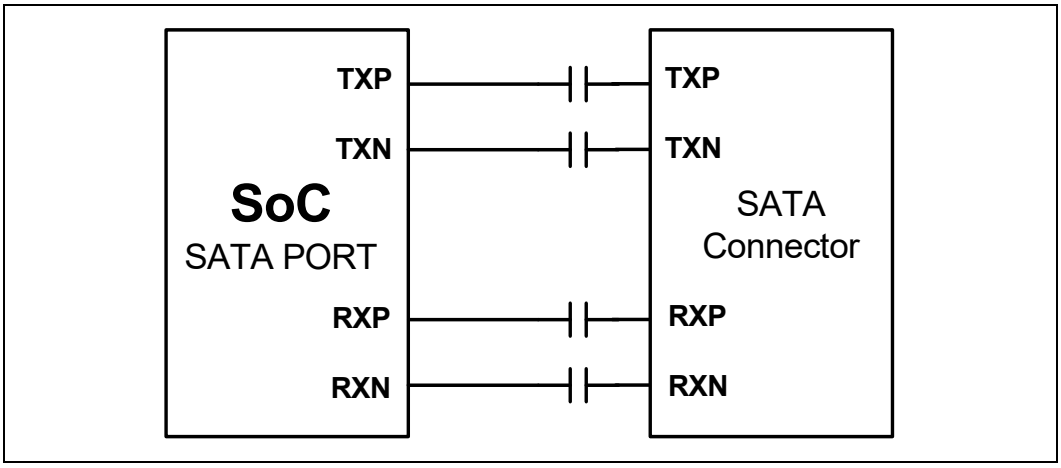
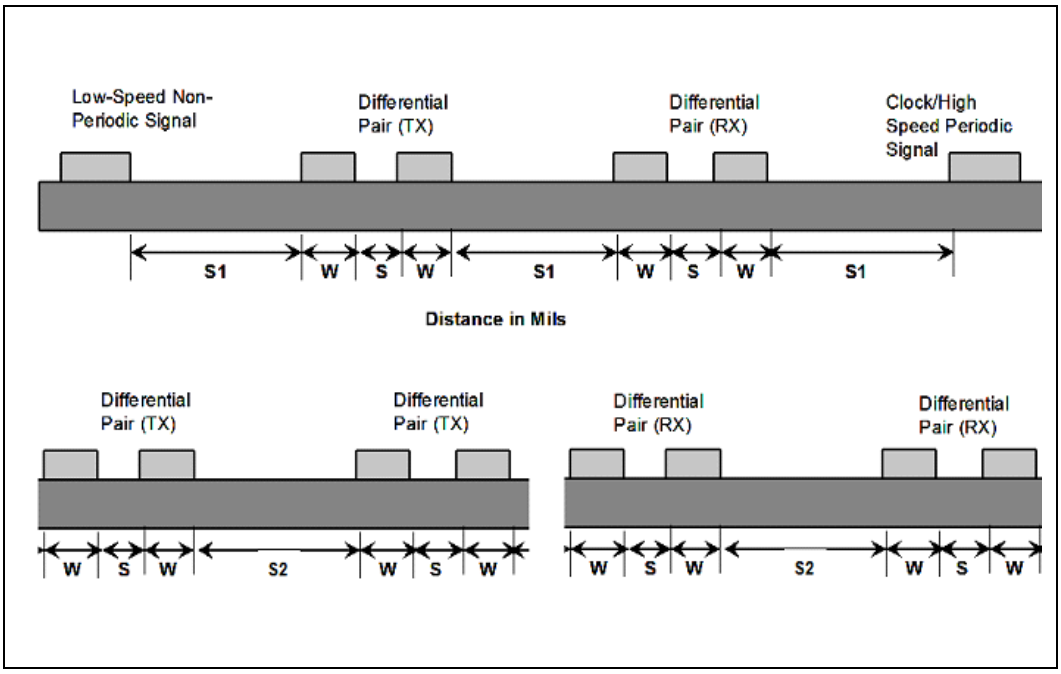


Figure 7-2. Illustration of Serial ATA Trace Spacing



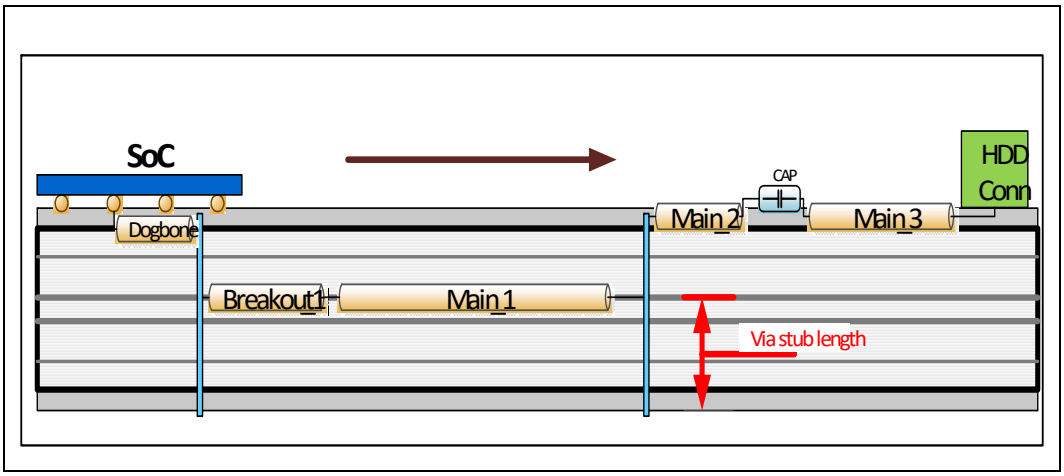
If the trace length of the differential pair is longer than recommended, the high-frequency differential signal suffers signal attenuation and a slower rise time/fall time.

The Gen3 internal SATA topology supports the routing of a SATA port to the Hard Disk Device (HDD) with the SATA cable. Maximum length allowed for the SATA cable is 1 m (39.4”). All SATA ports also support SATA Gen1 and Gen2.

This section provides details on SATA routing topologies and routing length requirements.

- If the trace length of the differential pair is longer than recommended, the high-frequency differential signal will suffer signal attenuation, an increase in crosstalk, and a diminished signal integrity.
- When using a through-hole connector including a joint antipad in the pin field is strongly recommended for better signal integrity, as illustrated in Figure 7-9.
- Voiding the mounting pads is recommended to improve signal integrity when a surface-mount (SMT) connector is used.
- The maximum via count allowed depends on the topology being used.
- Refer to Section 7.2.2, “Cable and Connector Requirements for detailed guidelines of SATA cable implementation.

Figure 7-3. Routing Topology for the SATAx TX Differential Signals using Stripline



Notes:
1. This topology uses a SM-HDD connector.
2. Breakout_1 should not exceed 500 mils
3. This topology requires a capacitor on the top layer only.
4. Capacitor to SM_HDD connector total length should not exceed 250 mils
5. Breakout_1 and Main_1 are allowed to run on the bottom layer (microstrip).
6. For via stub of 60 mils see the table below for routing restrictions.
7. Intel supports the same Direct Attached topologies (NO cable) with a M.2 connector.

Table 7-2. SATAx TX Differential Signals using Stripline Layout Recommendations

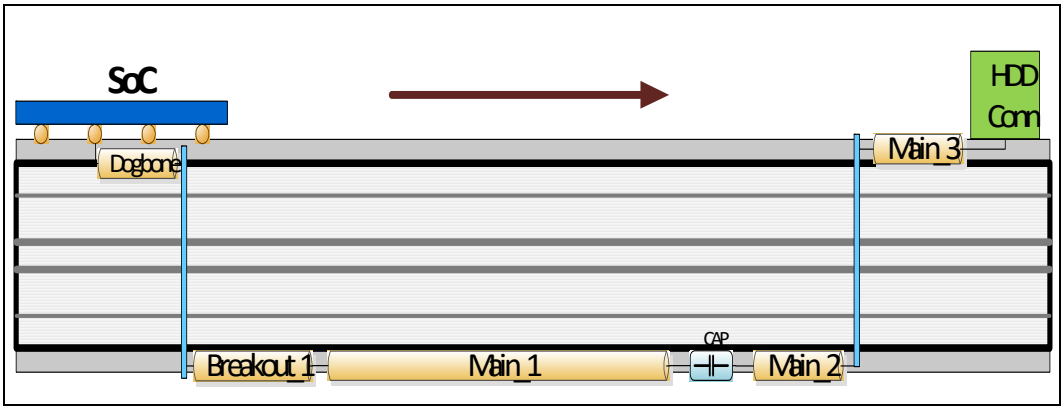
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	stripline	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all				2	2500	8000	GND

Notes:
1. The trace-length matching requirement for differential pairs is < 5 mils for each segment.

Table 7-3. SATAx TX Differential Signals using Stripline Layout Spacing Recommendations

Routing Section	Layer	Type (TX)	Type (RX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-4. Routing Topology for the SATAx TX Differential Signals using Microstrip



Notes:
1. This topology uses a SM-HDD connector.
2. Breakout_1 should not exceed 500 mils.
3. Capacitor to SM_HDD connector total length should not exceed 500 mils.
4. The ac capacitor placement should within 500 mils of either the SoC or the SM-HDD connector or a M.2 SATA module.

Table 7-4. SATAx TX Differential Signals using Microstrip Layout Recommendations

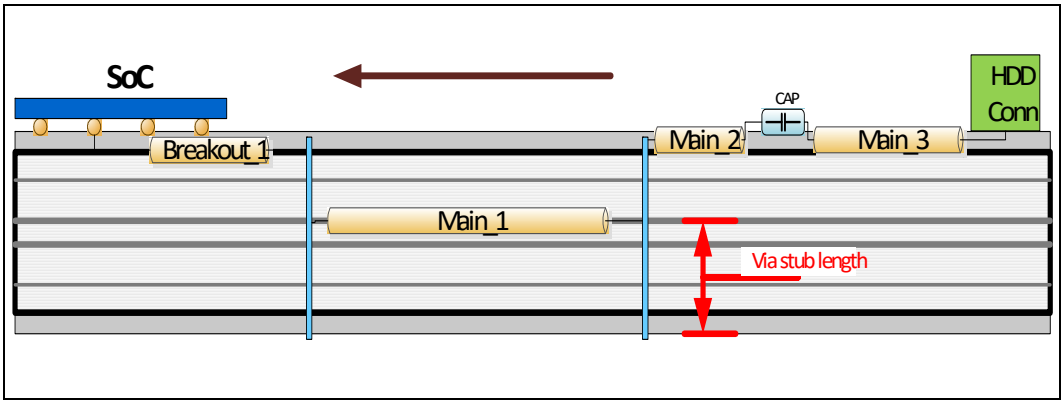
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	stripline	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all				2	2500	8000	GND

Notes:
1. The trace-length matching requirement for differential pairs is ≤ 5 mils for each segment.

Table 7-5. SATAx TX Differential Signals using Microstrip Layout Spacing Recommendations

Routing Section	Layer	Type (TX)	Type (RX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline						
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-5. Routing Topology for the SATAx RX Differential Signals using Stripline



Notes:
1. This topology uses a SM-HDD connector.
2. Breakout_1 should not exceed 500 mils.
3. Breakout_1 and Main_1 are also allowed to route on the bottom layer (microstrip).
4. Breakout_1 and Main_1 are also allowed to route on the top layer if all transitional vias are removed.
5. Connector to capacitor total length should not exceed 250 mils.
6. For via stub of 60 mils see the table below for routing restrictions.

Table 7-6. SATAx RX Differential Signals using Stripline Layout Recommendations

Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	microstrip	0						
	stripline [1]	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline							
MAIN_1+MAIN_2+ MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	microstrip	0						
	stripline	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn	microstrip					0	250	
Entire Signal	all				2	2500	8000	GND

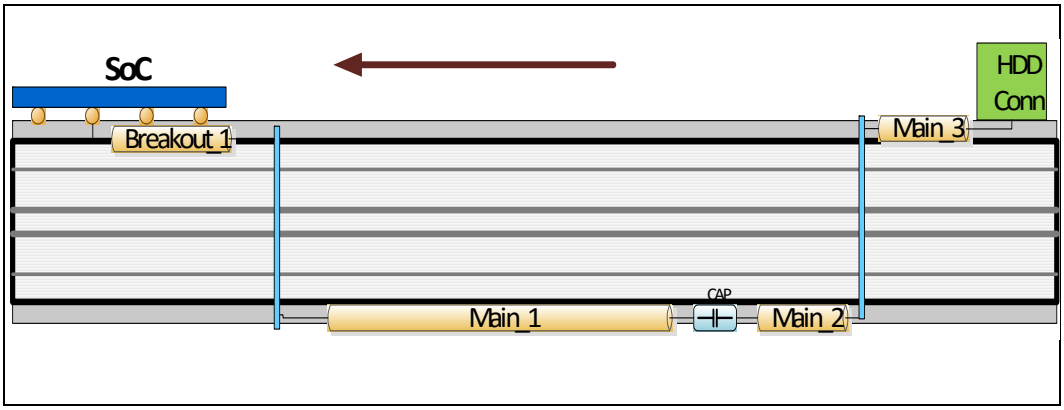
Note:
1. If via stubs = 60mils then maximum length is constrained to 7”.

Table 7-7. SATAx RX Differential Signals using Stripline Layout Spacing Recommendations

Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip [1]	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip [2]	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Notes:
1. Breakout_1 amd <ain_1 are also allowed on the top layer if all transitional vias are removed.
2. This topology requires Main_2 and Main_3 on the top layer (microstrip).

Figure 7-6. Routing Topology for the SATAx RX Differential Signals using Microstrip



Notes:
1. This topology uses a SM-HDD connector.
2. Breakout_1 should not exceed 500 mils.
3. Connector to capacitor total length should not exceed 375 mils.
4. This topology only considers routing for microstrip options.

Table 7-8. SATAx RX Differential Signals using Microstrip Layout Recommendations

Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	microstrip	0						
Breakout_1	microstrip		3.5			0	500	GND
	stripline							
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline							
MAIN_1	microstrip							
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn	microstrip [1]					0	375	
Entire Signal	all				2	2500	8000	GND

Note:
1. Connector to capacitor total length should not exceed 375 mils.

Table 7-9. SATAx RX Differential Signals using Microstrip Layout Spacing Recommendations

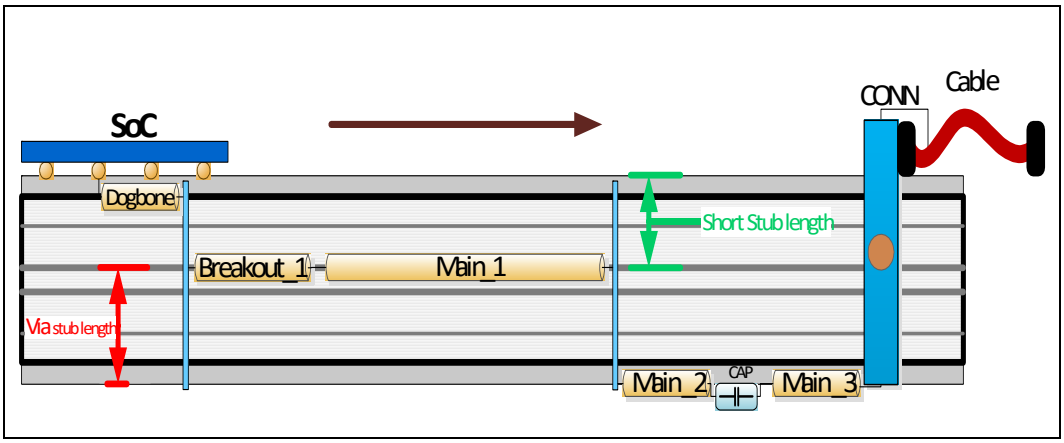
Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline						
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

7.2.2 Cable and Connector Requirements

The SATA 3.0 interface is sensitive to impedance mismatch; therefore, managing the cable and connector impedance mismatch is critical to ensuring proper performance. Analysis has also shown that the cable between two impedance-mismatched connectors is the major source of multiple reflections. This section outlines the high-speed electrical performance requirements for through-hole connector and the cable assemblies along with the through-hole connector footprint recommendations.

7.2.2.1 Using Through-hole Connectors and Cables

Figure 7-7. Routing Topology for the SATAx TX Differential Signals using Stripline to a Through-hole Connector and Cable



Notes:
1. This topology uses a Through-hole (TH) connector.
2. Breakout_1 should not exceed 500 mils.
3. This topology requires a capacitor on the bottom layer only.
4. Capacitor to the TH connector total length should not exceed 250 mils.
5. Breakout_1 and Main_1 are allowed to run on the bottom layer (microstrip) if the transitional via between Main_1 and Main_2 is removed. Breakout_1 and Main_1 routing is not allowed on the top layer (microstrip).
6. For via stub of 60 mils see the table below for routing restrictions.
7. This topology supports a 1 meter SATA spec cable.

Table 7-10. SATAx TX Differential Signals using Stripline to a Through-hole Connector and Cable Layout Recommendations

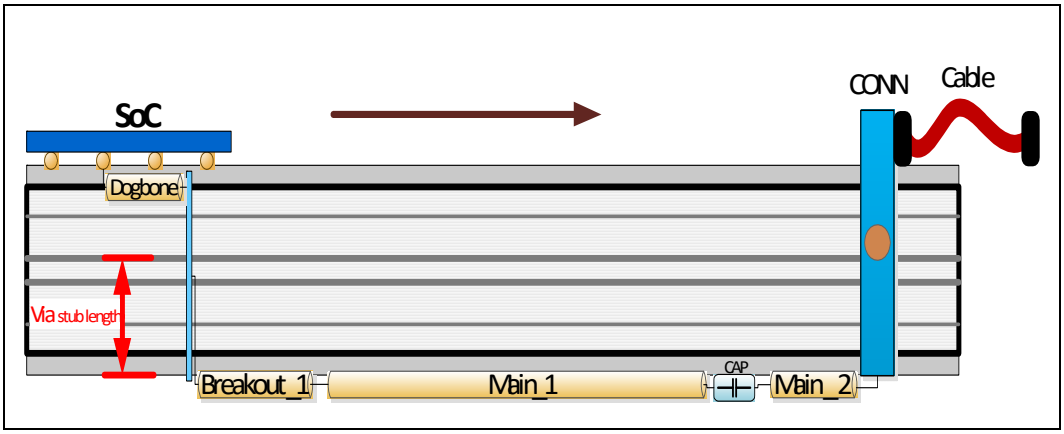
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	stripline	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all				2	2500	6000	GND

Note:
1. The trace-length matching requirement for differential pairs is ≤ 5 mils for each segment.

Table 7-11. SATAx TX Differential Signals using Stripline Layout Spacing Recommendations

Routing Section	Layer	Type (TX)	Type (RX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-8. Routing Topology for the SATAx TX Differential Signals using Microstrip to a Through-hole Connector and Cable



Notes:
1. This topology uses a Through-hole (TH) connector.
2. Breakout_1 should not exceed 500 mils.
3. This topology requires the capacitor to be on the bottom layer only.
4. Capacitor to TH connector total length should not exceed 500 mils.
5. The ac capacitor placement should within 500 mils of either the SoC or the SM-HDD connector.
6. This topology supports a 1 meter SATA spec cable.

Table 7-12. SATAx TX Differential Signals using Microstrip to a Through-hole Connector and Cable Layout Recommendations

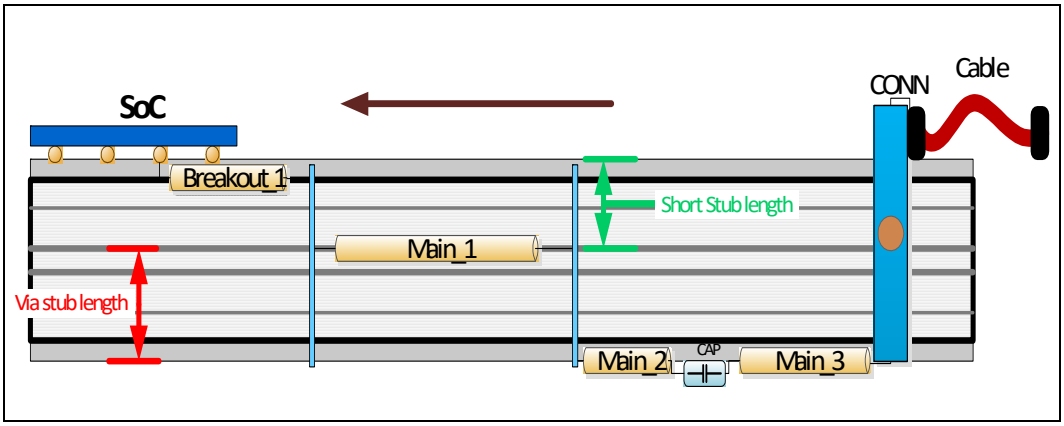
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline							
MAIN_1+MAIN_2	microstrip		5.0	85 ± 15%				
	stripline							
MAIN_1	microstrip	50						
MAIN_2	microstrip					0	500	
Cap, HDD Conn						0	250	
Entire Signal	all				1	2500	6000	GND

Notes:
1. The trace-length matching requirement for differential pairs is ≤ 5 mils for each segment.

Table 7-13. SATAx TX Differential Signals using Microstrip Layout Spacing Recommendations

Routing Section	Layer	Type (TX)	Type (RX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline						
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-9. Routing Topology for the SATAx RX Differential Signals using a Through-hole Connector and Cable



Notes:

1. This topology uses a Through-hole (TH) connector.
2. Breakout_1 should not exceed 500 mils.
3. This topology requires a capacitor on the bottom layer only.
4. Breakout_1 and Main_1 are also allowed to route on the bottom layer if the transitional via between Man_1 and Main_2 is removed.
5. Breakout_1 and Main_1 are also allowed to route on the top layer if all transitional vias between the dogbone and Breakout_1 are removed.
6. Connector to capacitor total length should not exceed 250 mils.
7. For via stub of 60 mils see the table below for routing restrictions.
8. This topology supports a 1 meter SATA spec cable.

Table 7-14. SATAx RX Differential Signals using a Through-hole Connector and Cable Layout Recommendations

Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	microstrip [2]	0						
	stripline [1,3]	50						
Breakout_1	microstrip [2]		3.5			0	500	GND
	stripline							
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	microstrip [2]	0						
	stripline [1,3]	50						
MAIN_2	microstrip [4]					0	125	
MAIN_3	microstrip [4]					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all [5]				2	2500	6000	GND

Notes:
1. This topology does not support via stubs longer than 60 mils.
2. Breakout_1 and Main_1 are also allowed on the bottom layer if the transitional via between Main_1 and Main_2 is removed.
3. If via stub lengths are 60 mils then the maximum length is 5”.
4. This topology requires Main_2 and Main_3 to be on the bottom layer (microstrip).
5. This topology supports a 1 meter SATA spec cable.

Table 7-15. SATAx RX Differential Signals using a Through-hole Connector and Cable Layout Spacing Recommendations

Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

7.2.2.2 Through-hole Electrical Performance Requirements

Surface-mount or through-hole connectors can be used for the SATA 6 Gb/s speeds as long as the requirements outlined in Table 7-16 are met.

Table 7-16. SATA 6 Gb/s Through-hole Connector and Cable Assembly Electrical Requirements

Parameter	Requirement	Measurement Description
Cable Differential Impedance	90 - 100 Ω with a rise time of 50 ps (20-80%) entering the connector	Applies to the raw cable and is measured on a mated-cable assembly, away from the mated-connector discontinuities.
Mated Connector Differential Impedance	78 to 108 Ω with a rise time of 50 ps (20-80%) entering the connector	Measured on a mated cable assembly.
Cable Assembly Differential Insertion Loss	≤-4.2 dB, up to 3 GHz	Frequency-domain measurement, does not include test fixture. The cable assembly length shall be ≤ 1 meter.
Cable Assembly Differential Near-End Crosstalk	-32 dB maximum, up to 3 GHz	Frequency-domain measurement, does not include test fixture.
Cable Assembly intraPair Skew	10 ps maximum	Delay difference between the + and - signals in a differential pair.

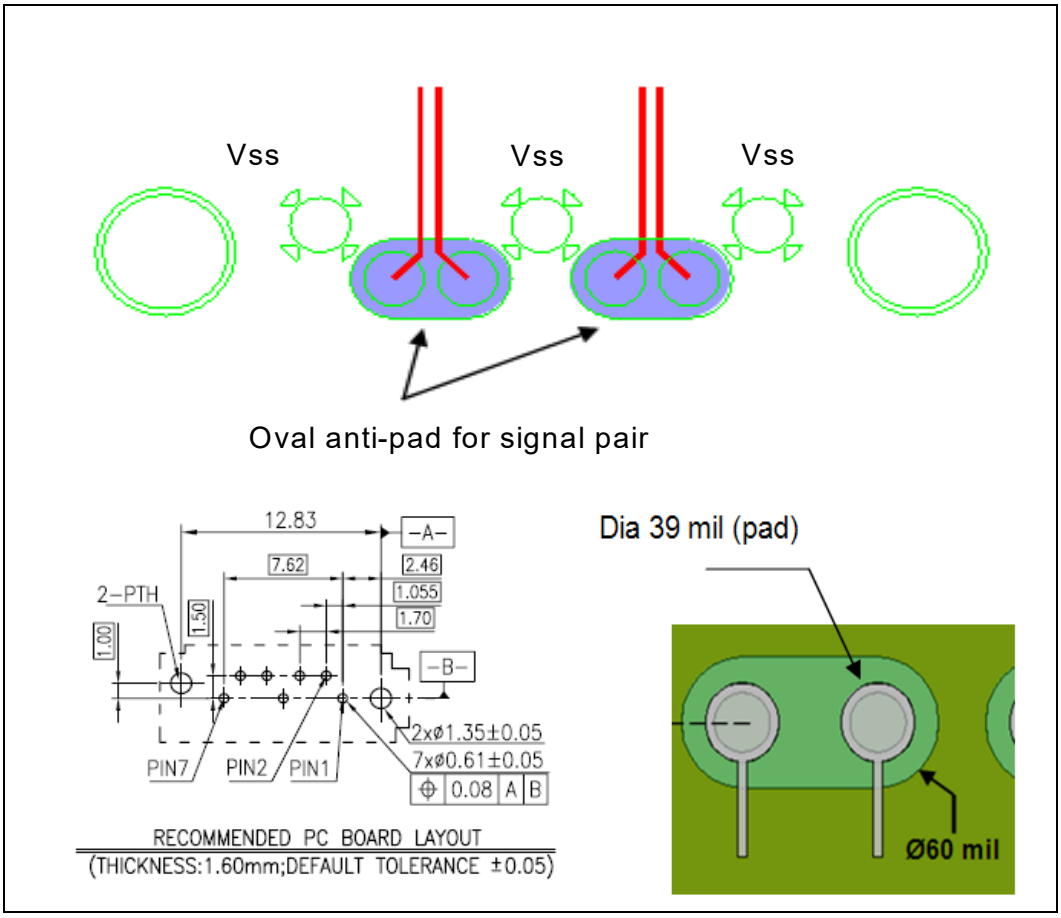
Notes:
1. The parameters are tested with each different pair of the connector and cable assembly under test.
2. The target impedance for the mated-connector impedance is 90 Ω.
3. The parameters are tested with a quality test fixture with the signals launched into the connector on the top of the PCB (long stub for through-hole connector).
4. The test fixture has the capability of verifying the rise time entering the connector and removing the fixture loss effect on the differential insertion loss and the differential near-end crosstalk.

7.2.2.3 Through-hole Connector Footprint Recommendations

Figure 7-10 shows the recommended 7-pin, vertical through-hole SATA 6 Gb/s connector footprint and the pad and antipad dimensions. The following points are noted about the through-hole connector footprint:

- The SATA 6 Gb/s connector footprint is different from the one for the existing SATA Gen2 connector. This is done to ensure that high-performance SATA connectors are used with the SATA 6 Gb/s interface.
- The through-hole, pad, and antipad sizes are chosen to prevent the through-hole impedance from being too low. The finished through-hole diameter is 0.61 mm (24 mils); the pad diameter is 0.99 mm (39 mils); and antipad diameter is 1.52 mm (60 mils).
- The oval-shaped antipad (GND void), shown in Figure 7-10, reduces the through-hole capacitance when the traces enter the connector on the top of the PCB (maximum through-hole stub length). When the traces, however, enter the connector on the bottom of the PCB (minimum through-hole stub length), the regular circular antipad diameter of 60 mils is used.

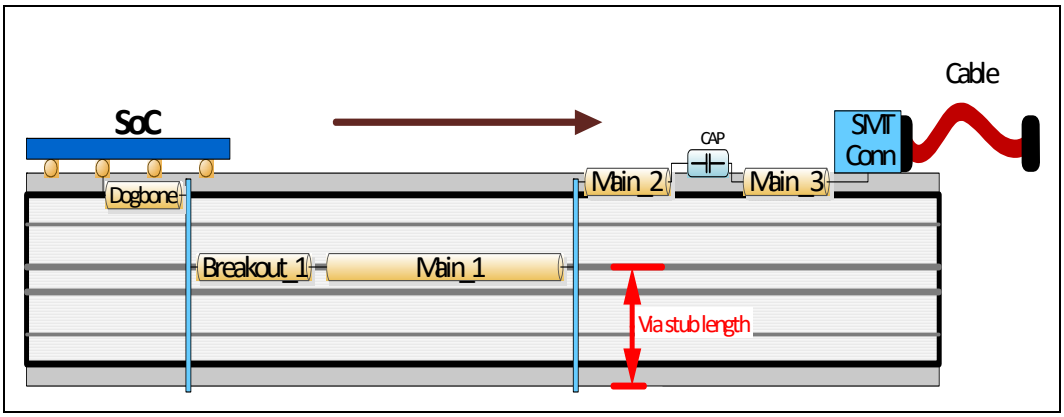
Figure 7-10. SATA 6 Gb/s Through-hole Connector Footprint and Pad/Antipad Size



7.2.3 Surface-Mount (SMT) Connector and Cable Layout Recommendations

The SATA 6 Gb/s Surface-Mount (SMT) connector footprint has the same footprint as the SATA Gen2 connector but voiding the GND/power plane underneath the SMT signal pads is necessary to minimize the impedance mismatch caused by the SMT pads. The size and shape of the voiding can be the same size/shape as the signal pads.

Figure 7-11. Routing Topology for the SATAx TX Differential Signals using Stripline to a Surface Mount (SM) Connector and Cable



Notes:
1. This topology uses a SM connector.
2. Breakout_1 should not exceed 500 mils.
3. This topology requires a capacitor on the top layer only.
4. Capacitor to the SM connector total length should not exceed 250 mils.
5. Breakout_1 and Main_1 are allowed to run on the bottom layer (microstrip).
6. For via stub of 60 mils see the table below for routing restrictions.
7. This topology supports a 1 meter SATA spec cable.

Table 7-17. SATAx TX Differential Signals using Stripline to a Surface Mount Connector and Cable Layout Recommendations

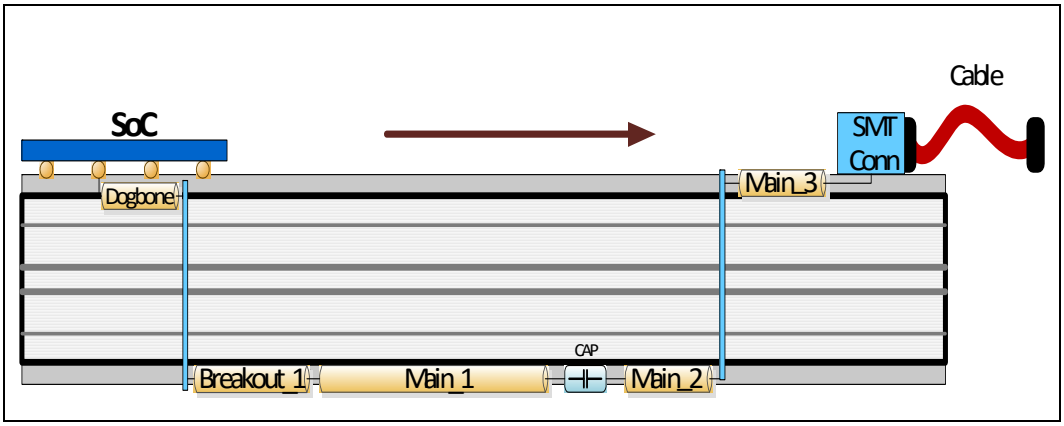
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline	50						
Breakout_1	microstrip		3.5			0	500	GND
	stripline		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	stripline	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all				2	2500	6000	GND

Notes:
1. The trace-length matching requirement for differential pairs is ≤ 5 mils for each segment.

Table 7-18. SATAx TX Differential Signals using Stripline Layout Spacing Recommendations

Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-12. Routing Topology for the SATAx TX Differential Signals using Microstrip to a Surface Mount (SM) Connector and Cable



Notes:
1. This topology uses a SM connector.
2. Breakout_1 should not exceed 500 mils.
3. Capacitor to SM connector's total length ≤ 500 mils.
4. The ac capacitor placement can be close to the SM connector or close to the SoC package (≤ 500 mils for either option).
5. This topology supports a 1 meter SATA spec cable.

Table 7-19. SATAx TX Differential Signals using Microstrip to a Surface Mount Connector and Cable Layout Recommendations

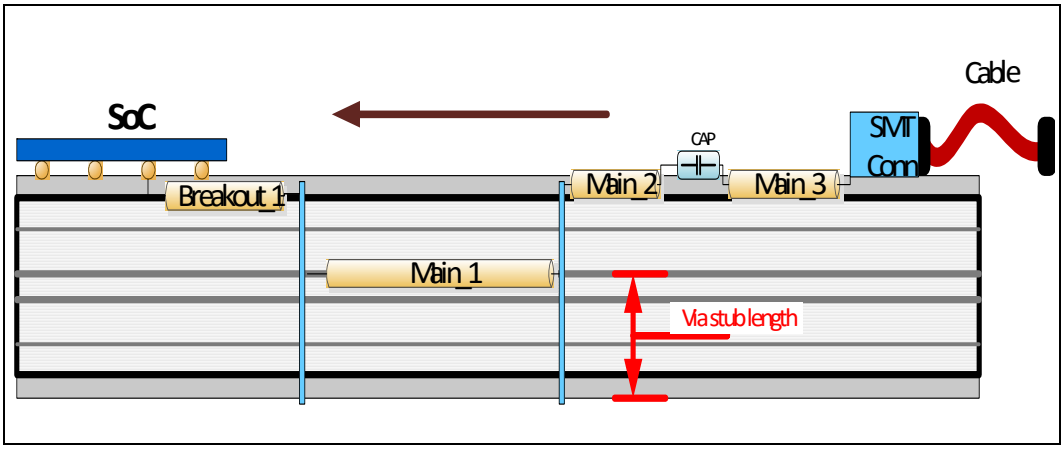
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	stripline							
Breakout_1	microstrip		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline							
MAIN_1	stripline							
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all				2	2500	6000	GND

Notes:
1. The trace-length matching requirement for differential pairs is ≤ 5 mils for each segment.

Table 7-20. SATAx TX Differential Signals using Microstrip Layout Spacing Recommendations

Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-13. Routing Topology for the SATAx RX Differential Signals using Stripline to a Surface Mount (SM) Connector and Cable



Notes:

1. This topology uses a SM connector.
2. Breakout_1 should not exceed 500 mils.
3. Breakout_1 and Main_1 are also allowed to route on the bottom layer (microstrip).
4. Breakout_1 and Main_1 are also allowed to route on the top layer if all transitional vias are removed.
5. Connector to capacitor total length should not exceed 250 mils.
6. For via stub of 60 mils see the table below for routing restrictions.
7. This topology supports a 1 meter SATA spec cable.

Table 7-21. SATAx RX Differential Signals using Stripline to a Surface Mount Connector and Cable Layout Recommendations

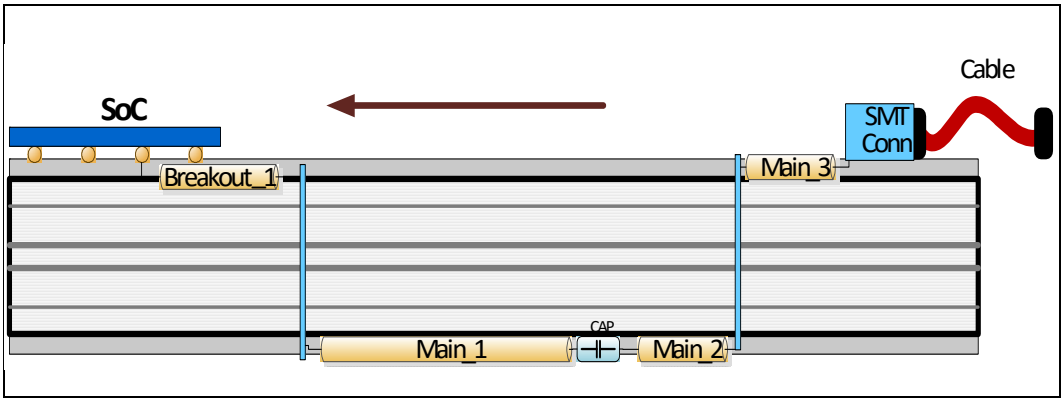
Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	microstrip	0						
	stripline [1,3]	50						
Breakout_1	microstrip [2]		3.5			0	500	GND
	stripline							
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline		5.3	85 ± 10%				
MAIN_1	microstrip [2]							
	stripline [1,3]	50						
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn						0	250	
Entire Signal	all [4]				2	2500	6000	GND

Notes:
1. This topology does not support via stubs longer than 60 mils.
2. Breakout_1 and Main_1 are also allowed on the bottom layer (microstrip).
3. If via stub lengths are 60 mils then the maximum length is 5".
4. This topology supports a 1 meter SATA spec cable.

Table 7-22. SATAx RX Differential Signals using Stripline Layout Spacing Recommendations

Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline	2H	3H	7H	4		
MAIN_1	microstrip	7H	9H	9H	7		
	stripline	5H	7H	7H	6.2		
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

Figure 7-14. Routing Topology for the SATAx RX Differential Signals using Microstrip to a Surface Mount (SM) Connector and Cable



Notes:
1. This topology uses a SM connector.
2. Breakout_1 should not exceed 500 mils.
3. Connector to capacitor total length should not exceed 375 mils.
4. This topology supports a 1 meter SATA spec cable.

Table 7-23. SATAx RX Differential Signals using Microstrip to a Surface Mount Connector and Cable Layout Recommendations

Routing Section	Layer	Max Via Stub Length (mils)	Trace Width (mils)	Trace Imp.	Total Via count	Length (mils)		Reference
						min	max	
Dogbone	microstrip	0						
Breakout_1	microstrip		3.5			0	500	GND
MAIN_1+MAIN_2+MAIN_3	microstrip		5.0	85 ± 15%				
	stripline							
MAIN_1	microstrip							
MAIN_2	microstrip					0	125	
MAIN_3	microstrip					0	250	
Cap, HDD Conn	microstrip [1]					0	375	
Entire Signal	all [2]				2	3000	6000	GND

Notes:
1. Connector to capacitor total length should not exceed 375 mils.
2. This topology supports a 1 meter SATA spec cable.

Table 7-24. SATAx RX Differential Signals using Microstrip Layout Spacing Recommendations

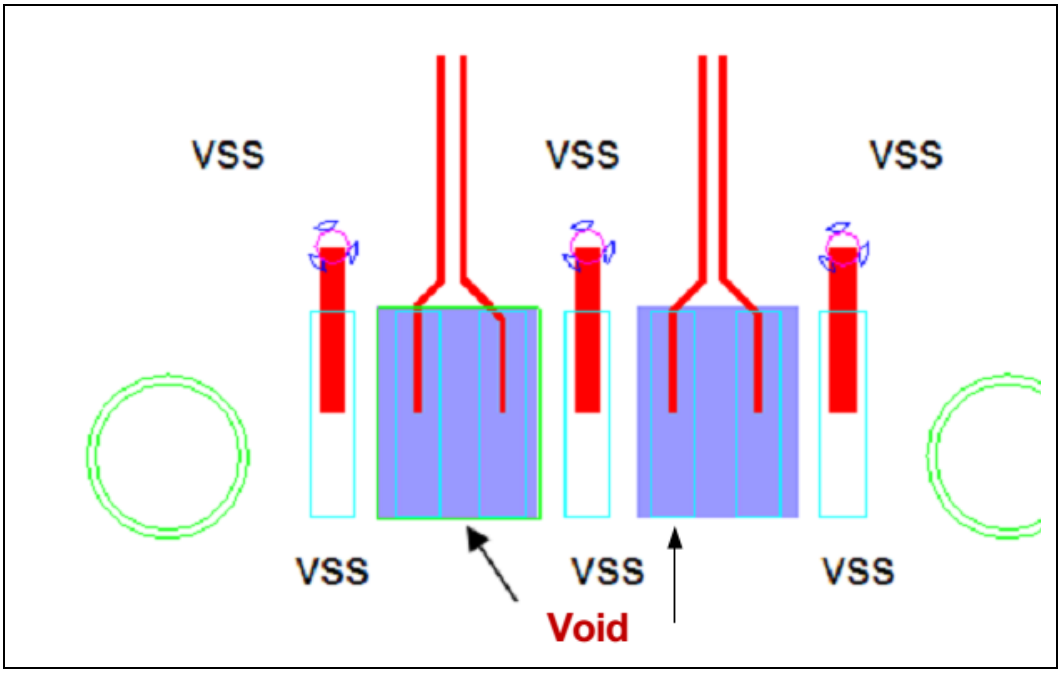
Routing Section	Layer	Type (RX)	Type (TX)	Other Signals	Differential	Distance to plane edge	Distance to voids
		Pair-to-Pair (mils)	Pair-to-Pair (mils)	Pair-to-Pair (mils)	P/N Spacing (mils)		
Breakout_1	microstrip	3H	9H	9H	4		
	stripline						
MAIN_1	microstrip	7H	9H	9H	7		
	stripline						
MAIN_2	microstrip	7H	9H	9H	7		
MAIN_3	microstrip	7H	9H	9H	7		
Entire Signal	all					20H	5H

7.2.3.1 SATA 6 Gb/s Surface-Mount (SMT) Connector Footprint Recommendations

The SATA 6 Gb/s Surface-Mount (SMT) connector footprint has the same footprint as the SATA Gen2 connector but voiding the GND/power plane underneath the SMT signal pads is necessary to minimize the impedance mismatch caused by the SMT pads. The size and shape of the voiding can be the same size/shape as the signal pads.

Note: The surface mount M.2 connector is also supported for Direct Attach drives.

Figure 7-15. SATA 6G SMT Connector Footprint and GND Voiding



7.3 Serial ATA AC Coupling Requirements

The SoC requires AC coupling capacitors for both the Tx and Rx SATA differential pairs. See Figure 7-1. The series capacitors are placed at any point on the traces between the processor and the serial ATA connector. Intel recommends that they are close to the connector for optimal signal quality. The capacitors must be of type 0402. The Layout needs to minimize the placement mismatch within a differential pair between the capacitors. The distance between the processor and the capacitor on the P signal is identical to the distance between the processor and the capacitor on the N signal for the same pair.

Table 7-25. AC Coupling Capacitor

Signal name	Capacitor	Figure	Notes
SATA0_TX_DP[7:0] SATA0_TX_DN[7:0] SATA1_TX_DP[7:0] SATA1_TX_DN[7:0]	C = 1 – 10 nF ± 20%	Figure 7-1	1
SATA0_RX_DP[7:0] SATA0_RX_DN[7:0] SATA1_RX_DP[7:0] SATA1_RX_DN[7:0]	C = 1 – 10 nF ± 20%	Figure 7-1	1

Note:
1. Intel recommends to use 0402-size capacitors.

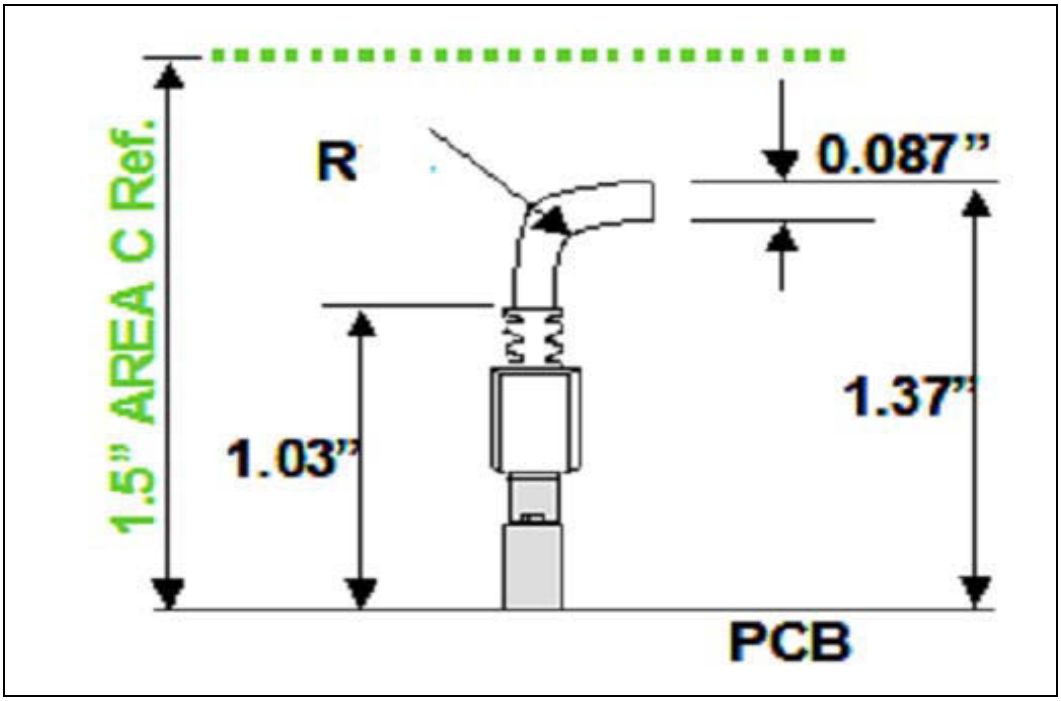
7.4 SATA Optimization Guidelines

SATA Host Connector Placement Considerations

Applicable keepout regions must be considered in the layout of the board when placing SATA host connectors.

The following figure shows an example cable and the height required for bending the cable to a 90° bend. This can be used as an example when considering height obstruction regions.

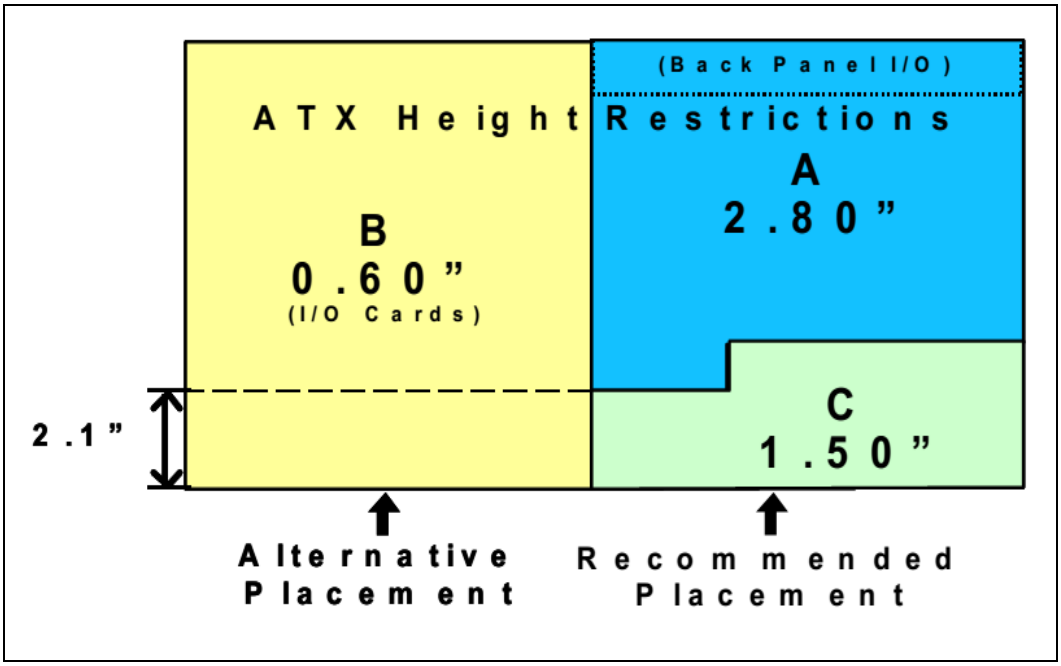
Figure 7-16. SATA Cable 90-Degree Bend Height Example



Note: "R" in the figure above represents the minimum bend radius of the SATA cable. Please contact the cable vendor for minimum bend radius limits.

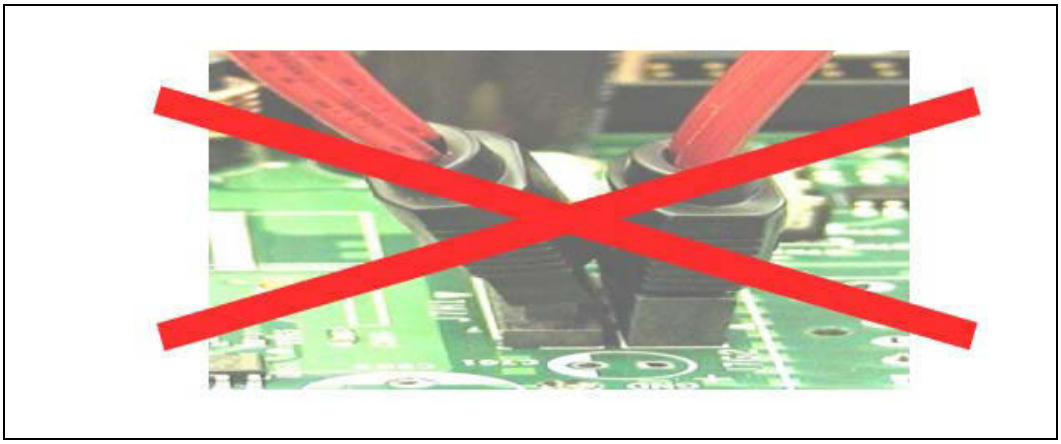
The next figure shows the ATX Specification, Rev 2.1 height restriction regions. With the example cable, Area C is the recommended placement region to allow the cable to bend fully to avoid any obstructions.

Figure 7-17. SATA Host Connector Placement Region Recommendations



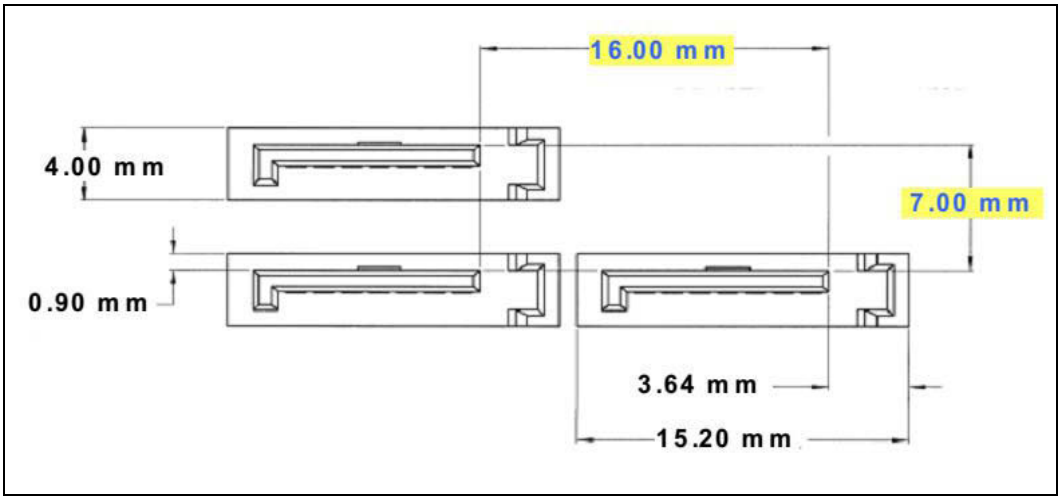
An additional consideration is the relative placement to other SATA host connectors as well as neighboring parts and devices on the motherboard. The following figure shows an example of a case where two adjacent SATA host connectors were placed too close to one another.

Figure 7-18. Example of Poor Host Connector Placement



The last figure shows the minimum host connector spacings recommended in the SATA Specification.

Figure 7-19. Minimum Host Connector Placement Spacing (from SATA Specification)



Transitional Via Recommendations

Transitional vias will use oval-shaped antipads on all plane layers. This antipad can be created using a rectangular-shaped void to overlap with the usual round-shaped via antipad. The vias must also have a symmetrical trace entry.

Below are the transitional differential via pad stack details.

Figure 7-20. SATA 6 Gb/s Transitional Via Layout

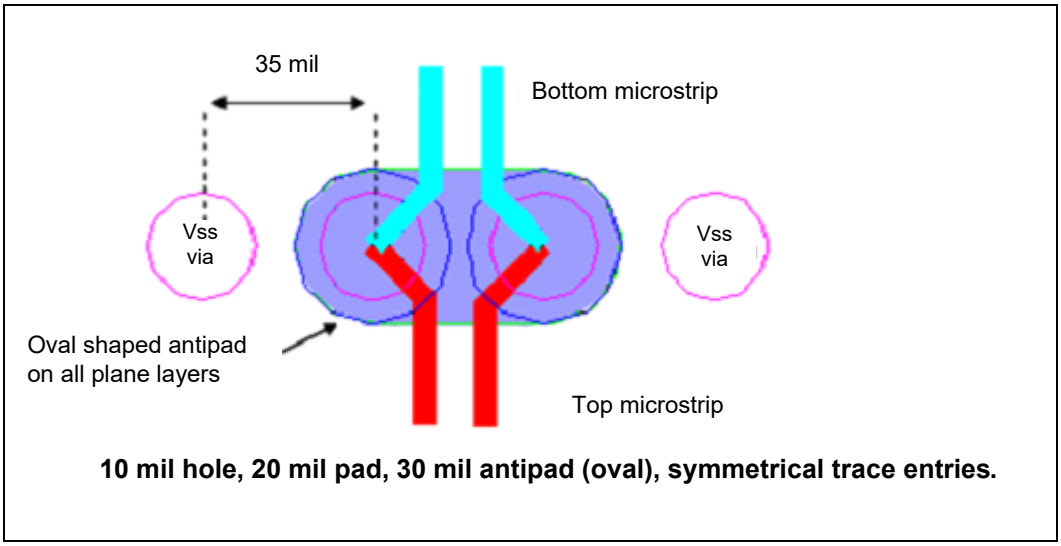


Table 7-26. SATA 6 Gb/s Transitional Via Layout Recommendations

Parameter	Requirement
Via size	10 mils
Pad size	20 mils
Oval-shaped antipad size	30 mils
Via-to-Via distance (from center)	35 mils
Note: 1. For PCB and breakout pin field via routing, follow generic rule.	

Byte Lane Placement

It is helpful for testability to route the TX and RX pairs for a given port on the same layer and group together to ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.

7.5 Miscellaneous Signals

There is a signal called SATAx_LED_N to indicate SATA device activity. Intel recommends to implement the circuit in Figure 7-21 to show hard drivers activity by using this signal.

SATAx_LED_N is an open-collector output and requires a weak external pull-up (4.7 kΩ to 10 kΩ) to V3P30. When SATAx_LED_N is low, it indicates the hard drive LED is light on and shows SATA device has activity. When SATAx_LED_N is in tri-state, the hard drive LED is off and shows no SATA device activity.

Figure 7-21. SATAx_LED_N Circuitry Example

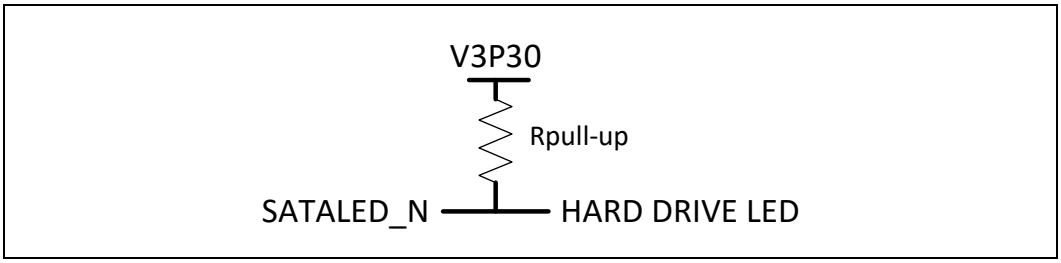


Figure 7-22. SATA_PDETECT[1:0] Routing Illustration: SoC CMOS Input

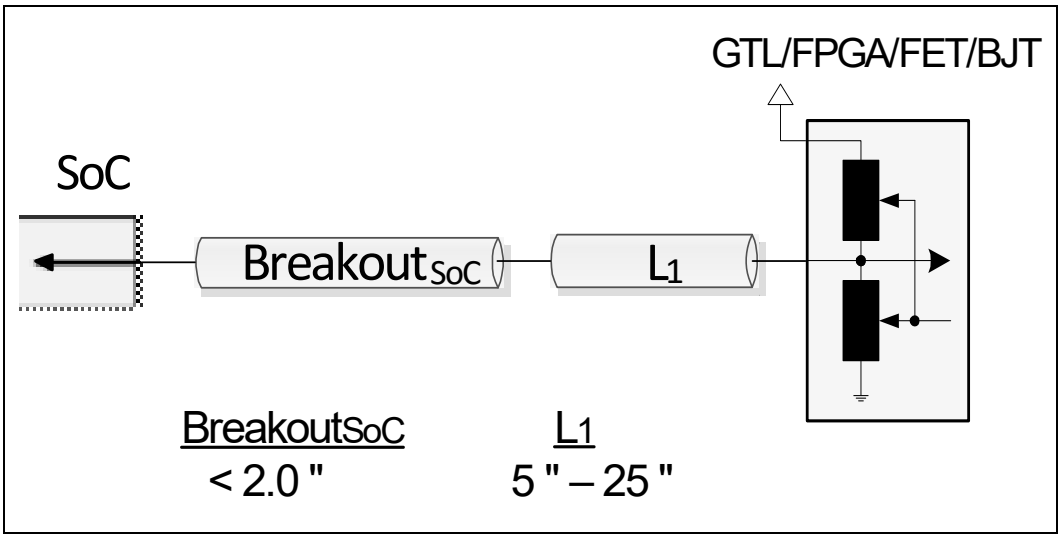


Figure 7-23. SATAx_SCLK, SATAx_SLD, SATAx_SDOUT Routing Illustration: SoC Daisy Chain Open Drain Output

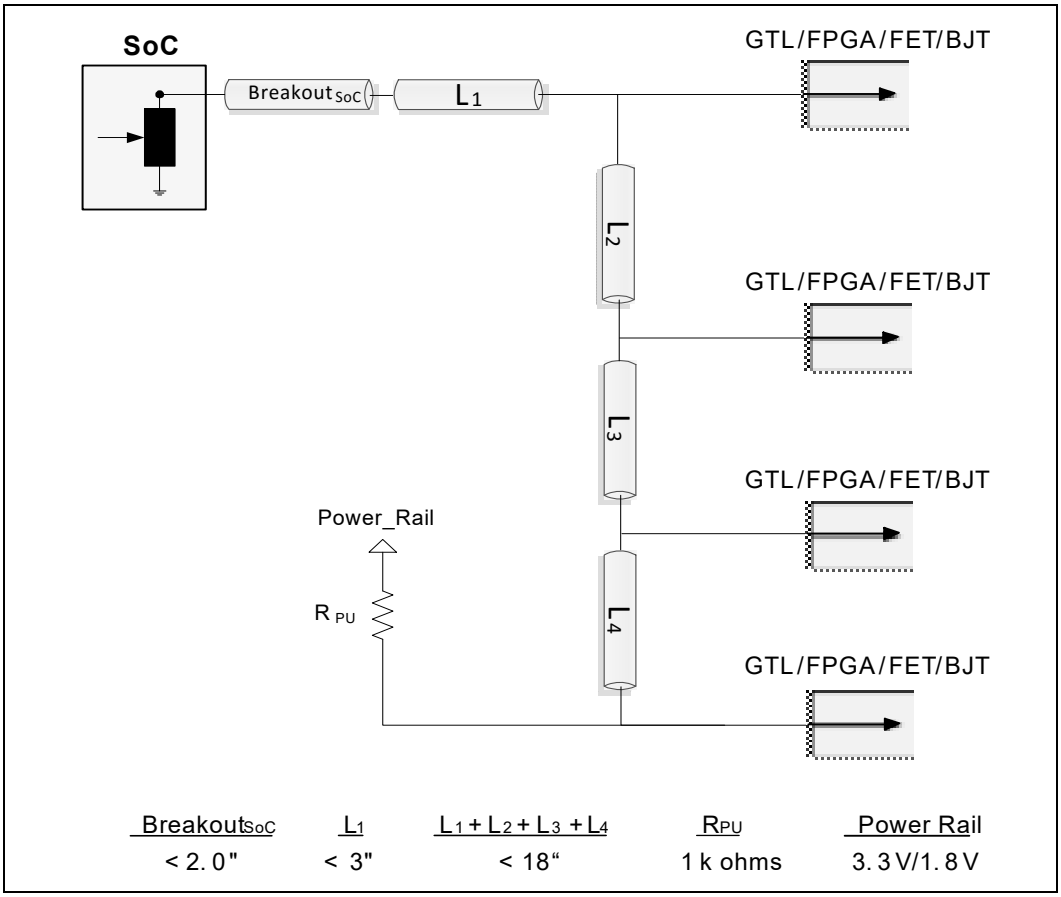


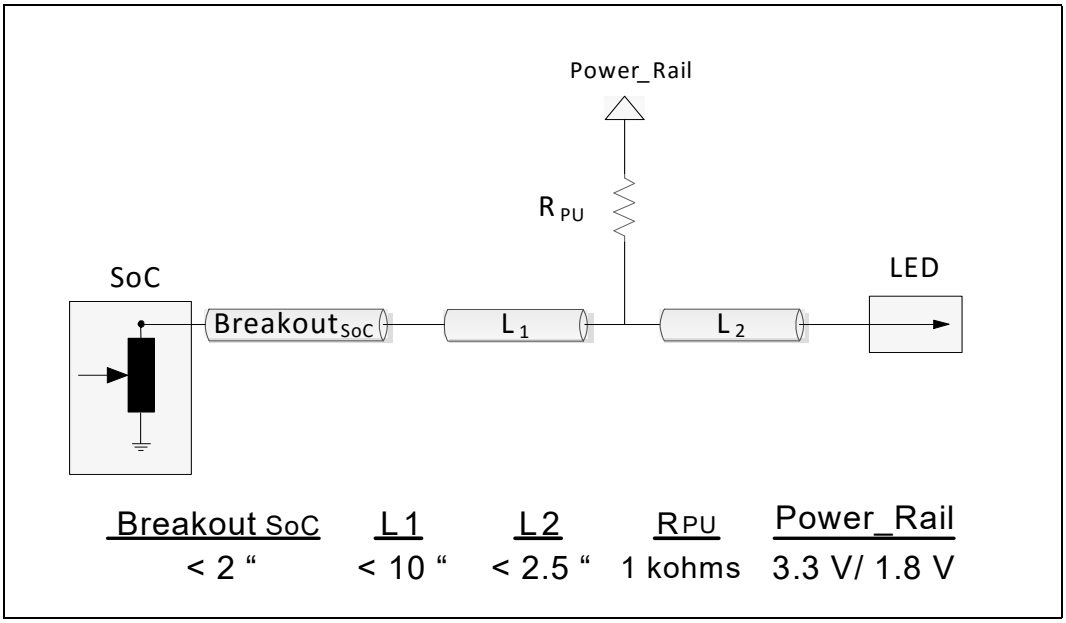
Table 7-27. SATAx_SCLK, SATAx_SLD, SATAx_SDOUT SoC Daisy Chain Open Drain Output Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	
L1+L2+L3+L4	all			0	18000	
L5	all			0	1000	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Table 7-28. SATAx_SCLK, SATAx_SLD, SATAx_SDOUT Layout Recommendations for Daisy Chain Open Drain Topology: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 7-24. SATAx_LED_N Interface Open Drain Point-to-Point to a Device Down Connections



The power rail pull-up resistor is chosen according to the signal voltage level of the SoC and the power rail availability at the different platform power states to avoid current leakages.

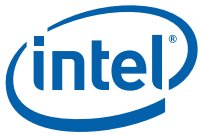


Table 7-29. SATAx_LED_N Interface Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	GND
L2				0	2500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 7-30. SATAx_LED_N Interface Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

7.6 Terminating Unused SATA Interface

If a SATA port(s) is not implemented then SATA[*x*]RXp/n and SATA[*x*]TXp/n signals may be left unconnected. SATA Power, Ground, and IREF signals must be connected as defined even if zero SATA ports are implemented.

- The following signals are left as no connects:
  SATA0_RX_DP/DN[7:0], SATA0_TX_DP/DN[7:0], SATA1_RX_DP/DN[7:0], SATA1_TX_DP/DN[7:0], SATAx_LED_N
- Disable the SATA function via the BIOS.

7.7 SATA Interface Re-driver

SATA signal re-driver might be needed on some special design. The detail design guidelines is not described here. Please refer to *Repeater Assessment Methodology for Intel® Server Platforms Specification*. The document describes a methodology that re-driver component manufacturers and customers follow to evaluate and report re-driver performance from a signal integrity point of view to satisfy design needs.

§ §

8 USB Interfaces

The SoC supports up to four USB 3.0 or four USB 2.0 compliant ports. The USB 3.0 Super Speed data interface is dual-simplex, four-wire differential signals which are separate from the USB 2.0 signals.

Table 8-1. Signal Names and Descriptions

Signal Names	Direction	Shared	Description
USB3_TX_DP[3:0] USB3_TX_DN[3:0]	O, Differential	Yes	USB 3.0 Transmit Data: Differential output signals from the USB Combo Controller to the FIA/PHY.
USB3_RX_DP[3:0] USB3_RX_DN[3:0]	I, Differential	Yes	USB 3.0 Receive Data: Differential input signals to the USB Combo Controller from the FIA/PHY.
USB2_DP[3:0] USB2_DN[3:0]	I,O, Differential	No	USB 2.0 Transceiver Data: Differential bi-directional signal pins.
USB_OC_N	I	No	USB Over Current. Active low input signal from the platform board that alerts the SoC that a VBUS over-current condition exists.
USB2_COMP	I	No	Compensation: The platform board must provide a 113 Ω, 1% resistor connected from this pin to VSS.

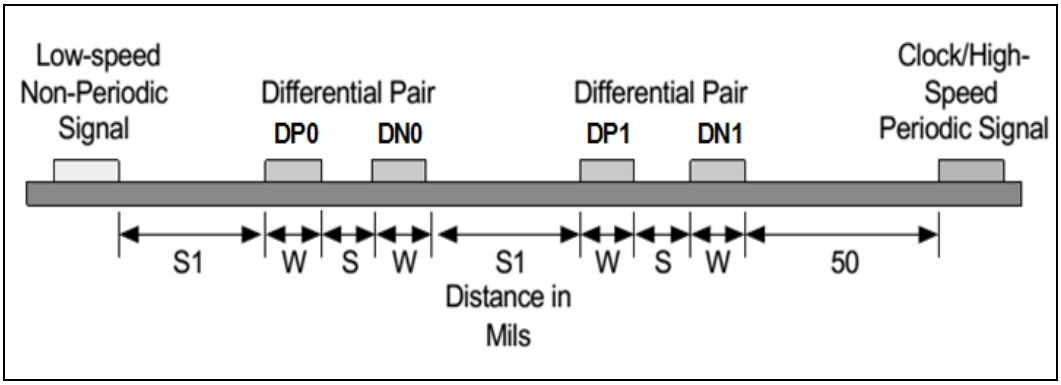
8.1 USB 2.0 Design Guidelines

8.1.1 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 8-1 shows the recommended trace spacing.

- Maintain parallelism between the USB differential signals with the trace spacing which allows a 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) differential impedance. Deviations normally occur due to the package breakout and routing to the connector pins. Ensure the amount and length of the deviations are kept to a minimum.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup. The target is 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) differential impedance.
- Minimize the length of any high-speed clock or periodic signal traces that runs parallel to the high-speed USB signal lines. This minimizes crosstalk. The minimum suggested spacing to clock signals is 50 mils.
- Use 5*h* for stripline and 7*h* for microstrip to calculate the minimum spacing between the high-speed USB signal pairs and the other signal traces for optimal signal quality. This helps to prevent crosstalk and is based upon simulations. The constant *h* is defined is the distance to the nearest reference plane.

Figure 8-1. Recommended USB Trace Spacing



8.1.2 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 8-2. USB 2.0 Trace Length Guidelines

Topology	USB 2.0 routing requirement/trace impedance	Breakout	Maximum motherboard trace length (inches)	Maximum internal cable length (inches)	Maximum daughter card trace length (inches)
Back Panel	IL max = -0.79 dB/inch @4 GHz Z= 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) S1 [3] 5h for stripline; 7h for microstrip W, S	W = 3.5 mils S = 4 mils S1 = 4 mils for like pairs; 4*h* or different layers for others L ≤ 500 mils	16	N/A	N/A
Front Panel, Cable Up			6	24	N/A
Front Panel Daughter Card			5	12	1

Notes:

1. These lengths are based upon simulation results and may be updated in the future.
2. W refers to trace width. S refers to inter-pair spacing. S1 refers to spacing between USB 2.0 pairs and any other signals.
3. For breakout, keep S1 as big as possible and the breakout length as short as possible.
4. All lengths are based upon using a common mode choke and an ESD diode (see Section 8.4.1, "Common Mode Chokes for details on the common mode choke).
5. The numbers in Section 8.1, "USB 2.0 Design Guidelines are based on the following simulation assumptions: a USB twisted-pair shielded cable as specified in the Universal Serial Bus (USB) Specification, Rev 2.0.
6. The actual trace width (W) and spacing (S) depends on Insertion loss (IL), impedance (Z) and stackups options described in this document.
7. For front-panel solutions, signal matching is considered from the SoC to the front-panel header.
8. The maximum mismatch within data pairs should not be greater than 20 mils (this includes total channel length matching and per-layer/layer-wise length matching).
9. Signals are ground referenced.
10. If the main routing is stripline, no more than three vias are allowed on the signal path including via under USB connector. If the main routing is microstrip, no more than two vias.
11. Internal cable used for simulation assumed the following loss per meter information: -0.34dB at 120 MHz, -0.49dB at 240 MHz, -0.71dB at 480 MHz, -1.07dB at 1 GHz.

8.1.3 Recommended Front- and Back-Panel Configurations for USB2

Figure 8-2. Recommended Back-Panel Configuration

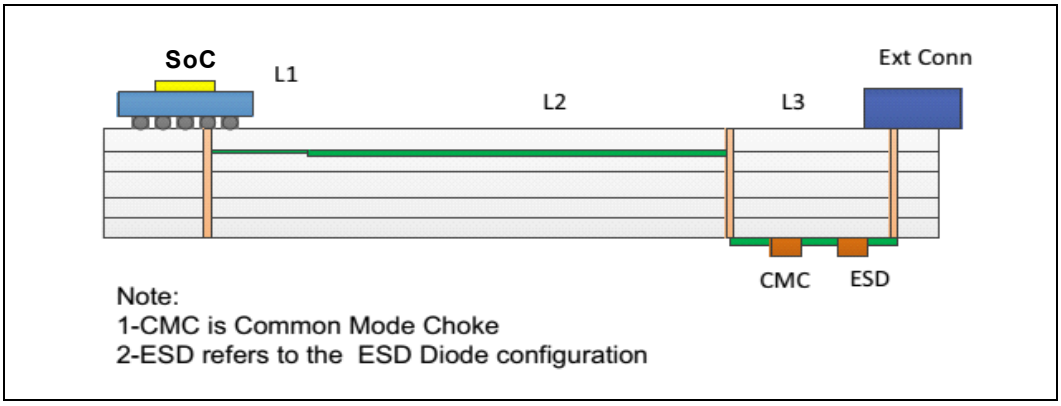


Table 8-3. Recommended Back-Panel Configuration Trace Length Guidelines

Description	L1	L2	L3
Maximum Length	0.5”	16” - (L1+L3)	1”
Allowed Layers	All	All	Top/Bottom

Notes:
1. The placement of the CMC and ESD components is flexible within the 1” allowed.
2. If the main routing is stripline, no more than three vias are allowed on the signal path including via under USB connector. If the main routing is microstrip, no more than two vias.

Figure 8-3. Recommended Front-Panel Cable Up Configuration

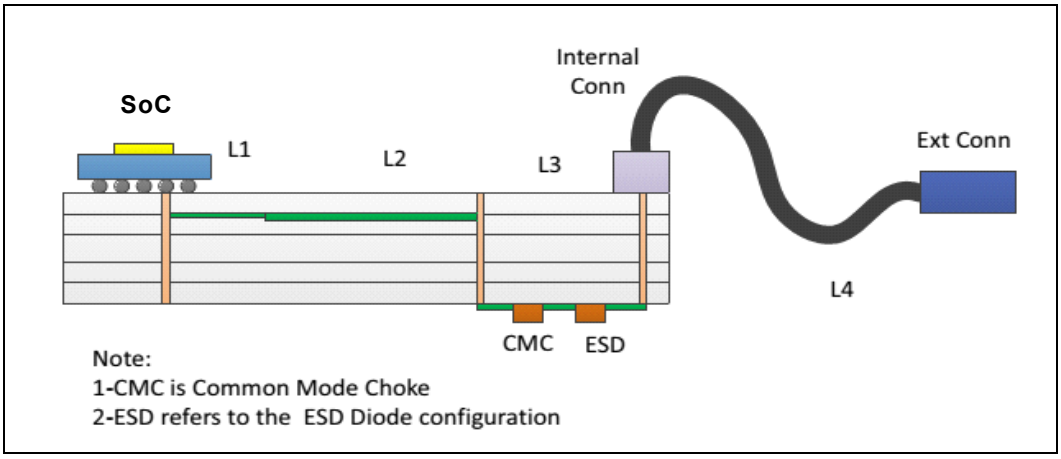


Table 8-4. Recommended Front-Panel Cable Up Configuration Trace Length Guidelines

Description	L1	L2	L3	L4 (internal cable)
Maximum Length	0.5”	6” - (L1+L3)	1”	24”
Allowed Layers	All	All	Top/Bottom	NA

Notes:
1. The placement of the CMC and ESD components is flexible within the 1” allowed.
2. If the main routing is stripline, no more than three vias are allowed on the signal path including via under USB connector. If the main routing is microstrip, no more than two vias.
3. Intel recommends using low-delay cables when implementing USB 2.0 front panel- cable up; otherwise the 3-ns delay budget defined in the USB 2.0 specification might be violated.

Figure 8-4. Recommended Front-Panel Daughter Card Configuration

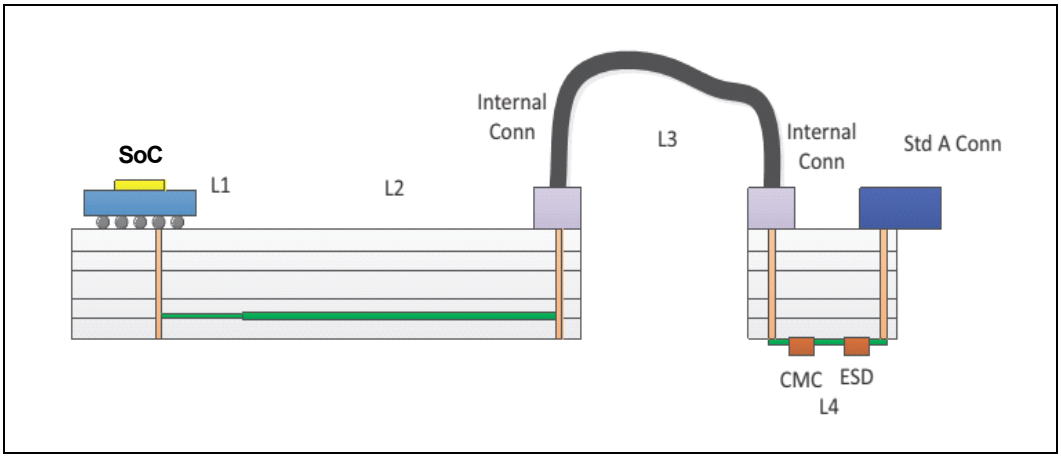


Table 8-5. Recommended Front-Panel Daughter Card Trace Length Guidelines

Description	L1	L2	L3	L4
Maximum Length	0.5”	5” - L1	12”	1”
Allowed Layers	Via stub < 10 mils	Via stub < 10 mils	N/A	Bottom

Notes:
1. The placement of the CMC and ESD components is flexible within the 1” allowed.
2. CMC, ESD and L4 routing are recommended to be placed at Bottom Layer in Daughter Card for optimal performance.

8.1.4 SoC to BMC Routing Guidelines

For a USB 2.0 topology connecting the SoC to a BMC routing without Common Mode Choke and ESD protection diode is allowed. The maximum routing length requirement is 20 inches and the maximum number of vias allowed is 4. The length matching within a differential pair should be within 5 mils.

8.1.5 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help to maximize signal quality and minimize EMI problems.

- Place the SoC and major components on the unrouted board first. With the minimum trace lengths, route the high-speed clock, the periodic signals, and the USB 2.0 differential pairs. Maintain the maximum distance between the high-speed clocks/periodic signals to the USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB 2.0 signals are *ground referenced.*
- Route the USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- If a 90-degree turn cannot be avoided, use two 45-degree turns or an arc instead of making a single, 90-degree turn. This reduces reflections on the signal by minimizing the impedance discontinuities.
- Do not route the USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.
- Avoid stubs on the high-speed USB signals. Stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line is no greater than 100 mils.
- Route all traces over the continuous planes with no interruptions. Avoid crossing over the anti-etch. Crossing over an anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Avoid changing layers with the USB 2.0 traces as much as practical. Changing the layers is preferable to avoid crossing a plane split. See Section 8.1.6, "Referencing (Anti-Etch) for further details.
- Separate the signal traces into similar categories and route them together (e.g., routing differential pairs together).
- Keep the USB 2.0 signals clear of the core logic set. High-current transients are produced during internal state transitions and are difficult to filter out.
- Follow the 20 x H (height above the plane) thumb rule. Keep the traces at least 20 x H away from the edge of the plane (Vcc or GND depending on the plane the trace is over).
- Minimize the length of the high-speed clock and the periodic signal traces that run parallel to the USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.

8.1.6 Referencing (Anti-Etch)

- Avoid anti-etch on the GND plane.
- Use the following guidelines for the Vcc planes.
  - Traces do not cross anti-etch; it greatly increases the return path for those signal traces. This applies to the USB 2.0 signals, the high-speed clocks, and the signal traces, as well as the slower signal traces, which are coupled to them. USB signaling is not purely differential in all speeds (i.e., the full-speed, single-ended zero is the common mode).
  - Avoid routing the USB 2.0 signals within 25 mils of any anti-etch to avoid coupling to the next split or radiation from the edge of the PCB.

When breaking the signals out from the packages, avoiding crossing the plane splits, or changing the signal layers is difficult. Changing the signal layers is preferable to crossing the plane splits if a choice has to be made between one or the other.

If crossing a plane split is unavoidable, the proper placement of the stitching capacitors minimizes the adverse effects on EMI and signal quality caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge the voltage plane splits close to where the high-speed signals or clocks cross the plane split. The capacitor ends tie to each plane separated by the split. They are also used to bridge or bypass the power and ground planes close to the places where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates the V5REF and Vcc3.3 planes have a stitching capacitor placed near any high-speed signal crossing. One side of the capacitor ties to V5REF and the other side ties to Vcc3.3. Stitching capacitors provide a high-frequency current return path across the plane splits. They minimize the impedance discontinuity and the current loop area created when crossing a split plane.

8.2 Front Panel Solutions

8.2.1 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the Universal Serial Bus (USB) Specification, Rev 2.0.

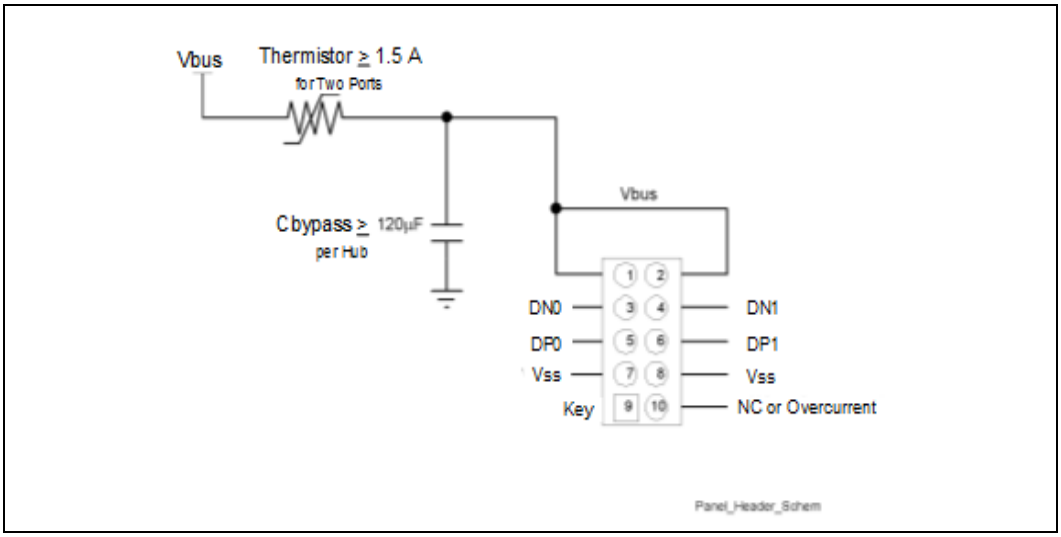
8.2.2 Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in Table 8-6 and schematic shown in Figure 8-5.

Table 8-6. Front Panel Header Pinout

Pin	Description
1	Vbus (+5V ± 5%)
2	Vbus (+5V ± 5%)
3	DN0
4	DN1
5	DP0
6	DP1
7	Vss
8	Vss
9	KEY
10	No connect or overcurrent sense.

Figure 8-5. Front Panel Header Schematic



It is recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage for the following reasons:

- This protects the motherboard from damage in the case where an unfused front panel cable solution is used.
- It also provides protection from damage if an unkeyed cable is inadvertently plugged onto the front panel USB connector.

It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between VBUS and ground.

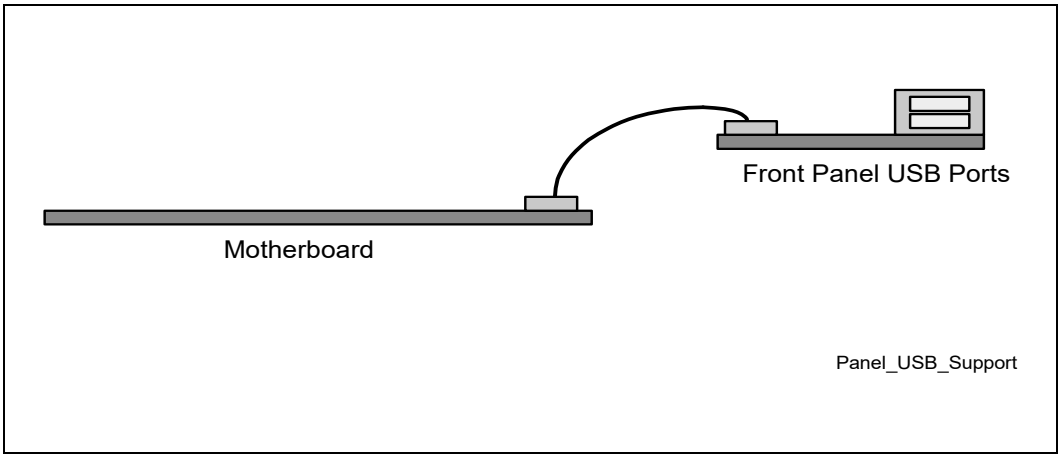
8.2.3 Routing Considerations

- Traces or surface shapes from VCC to the thermistor, to C_{BYPASS} and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.
- Power and ground nets should have double vias.
- Trace lengths should be kept as short as possible.

8.2.4 Front Panel Daughter Card Considerations

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 8-6 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information, refer to the Front Panel I/O Connectivity Design Guide (Look for I/O Connectivity in formfactors.org) available at: http://www.formfactors.org/.

Figure 8-6. Motherboard Front Panel USB Support

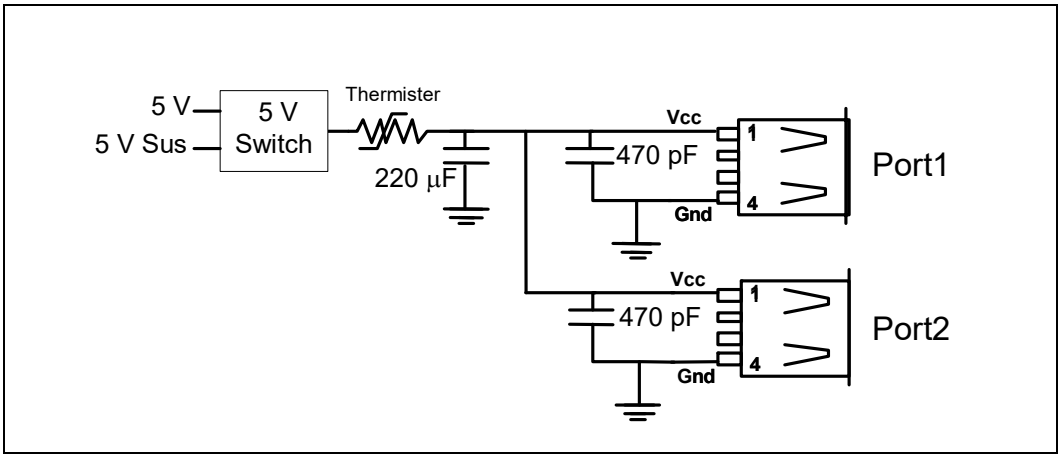


When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a daughter card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

8.3 USB Port Power Delivery

The following is a suggested topology for the power distribution of VBUS to the USB ports. Circuits of this kind provide two types of protection during dynamic attach and detach situations on the bus: the inrush current limiting (droop) and the dynamic detach flyback protection. These two different situations require both a bulk capacitance (droop) and a filtering capacitance (for the dynamic detach flyback voltage filtering). Minimize the inductance and resistance between the coupling capacitors and the USB ports. Place the capacitors close to the port. Intel recommends implementing a plane to carry power to the USB ports. Otherwise make the power-carrying traces as wide as possible. The traces should be wide enough that the system fuse blows in an over-current event. For example, the power-carrying traces should be wide enough to carry 1.5A when the system fuse is rated at 1A.

Figure 8-7. Good Downstream Power Connection



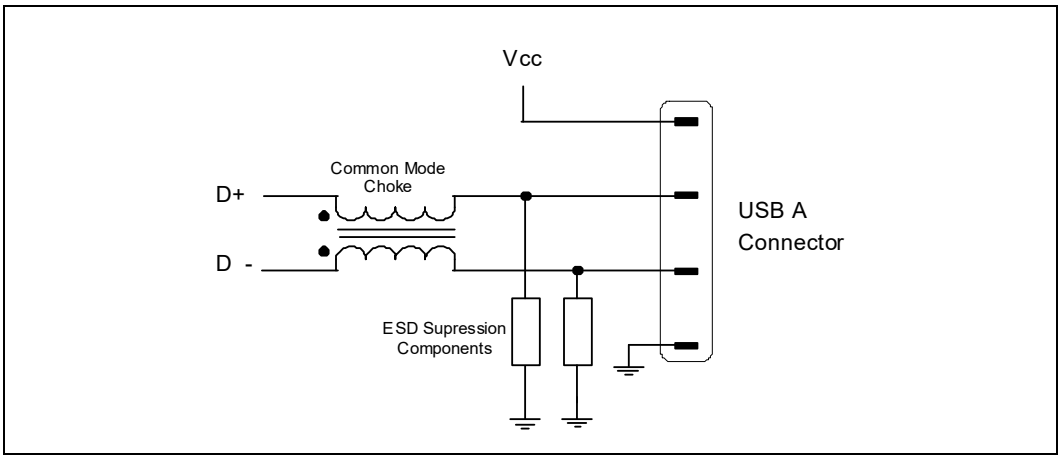
8.4 EMI and ESD Considerations

The following guidelines apply to the selection and placement of the common mode chokes and ESD protection devices.

8.4.1 Common Mode Chokes

Testing has shown that the common mode chokes provide the required noise attenuation. A design includes a common mode choke footprint. This provides a stuffing option if the choke is needed to pass EMI testing. Figure 8-8 shows the schematic of a typical common mode choke and the ESD suppression components. Place the choke close to the USB connector signal pins. In systems that route USB to a front-panel header, the choke is placed on the front-panel card.

Figure 8-8. Common Mode Choke



Common mode chokes distort full- and high-speed signal quality. As the common mode impedance increases, the distortion increases. Test the effects of the common mode choke on full- and high-speed signal quality. The common mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke is a two-step process:

- Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that are suppressed.
- After obtaining a part that gives passing EMI results, test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality. Care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-, full-, and high-speed USB operation.

Note: Further common mode choke information is found on the *High-Speed USB Platform Design Guides* available at www.usb.org/developers/docs.

8.4.2 ESD Protection

USB components and ICs are heavily subjected to frequent human contact due to their hot-plug usage model. There are repeated insertions and removals of the various USB devices from the USB ports. As a result, the USB ports are easily exposed to ESD strikes from the human body that destroy both the USB host and the devices on the platform. ESD discharges from human contact easily go up to ~35 kV in extreme cases. The USB ports need to be protected.

A variety of ESD protection devices are readily available on the market and are: Metal-Oxide Varistors (MOVs), zener diode, Transient Voltage Suppressor (TVS), polymer devices, and dual-rail clamp diodes. A classic USB (1.0/1.1) provides ESD suppression using in-line ferrites and capacitors that form a low-pass filter. This technique does not work for USB 2.0 due to the higher signal frequency. With a 480 Mbps data rate, USB 2.0 is sensitive to parasitic capacitance in its signal path. A small parasitic capacitance (a few pF) distorts the USB signal. This causes the USB signal to fail; devices do not work properly. To meet the stringent requirement on the device capacitive load, the dual-rail clamp diode is recommended. This diode has the lowest capacitance among the ESD protection devices and is the best option for USB 2.0 ESD protection.

Figure 8-9 shows the circuitry of the dual-rail clamp diodes.

Figure 8-10 shows the typical integrated diode array package and Figure 8-11 shows a layout example of the USB with a diode array.

Figure 8-9. ESD Protection Devices

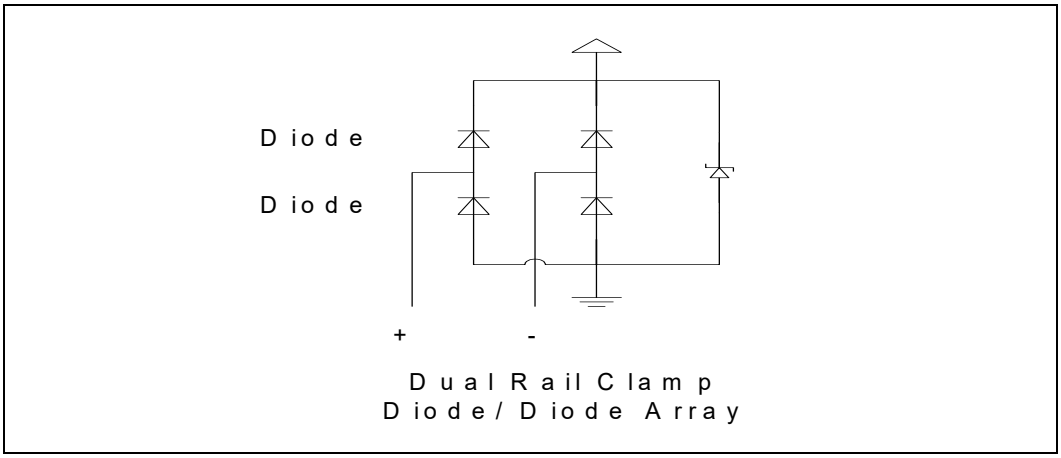
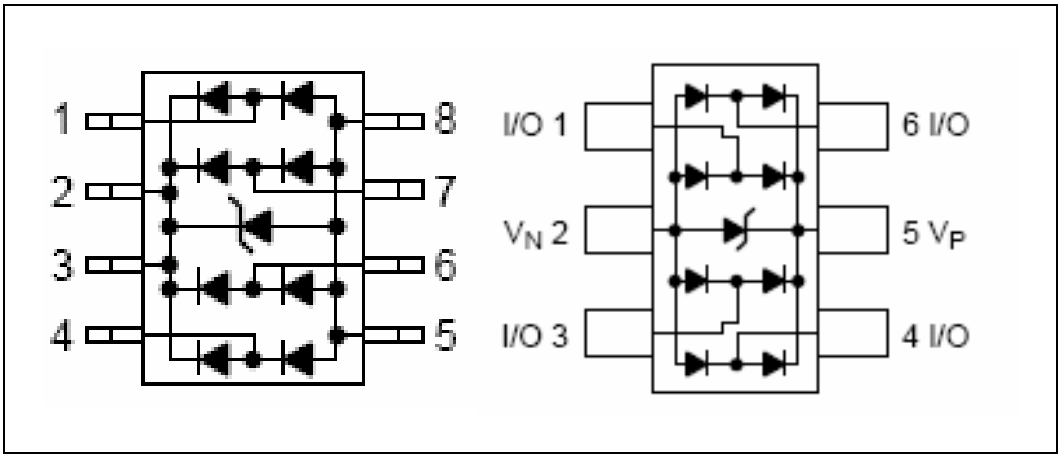
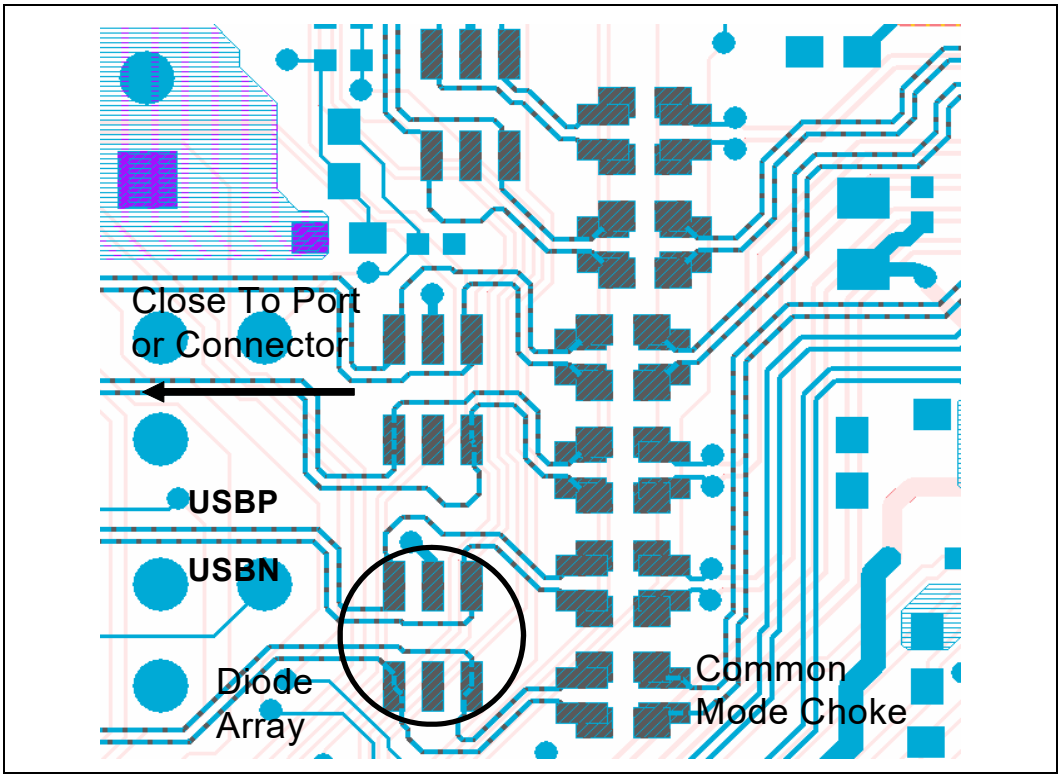


Figure 8-10. Typical Integrated Diode Array Package



The proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 8-8. The ESD protection devices are placed as close to the USB connector as possible. When an ESD strike occurs, the discharges are absorbed or diverted to the ground/power plane instead of coupling to the other signal paths nearby. The proper placement of the ESD protection devices improve the system protection effectiveness against ESD strikes. Other types of low-capacitance ESD protection devices work as well. They, however, have not been investigated.

Figure 8-11. USB with Diode Array Layout Example



Using the ESD protection devices with a higher parasitic capacitance impacts the USB 2.0 signal quality therefore limiting the routing solution space of the USB.

Note: Further ESD information is detailed in the *High-Speed USB Platform Design Guides* available at www.usb.org/developers/docs.

The recommended characteristics of an ideal ESD protection diode for USB 2.0:

- Withstands at least 8 kV of ESD, complying to the IEC 61000-4-2 standard.
- Has low capacitance (< 2 pF) to minimize the signal distortion at a high data rate.
- Has fast response time to ESD events.
- Has low-leakage current to minimize the static power consumption.
- Integrates and reduces the package dimension for better real estate and smaller parasitic package effects.
- Has a high reliability to absorb the repetitive ESD conditions without damage.

8.4.3 ESD Protection Diode Vendors

ESD suppression is always recommended by Intel. Intel does not recommend a specific part/device or circuit for ESD suppression because each solution is board/chassis/usage model specific. The following vendors manufacture an ESD protection diode for USB 2.0 that conforms to the IEC 61000-4-2 standard. Contact the ESD protection device vendors for more specific details on device availability, packaging option, data sheet, and board layout optimization for ESD.

ON Semiconductor*:	http://www.onsemi.com
NXP*:	http://www.nxp.com
ProTek Devices*:	http://www.protekdevices.com
Semtech Corporation*:	http://www.semtech.com
STMicroelectronics*:	http://www.st.com

Note: This is not an extensive list. There are others. Check with the preferred ESD solution vendor to determine if a compatible device is available.

8.5 USB2_COMP Connection

Intel recommends designers short the USB2_COMP pin at the package and then route it on the top layer to one end of a 113 Ω ± 1% resistor to ground. If routing on the top layer is not possible, then it is acceptable to route through a via close to the shorted package pins to the bottom layer. Place the resistor within 500 mils of the SoC. Avoid routing next to the clock pins.

Figure 8-12. USB2_COMP Connection

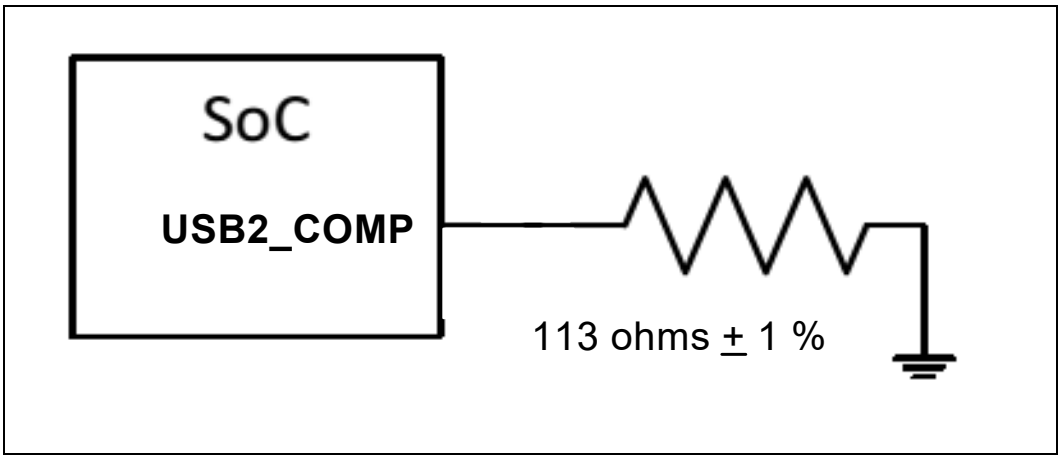


Table 8-7. USB2_COMP Routing Guidelines

Signal name	Impedance	Layer	Length	Length matching within differential pair	Figure
USB2_COMP	50 Ω ± 15%	Microstrip or Stripline	0 - 0.5”	N/A	Figure 8-12

Table 8-8. Resistor

Signal Name	Resistor	Figure	Notes
USB2_COMP	Rpd = 113 Ω ± 1%	Figure 8-12	

8.6 Terminating Unused USB Interfaces

If a USB port is not implemented on the platform:

- The USB2_D{NP}[3:0] signals are left unconnected.
- The USB_OC_N requires a pull-up to P3V3 with 8.2 kΩ - 10 kΩ resistors.
- USB2_COMP must be terminated as specified for normal use.

8.7 USB 3.0 Design Guidelines

Table 8-9. Reference Documents

Title	Doc #/Location
Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4	558579
USB 3.0 Radio Frequency Interference Impact on 2.4 GHz Wireless Devices White Paper*	http://www.intel.com/content/www/us/en/io/universal-serial-bus/usb3-frequency-interference-paper.html?wapkw=interference http://www.usb.org/developers/docs/whitepapers/
USB 3.0 Internal Connector and Cable Specification	http://www.intel.com/content/www/us/en/io/universal-serial-bus/usb3-internal-connector-cable-specification.html

Table 8-10. Compliance Documents

Title	Doc #/Location
USB 3.0 Specification	www.usb.org
Universal Serial Bus 3.0 Connectors and Cable Assemblies Compliance Document	www.usb.org/developers/docs/devclass_docs/CabConn_3_0_Compliance_Document_v1.02_2011-10-04.pdf

All general routing guidelines for USB 2.0 also apply to USB 3.0.

Figure 8-13 and Table 8-11 give general guidelines for USB 3.0 routing.

Figure 8-14 gives an example of recommended back panel topology.

Figure 8-15 and Figure 8-16 give examples of front panel topologies.

It is recommended to use minimum number of vias and use routing layer on motherboard that has the shortest via stub. The via stub is configuration dependent. The common mode choke and ESD diode is recommended to be placed on the bottom layer to reduce the impact of possible via stubs under the USB connector. If the common mode choke and ESD diode have to be placed on the top layer, then a 1” channel length reduction is required.

AC caps must have a separation that is less than 250 mils from the transition via. AC caps can be placed within 0.5” from the SoC, or within 0.6” from the USB connector on the bottom layer.

Figure 8-13. USB 3.0 Trace Geometries

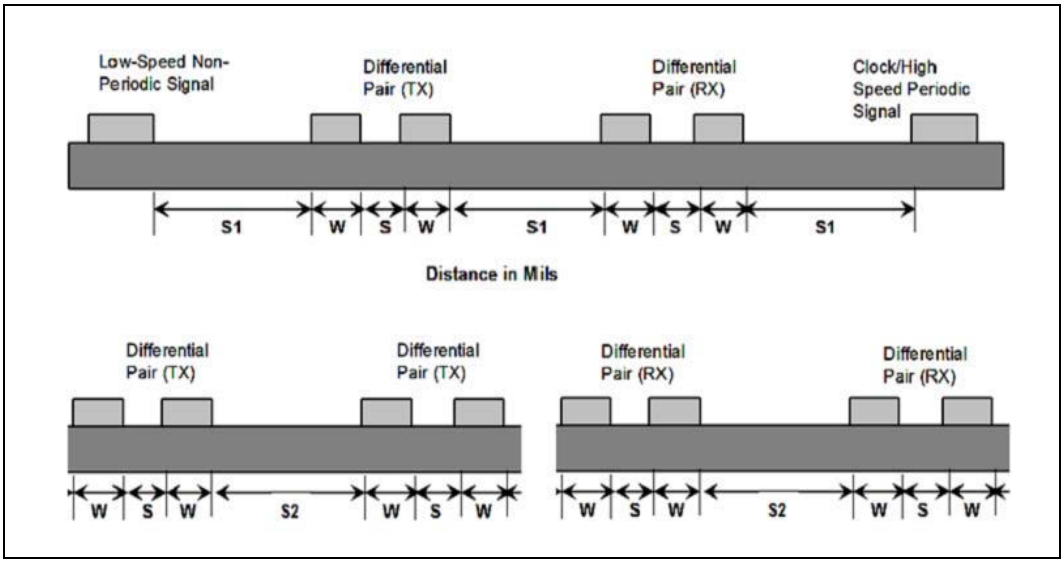


Table 8-11. USB 3.0 Topology Guidelines (w/Common Mode Choke and ESD Protection Diode)

Topology	Routing requirement / trace impedance	Breakout	Maximum motherboard trace length (inches)	Maximum internal cable length (inches)	Maximum daughter card trace length (inches)
Back Panel (standard loss)	IL max= -0.79 dB/inch @4 GHz Z = 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) [Sync with the stackup used.] S1 ≥ 7h for stripline; 11h for microstrip S2 ≥ 5h for stripline; 9h for microstrip W, S (note 2)	W = 3.5mils S = 4mils S1 = Different layers or 9h S2 ≥ 2h L ≤ 500mils	10"	NA	NA
Back Panel (low loss)	IL max = -0.48 dB/inch @4 GHz Z = 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) [Sync with the stackup used.] S1 ≥ 7h for stripline; 11h for microstrip S2 ≥ 5h for stripline; 9h for microstrip W, S (note 2)	W = 3.5mils S = 4mils S1 = Different layers or 9h S2 ≥ 2h L≤ 500mils	14"	NA	NA
Front Panel Cable Up	IL max = -0.79 dB/inch @4 GHz Z = 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) [Sync with the stackup used.] S1 ≥ 7h for stripline; 11h for microstrip S2 ≥ 5h for stripline; 9h for microstrip W, S (note 2)	W = 3.5mils S = 4mils S1 = Different layers or 9h S2 ≥ 2h L ≤ 500mils	5"	20"	NA
Front Panel Daughter Card	IL max = -0.79 dB/inch @4 GHz Z = 85 Ω ± 10% (stripline) or 85 Ω ± 15% (microstrip) [Sync with the stackup used.] S1 ≥ 7h for stripline; 11h for microstrip S2 ≥ 5h for stripline; 9h for microstrip W, S (note 2)	W = 3.5mils S = 4mils S1 = Different layers or 9h S2 ≥ 2h L ≤ 500mils	5"	10"	1"

Notes:

1. W refers to trace width. S refers to intra-pair spacing. S1 refers to spacing between USB 3.0 Rx pairs and any other signals or USB 3.0 Tx pairs to any other signals or USB 3.0 Rx pairs to Tx pairs. S2 refer to spacing between USB 3.0 Rx to Rx pairs or Tx to Tx pairs.
2. The actual trace width (W) and spacing (S) depends on Insertion loss (IL), impedance (Z) and stackups options described in this document.
3. Signals are ground referenced.
4. The maximum mismatch within data pairs should not be greater than 5 mils (this includes total channel length matching and per-layer/layer-wise length matching).
5. For front panel solutions, signal matching is considered from the Wellsburg PCH to the front panel header.
6. If the main routing is stripline, no more than three vias are allowed on the signal path including via under the USB connector. If the main routing is microstrip, no more than two vias.
7. All lengths are based upon using a Common Mode Choke (CMC) and ESD diode.
8. For breakout, keep S2 as big as possible and the breakout length as short as possible.

8.7.1 USB 3.0 Back Panel Topology

This topology is defined to be USB 3.0 signals routed directly to an A-connector. Non-interleaved break-out is required to mitigate concerns on near-end crosstalk. The main route supports interleaved routing and non-interleaved routing for maximum flexibility. However, Breakout (L1) must be routed using a non-interleaved scheme. TX and RX should either be on different board layers or have 9h mils minimum pair-to-pair spacing between them at breakout. TX-to-TX and RX-to-RX pair-to-pair spacing at Break-out only requires 2*h* mils minimum. It is recommended to use common mode chokes (CMC) and electrical static discharge (ESD) diode components at the expense of routing length. The combined effects of CMC and ESD should have insertion loss less than -1.7 dB at 2.5 GHz, -3.5 dB at 5 GHz and -6 dB at 7.5 GHz. For further guidance on CMC and ESD component selection, refer to Section 8.9, "USB 3.0 EMC Component Selection Guidelines for more details. These guidelines were developed assuming the USB 3.0 Device implements Tx de-emphasis and adaptive Rx CTLE equalization.

Figure 8-14. USB 3.0 Back Panel Topology

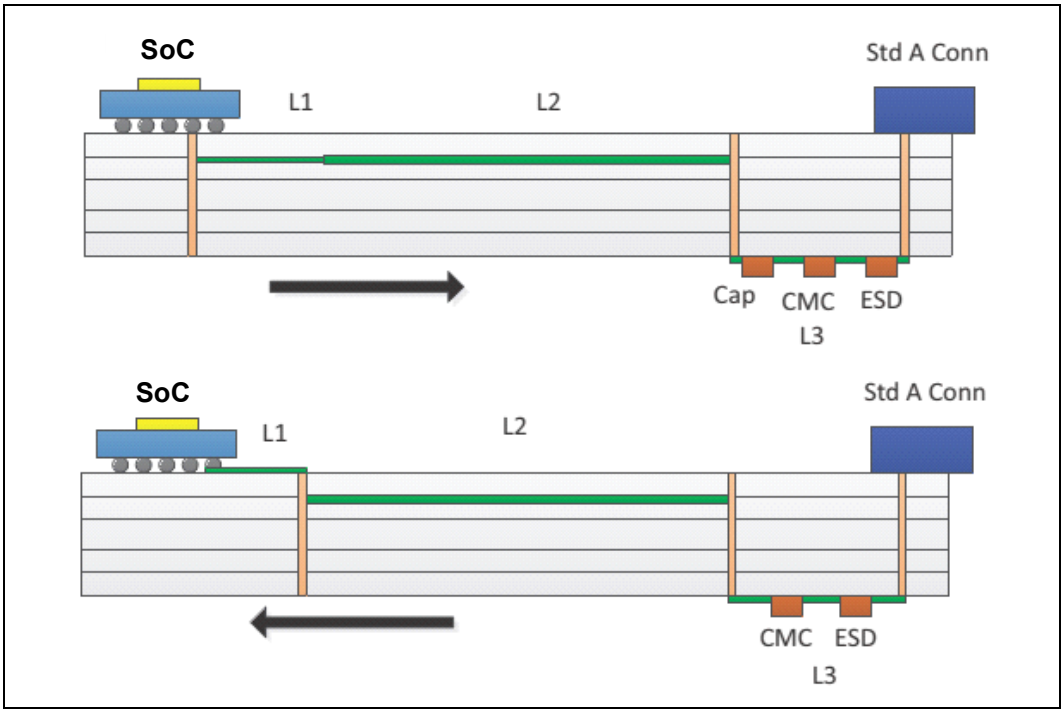


Table 8-12. USB 3.0 Back Panel Routing Guidelines

Description	L1	L2 (note 4)	L3 (notes 1,3)
Maximum length	0.5"	10"-L1-L3 (Std. loss) 14"-L1-L3 (Low loss)	0.6"
Minimum length	0"	3"-L1-L3 (Std. loss) 5"-L1-L3 (Low loss)	0"
Allowed layers	all	all	bottom

Notes:
1. The placement of the CMC and ESD components is flexible within the 0.6" allowed.
2. If the main routing is stripline, no more than three vias are allowed on the signal path including via under USB connector. If the main routing is microstrip, no more than two vias.
3. CMC, ESD and L3 routing are recommended to be placed at Bottom Layer for optimal performance. If they are placed at top layer, 1" reduction on max routing length is required.
4. Refer to table Table 8-11, "USB 3.0 Topology Guidelines (w/Common Mode Choke and ESD Protection Diode)" for insertion loss targets.

8.7.2 USB 3.0 Front Panel Topology

This topology supports an internal connector, internal cable solution and a daughter card. AC cap, CMC, and ESD placements are recommended to be on the daughter card for better signal integrity performance.

Non-interleaved break-out is required to mitigate concerns on near-end crosstalk. However the Main route supports interleaved routing and non-interleaved routing for maximum flexibility. Breakout must be routed using a non-interleaved scheme. TX and RX should either be on different board layers or have 9*h* mils minimum pair-to-pair spacing between TX and RX at Breakout. TX-to-TX and RX-to-RX pair-to-pair spacing at Break-out only requires 2*h* mils minimum.

Figure 8-15. USB 3.0 Front Panel Cable-Up Topology

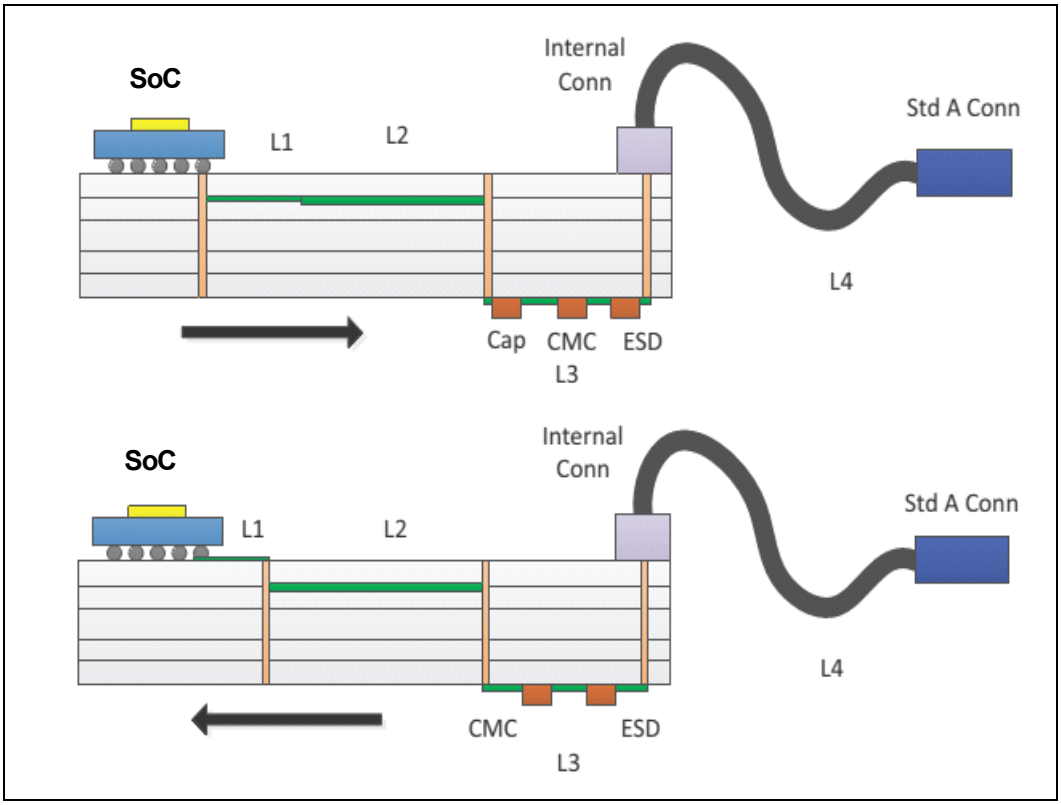


Table 8-13. USB 3.0 Front Panel Cable-Up Routing Guidelines

Description	L1	L2 (note 4)	L3 (notes 1,3)	L4
Maximum length	0.5”	5"- (L1+L3)	0.6”	20”
Minimum length	0”	3"- (L1+L3)	0”	10”
Allowed layers	all	all	bottom	NA

Notes:
1. The placement of the CMC and ESD components is flexible within the 0.6” allowed.
2. If the main routing is stripline, no more than three vias are allowed on the signal path including via under USB connector. If the main routing is microstrip, no more than two vias.
3. CMC, ESD and L3 routing are recommended to be placed at Bottom Layer for optimal performance. If they are placed at top layer, 1" reduction on max routing length is required.
4. Low loss dielectric materials are not recommended for short channels. Reflections may not be properly dampened.

Figure 8-16. USB 3.0 Front Panel - Daughter Card Topology

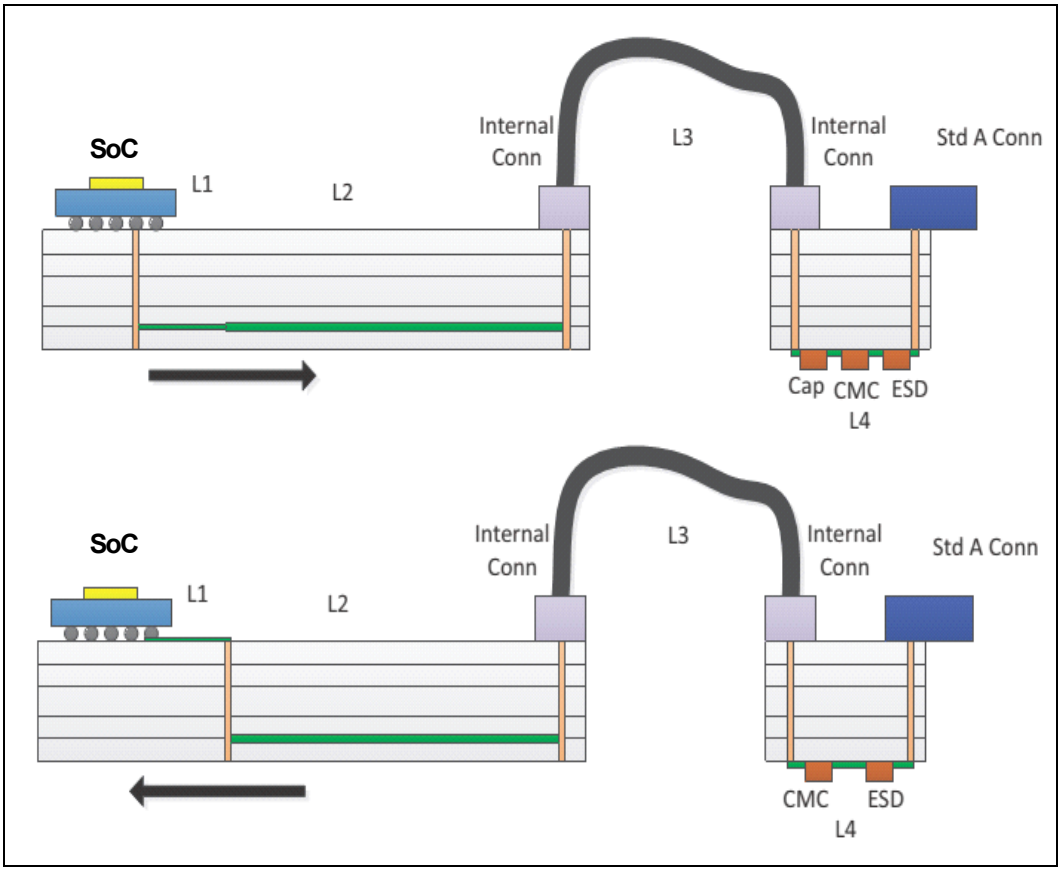


Table 8-14. USB 3.0 Front Panel - Daughter Card Routing Guidelines

Description	L1	L2	L3	L4
Maximum length	0.5”	5"- (L1+L4)	10”	1”
Minimum length	0”	3"- (L1+L4)	5”	0”
Layers	Via stub < 10 mils	Via stub < 10 mils	bottom	bottom

Notes:
1. The placement of the CMC and ESD components is flexible within the 1” allowed.
2. CMC, ESD and L4 routing are recommended to be placed at Bottom Layer for optimal performance.
3. Low loss dielectric materials are not recommended for short channels. Reflections may not be properly dampened.

8.7.3 Stub Guidelines

Avoid stubs on USB Super Speed signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 100 mils. For front panel with a daughter card configuration the total via stub should not be greater than 20 mils.

8.7.4 USB 3.0 Non-Interleaved Breakout Guidelines

Simulation results show that SoC Receiving margin is severely degraded by near-end crosstalk (NEXT) from adjacent Transmit signals. Thus, non-interleaved breakout is required to mitigate concerns on near-end crosstalk. The SoC chipset package ballmap has USB 3.0 TX signals on inner balls and USB 3.0 RX signals on outer balls to help facilitate non-interleaved breakout.

Recommended implementation is to break-out USB 3.0 TX and USB 3.0 RX signals on different board layers as shown in Figure 8-18. If this is not possible, care must be taken to maintain at least 9h pair to pair spacing between TX and RX signals at breakout region. Pair-to-pair spacing for TX-to-TX and RX-to-RX is less stringent and requires 2h at breakout.

Figure 8-17. Non-Interleaved vs. Interleaved Routing

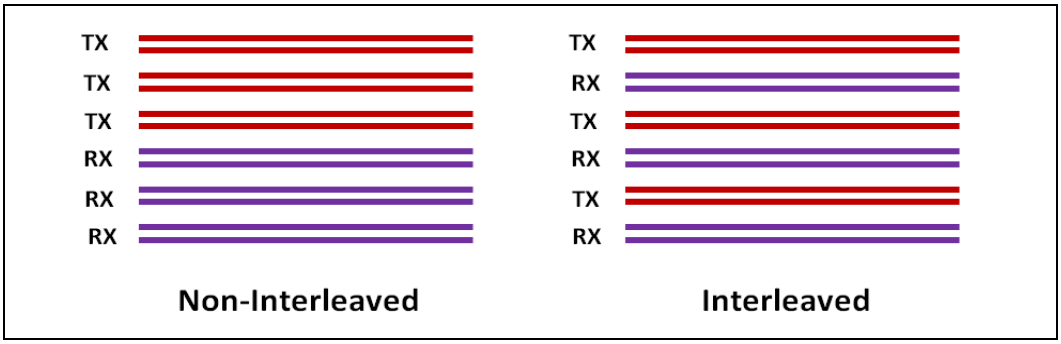
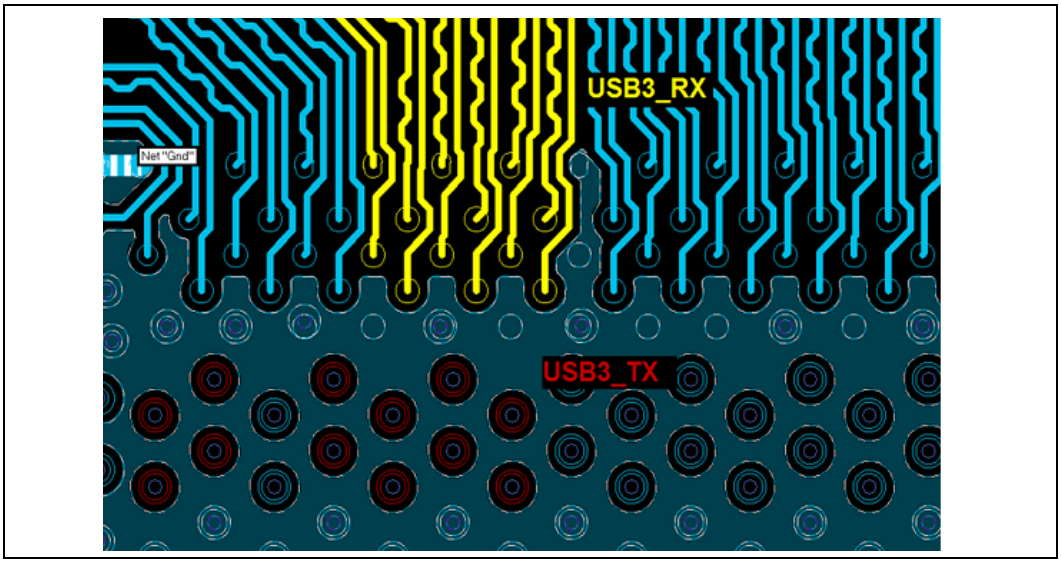


Figure 8-18. Example of Non-Interleaved Breakout using Different Layers



8.7.5 Length Matching and Length Formulas

Each net within a differential pair should be length matched. Matching of TX to RX within the same port and between USB TX and RX pairs from different ports is not required. When length matching compensation occurs, it should be made as close as possible to the point where the variation occurs. The maximum mismatch within differential pairs should not be greater than 5 mils over entire routing length. Per layer length matching within differential pairs should be within 5 mils also.

Please refer to Chapter 2, "Platform Stack-up and General Design Considerations" for length matching guidelines.

8.8 USB 3.0 Optimization Guidelines

8.8.1 USB Connector/Receptacle Recommendations

Proper connector choice is critical to ensure adequate USB signal quality. Empirical data has shown that triple-stack and quad-stack USB stack connectors may add interference causing poor USB signal quality.

Please refer to usb.org for a list of tested connectors and receptacles.

Proper selection of a motherboard mating connector with USB 3.0 support is important to ensure signal quality is not adversely affected due to a poor connector design. USB 3.0 may utilize either a Standard A or Dual-A Connector.

Triple-stack and Quad-stack Connectors are not recommended due to potential Signal quality degradation on the top most ports. The back panel connector must meet the requirements listed in the *USB 3.0 Specification*. USB 3.0 and USB 2.0 A-receptacle connectors are not footprint compatible. In addition, it is also recommended to use a color scheme to distinguish between USB 2.0 and USB 3.0 connectors. See Section 5.3.1.3 of the *USB 3.0 Specification* for more details.

8.8.1.1 USB 3.0 Standard A Connector Recommendations

USB 3.0 may utilize either a Standard A or Dual-A Connector. Quad-stack Connector is not recommended due to potential Signal quality degradation on the top most ports. Signals shall be launched into the connector from the bottom of the board to minimize the through-hole stub effect. The connector footprint shall have the following through-hole dimensions: 28 mil finished hole, 43 mil pad, and 58 mil anti-pad.

8.8.1.2 USB 3.0 Triple Stacked Connector Selection Considerations

USB 3.0 specification rev1.0 Section 5.3 only defines single and double stacked connectors. Using non-spec compliant connectors such triple stacked connector may impact signal quality, especially for the third port on the top due to crosstalk and insertion loss. Since no spec is defined for triple stacked connector, customers should perform their own signal integrity simulation using the connector modules provided by vendors.

The routing guideline in Table 8-11, "USB 3.0 Topology Guidelines (w/Common Mode Choke and ESD Protection Diode)" for triple stacked connector is only as Intel recommendation based on simulation, but won't be validated.

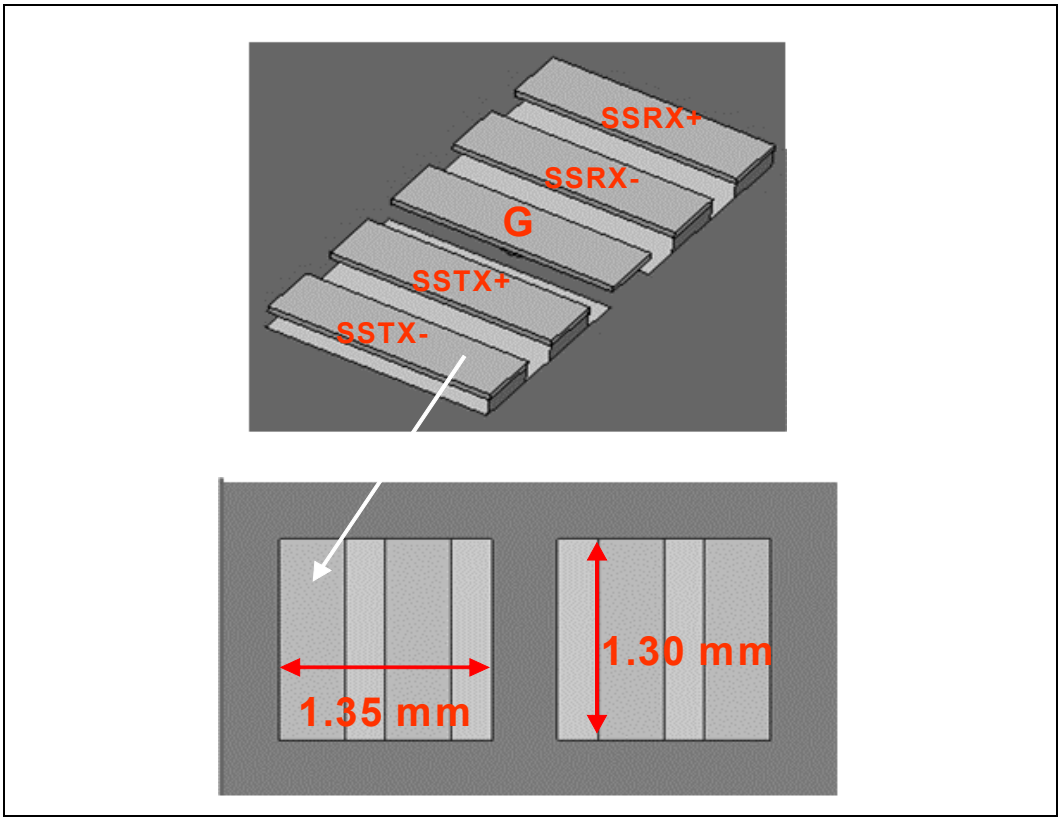
8.8.1.3 USB 3.0 Standard B and Power B Connector Recommendations

USB 3.0 may utilize either a Standard B or Power B Connector. Signals shall be launched into the connector from the bottom of the board to minimize the through-hole stub effect. The connector footprint shall have the following through-hole dimensions: 28 mil finished hole, 43 mil pad, and 58 mil anti-pad.

8.8.1.4 USB 3.0 Micro B Connector Recommendation

USB 3.0 may utilize either a Micro B Connector. For USB 3.0 Micro B connector SMT application, signals shall be launched into the connector from the top of the board. The Vcc/GND reference plane shall have the following ground void to reduce capacitance from solder to reference plane.

Figure 8-19. USB 3.0 Micro B SMT Connector Footprint Recommendation

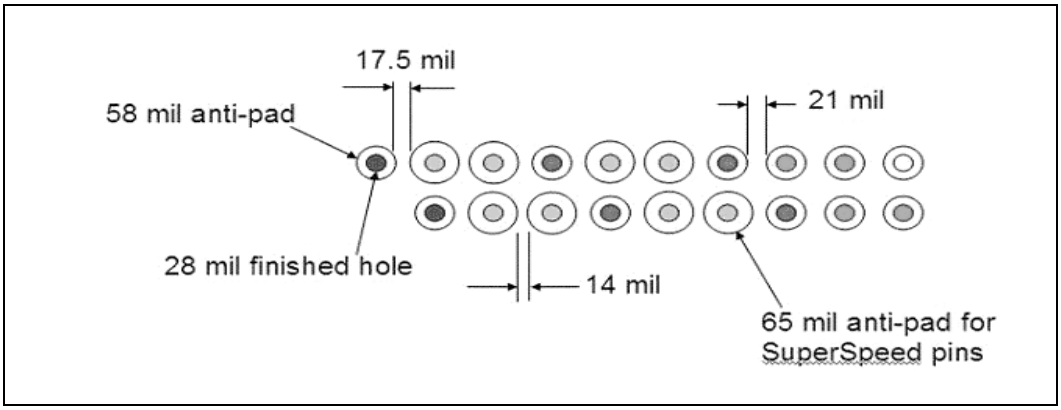


8.8.1.5 USB 3.0 Internal Connector

For platforms that implement a USB 3.0 front panel topology, a USB 3.0 internal connector may be required. This connector allows system designers to connect USB 3.0 from the motherboard to the front panel of the platform.

Signals shall be launched into the connector from the bottom of the board to minimized the through-hole stub effect. For super speed pins the connector footprint shall have the following through-hole dimensions: 31 mil finished hole, 41 mil pad, and 65mil anti-pad. For other pins the connector footprint shall have 28 mil finished hole, 43 mil pad, and 58 mil anti-pad.

Figure 8-20. USB 3.0 Internal Connector Footprint Recommendation



The USB 3.0 internal cable connector A, or USB 3.0 ICC A, is mounted on the motherboard, while the USB 3.0 internal cable connector B, or USB 3.0 ICC B on the daughter card. This document will focus only on the motherboard connector.

Note: This document assumes that the USB 3.0 internal connector supports up to 2 USB 3.0/ USB 2.0 ports.

Table 8-15. USB 3.0 Internal Connector Pinout (Motherboard)

Pin Number	Connector Signal	Description
1	VBus	Power
2	IntA_P1_SSRX-	USB 3.0 Port 1 SuperSpeed RX-
3	IntA_P1_SSRX+	USB 3.0 Port 1 SuperSpeed RX+
4	GND	GND
5	IntA_P1_SSTX-	USB 3.0 Port 1 SuperSpeed TX-
6	IntA_P1_SSTX+	USB 3.0 Port 1 SuperSpeed TX+
7	GND	GND
8	IntA_P1_D-	USB 3.0 Port 1 D- (USB 2.0 Signal D-)
9	IntA_P1_D+	USB 3.0 Port 1 D+ (USB 2.0 Signal D+)
10	ID	Over Current Protection
11	IntA_P2_D+	USB 3.0 Port 2 D+ (USB 2.0 Signal D+)
12	IntA_P2_D-	USB 3.0 Port 2 D- (USB 2.0 Signal D-)
13	GND	GND
14	IntA_P2_SSTX+	USB 3.0 Port 2 SuperSpeed TX+
15	IntA_P2_SSTX-	USB 3.0 Port 2 SuperSpeed TX-
16	GND	GND
17	IntA_P2_SSRX+	USB 3.0 Port 2 SuperSpeed RX+
18	IntA_P2_SSRX-	USB 3.0 Port 2 SuperSpeed RX-
19	VBus	Power

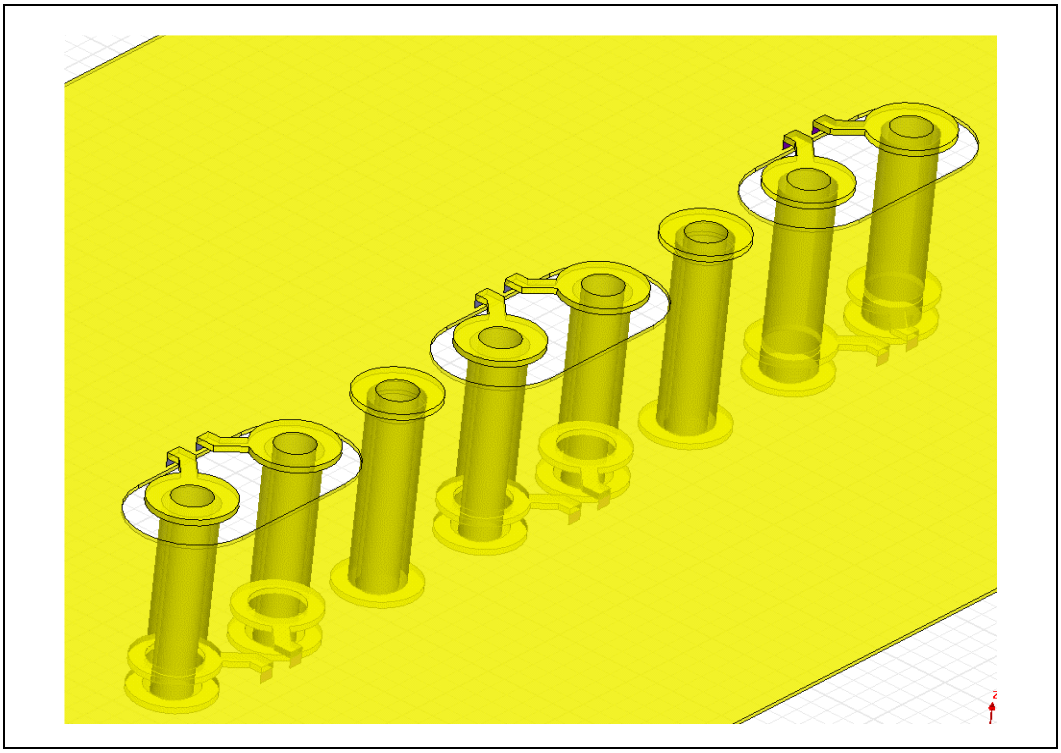
8.8.2 Differential Via Routing

USB 3.0 differential vias should follow the recommendation below. Oval shaped anti-pad features are created by taking out the plane from quadrant to quadrant of the 30 mil circular anti-pad. Trace should have a 45 degree entry to the pin pair symmetrically.

Table 8-16. USB 3.0 Differential Via (Not used in the Breakout Region)

Via Pad	20 mils
Via Diameter	10 mils
Anti-pad	30 mils
Via pitch	35 mils

Figure 8-21. USB 3.0 Differential Via Routing Recommendation



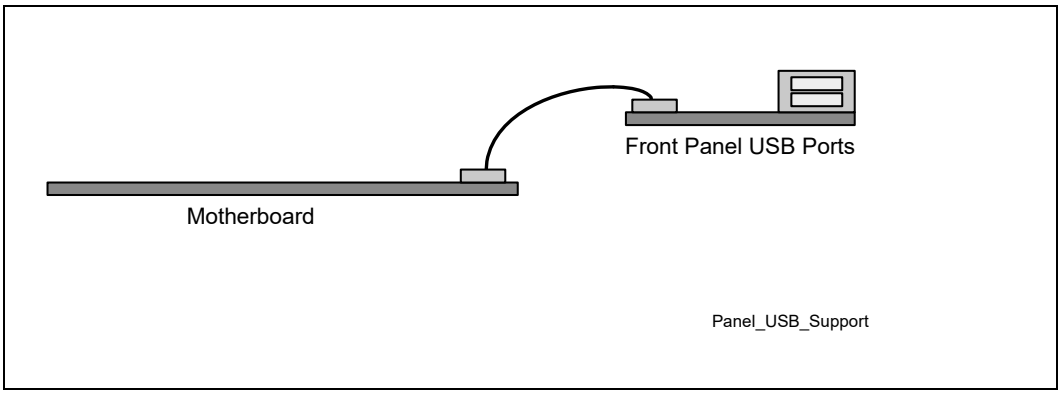
8.8.3 Front Panel Connector Design without a Daughter Card

There are "off the shelf" cables available from third party vendors that can connect to the mother board 2x10 USB header and then mount directly to the front panel chassis Internal/Front Panel using a Daughter Card.

One method to provide front or side panel support for USB 3.0 is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective.

Figure 8-22 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 8-22. Motherboard Front Panel USB Support



When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a daughter card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

8.8.3.1 Front Panel Daughter Card Design Guidelines

- Place the VBUS bypass capacitance on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 1-inch trace length is recommended.
- Use the same mating connector pinout as - USB 3.0 Internal Connector Pinout (Motherboard).
- Use the same routing guidelines as described in USB 3.0 Stackup Guidelines.

8.8.4 Internal USB Cables

The front panel internal cable solution must meet all the requirements of Chapter 5 of the *USB 3.0 Specification* for SuperSpeed cabling and the *USB 3.0 Internal Connector and Cable Specification*.

8.9 USB 3.0 EMC Component Selection Guidelines

8.9.1 USB 3.0 Common Mode Choke (CMC)

External IOs with cables such as USB interfaces need EMC treatment. USB 3.0 lanes can also produce a substantial level of common-mode (CM) noise thereby resulting in cable radiation violating the allowable limits for regulatory requirements and wireless radio frequency interference levels. The CM noise on USB 3.0 lanes can be accumulated many ways: a non-homogeneous PCB channel, unbalanced Vss-signal via placement, unbalanced package/connector Vss-signal pin maps, and an external cable. In addition, USB 3.0 Super-Speed data rate being 10 times higher than that of USB 2.0 High-Speed mode (480 Mbps) necessitates a much tighter control of the USB 3.0 CM noise than that of USB 2.0.

Intel recommends implementing a common-mode choke (CMC) footprint for each USB 3.0 TX and RX pairs. However, it should be noted that a CMC for USB 2.0 would not work for USB 3.0 because of its excessive insertion loss and return loss in the USB 3.0 operational frequency band. In fact, major EMC component suppliers have already developed USB 3.0 CMC whose S-parameter characteristics are optimized for the USB 3.0 operational bandwidth and for a channel impedance of 90 Ω. If designers want to perform EMI testing without the CMCs populated, it is recommended to combine a small form factor, 0402, chip resistor footprint and a CMC footprint to maintain high signal integrity performance at 5Gbps across the channel.

There are two important parameters to be examined for successful component selection. First, is the differential S-parameters (insertion and return losses) and the second is CM S-parameters (common mode rejection).

Figure 8-23 shows an example of a differential S-parameter set measured from various USB 3.0 CMCs. Intel recommends to choose a CMC such that the combined insertion loss (CMC and ESD) is less than -1.7 dB at 2.5 GHz, -3.5 dB at 5 GHz and -6 dB at 7.5 GHz. It is highly recommended to obtain the S-parameters and the SPICE models from the component suppliers and perform signal integrity simulations to verify eye diagram margin before using them.

Figure 8-23. Differential S-Parameters from USB 3.0 Common Mode Chokes

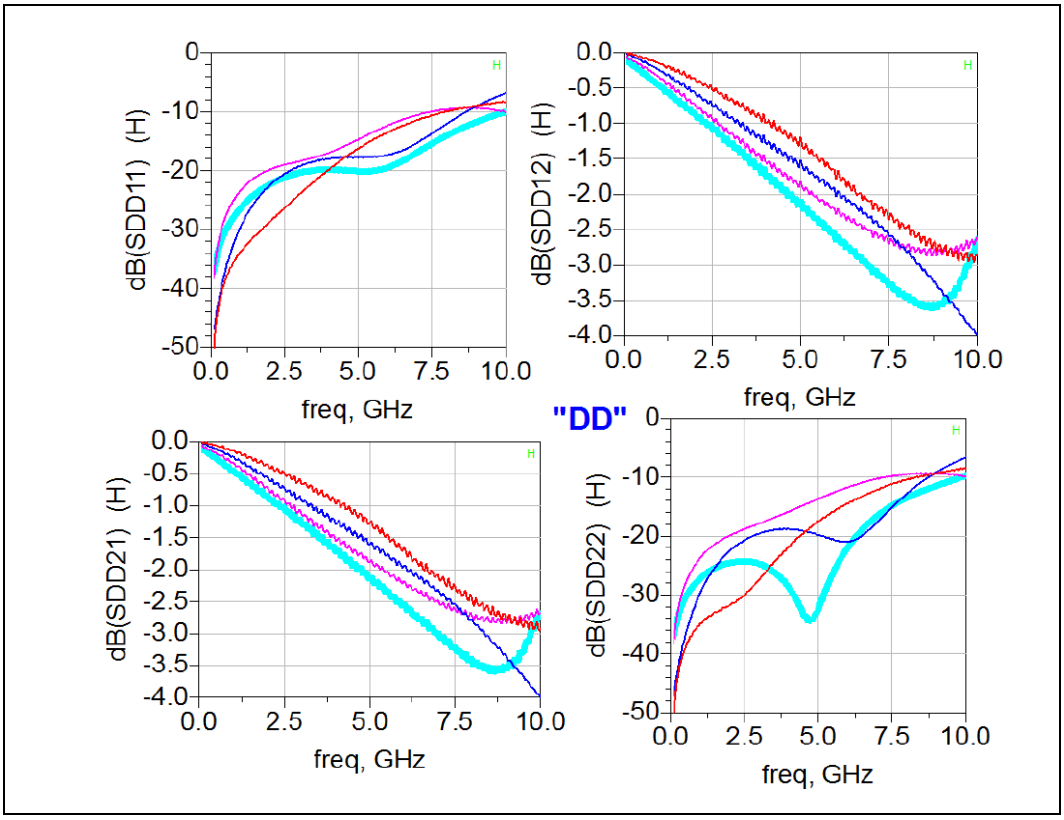
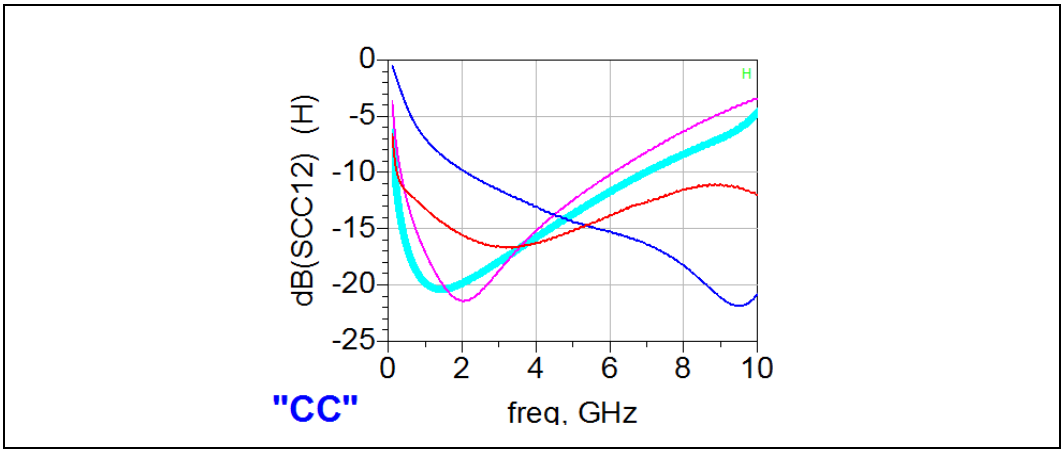


Figure 8-24 shows an ideal CMC component that exhibits a higher CM rejection for a wide frequency band. It is recommended to choose a CMC that can suppress CM lower than -10 dB from 500 MHz to 5 GHz frequency band.

Figure 8-24. Common Mode S-Parameters from USB 3.0 Common Mode Chokes



In summary, the selection of USB 3.0 CMC has to be made after careful consideration of signal integrity margin and CM rejection performance. In addition, it is not recommended to use a USB 2.0 CMC for USB 3.0.

8.9.2 PCB Designs for USB 3.0 EMC Component

As for a thin substrate where the thickness of the dielectric substrate is equal or less than 3 mils, additional insertion loss could be introduced because of the parasitic capacitance between the CMC and ESD device mounting pads and the reference plane underneath the components.

Figure 8-25 shows a PCB design recommendation for USB 3.0 CMC and ESD protection devices whose reference plane is voided with the same size as the surface mounting pad (blue rectangles).

Figure 8-26 illustrates the impacts of voided reference on differential insertion loss and CM rejection for a CMC, respectively. The insertion loss improvement is significant but the degradation of the CM rejection is negligible. Intel recommends this PCB design if inner layer (stripline) routings can be managed such that crossing over voids can be avoided. If the routing density is extremely high and stripline signals cannot avoid crossing over voids, smaller size voiding should be considered (e.g., 50% size of pads) and/or 1-line and 4-line ESD device voiding can be waived.

Figure 8-25. Voided Reference Plane to Improve Signal Integrity

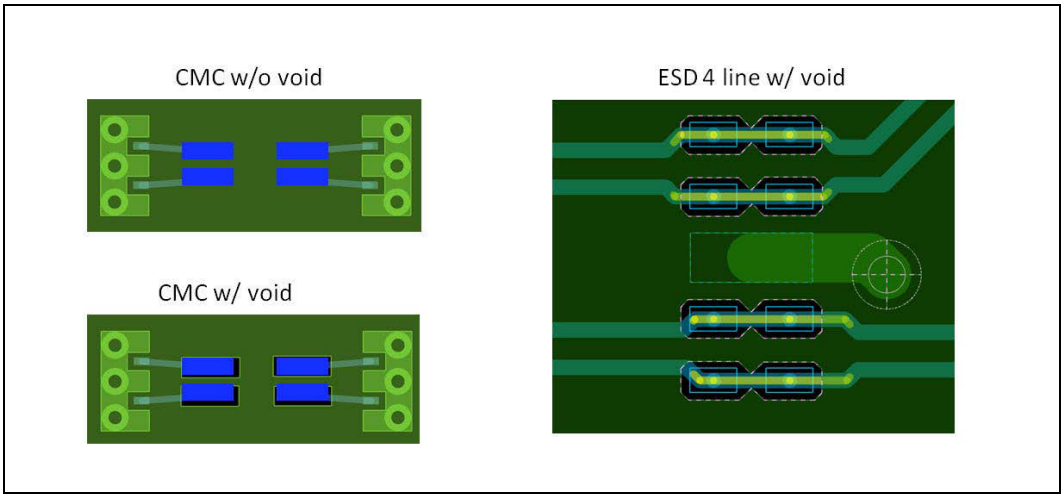
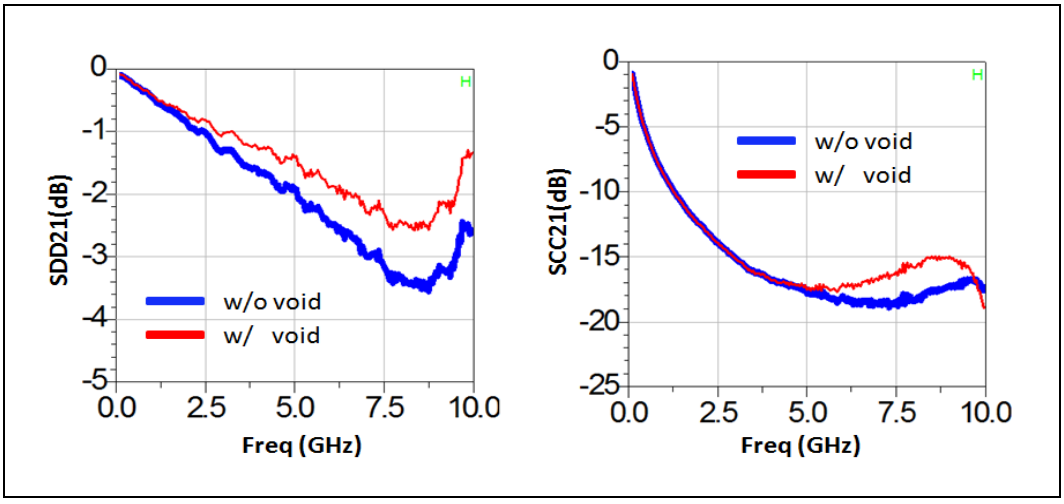


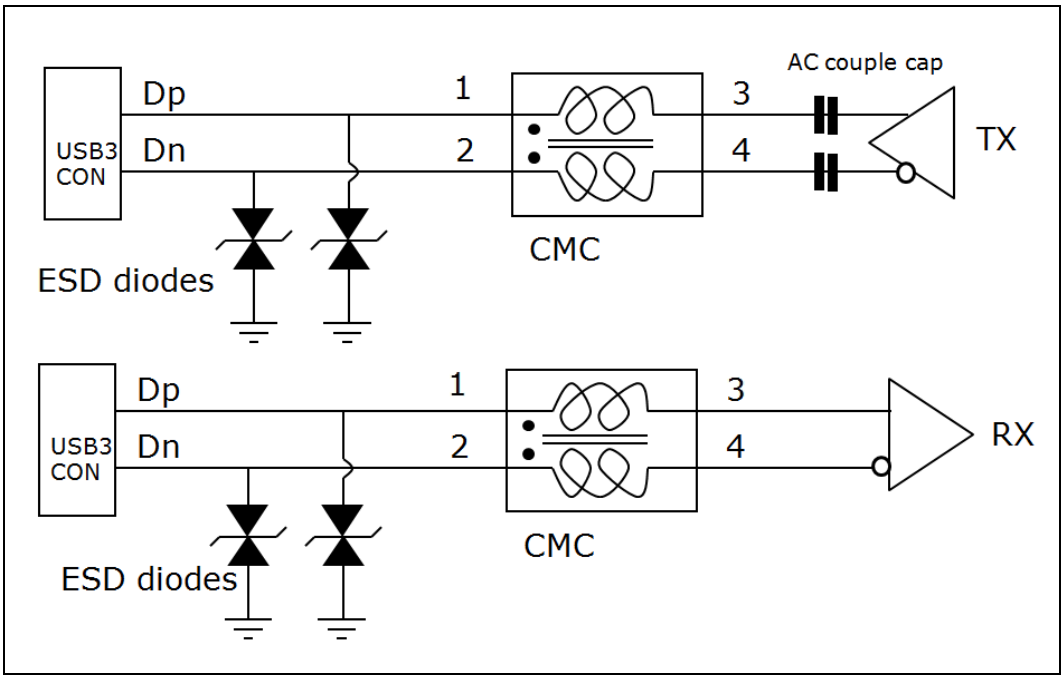
Figure 8-26. Voided Reference Plane Impacts on CMC Signal Integrity and CM Rejection



8.10 USB 3.0 ESD Protection

The USB 3.0 circuit block is vulnerable to ESD strikes because it belongs to I/O that is hot-pluggable thereby exposing the interface to a wide variety of dynamic conditions. Similar to USB 2.0, Intel recommends placing ESD protection devices for each USB 3.0 data pair on both the TX and RX lanes. General USB 3.0 ESD device placement rules are the same as that of USB 2.0 depicted in Figure 8-27. In other words, ESD protection devices are to be placed as close as possible to a connector so that the discharge current returns to chassis and earth ground before reaching the USB 3.0 IC block.

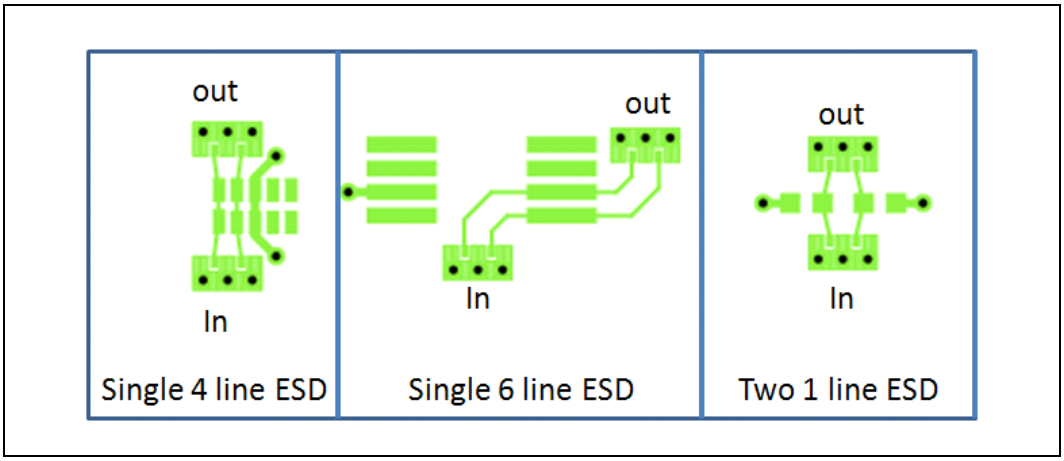
Figure 8-27. USB 3.0 ESD Protection Device Placement for TX and RX Signals



Multiple form-factors have been developed for USB 3.0 ESD protection devices: 1-line, 2-line, 4-line array, and 6-line arrays.

Figure 8-28 shows examples of ESD component placement highlighting the surface pads and break-in line S-parameter test. In addition to form-factor, a component selection can be made from two different manufacturing technologies: Si ESD protection and ceramic/polymer ESD protection devices. Ceramic/polymer based ESD protection devices have much (one order of magnitude) lower parasitic capacitance than Si ESD protection.

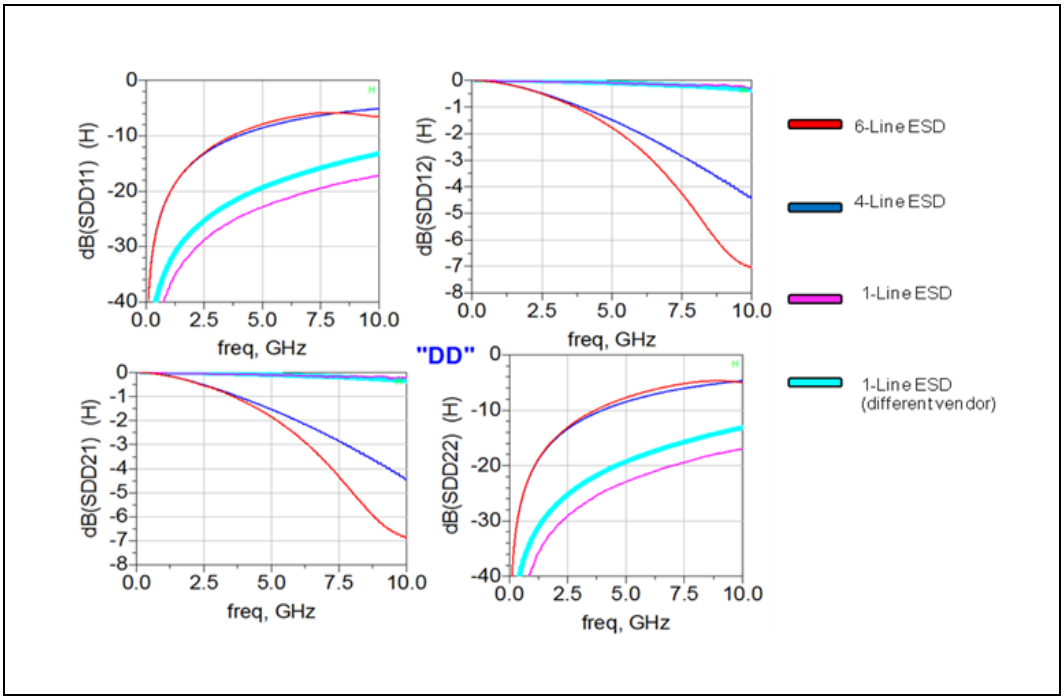
Figure 8-28. USB 3.0 ESD Protection Device Footprints and Routing Examples for S-Parameter Test



Various ESD protection devices have been developed to provide extremely low parasitic capacitance delivering minimal signal integrity impact to USB 3.0 Super Speed. Therefore, USB 2.0 ESD devices cannot be used for USB 3.0. The selection for USB 3.0 ESD protection device involves understanding the differential cross-talk between TX and RX pairs, device clamping voltage and response, and estimating signal integrity degradation from component package and surface pad parasitics. It should be noted that an ESD capacitance value extracted at 100 MHz (excluding package inductance) cannot address its impacts on USB 3.0 signal integrity. Therefore, differential S-parameters or differential time domain reflectometer (TDR) waveforms are the right metric to use.

Figure 8-29 shows an example of differential S-parameters measured from a 1-line ceramic device, a 4-line Si array device, and a 6-line Si array device. Lastly, there is a data set from a different vendor for a ceramic 1-line device but the differences between each other are negligible. Intel has not tested the 1-line Si technology device but it will have a similar S-parameter performance to the 4-line Si array device or slightly worse. As can be seen, the ceramic device has almost no impact on USB 3.0 signaling, however, both the 4-line Si array and 6-line Si array device insertion losses and return losses are significantly higher at 5 GHz and 7.5 GHz. Therefore, extreme care should be taken in selecting ESD protection devices for USB 3.0 signaling especially when signal eye-diagram margin is tight.

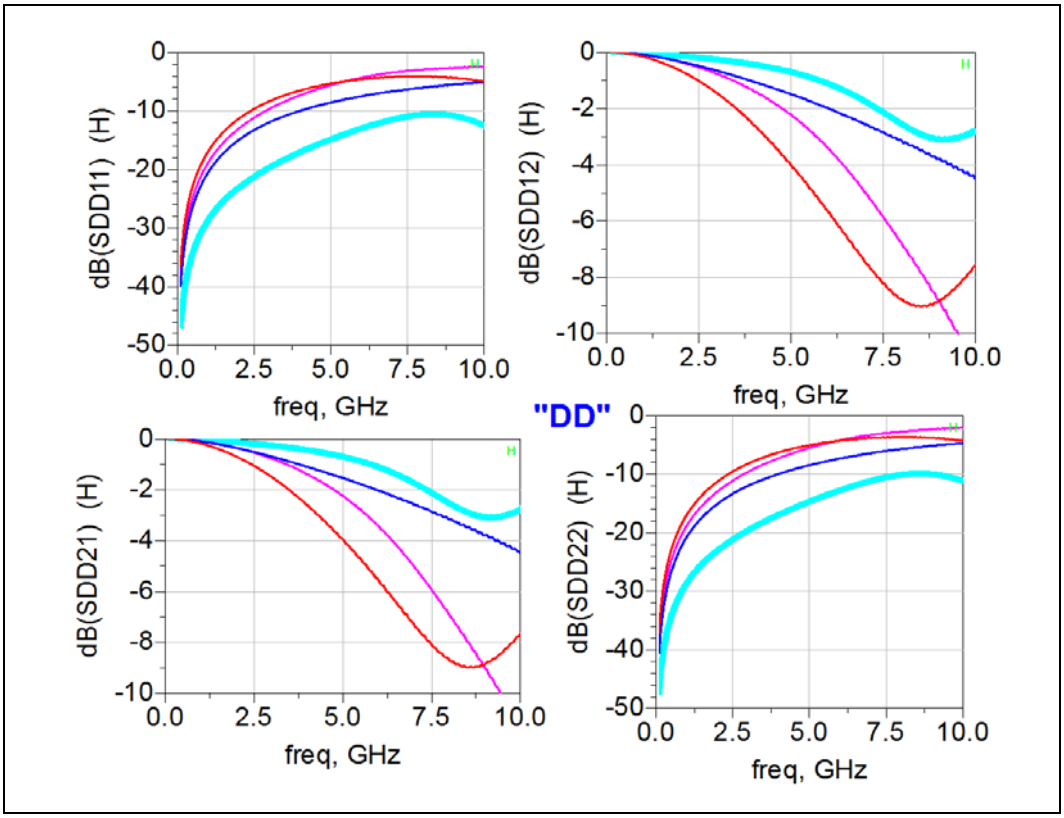
Figure 8-29. Differential S-Parameters from Ceramic 1-Line, Si 4-Line and Si 6-Line ESD Protection Devices



Among various form-factor ESD solutions, the 4-line Si array ESD protection devices are the most popular model because its footprint prevents cross-talk from the adjacent differential lane and allows straight differential transmission routing. However, it should be noted that there are significant S-parameter performance differences although their form factor and footprint are almost the same. This is caused by the differences in the diode physical design and package technology and are hard to capture solely from the vendor supplied parasitic capacitance values.

Figure 8-30 shows measured S-parameters from four different 4-line Si array ESD devices.

Figure 8-30. Differential S-Parameters from 4-Line Si Array ESD Devices

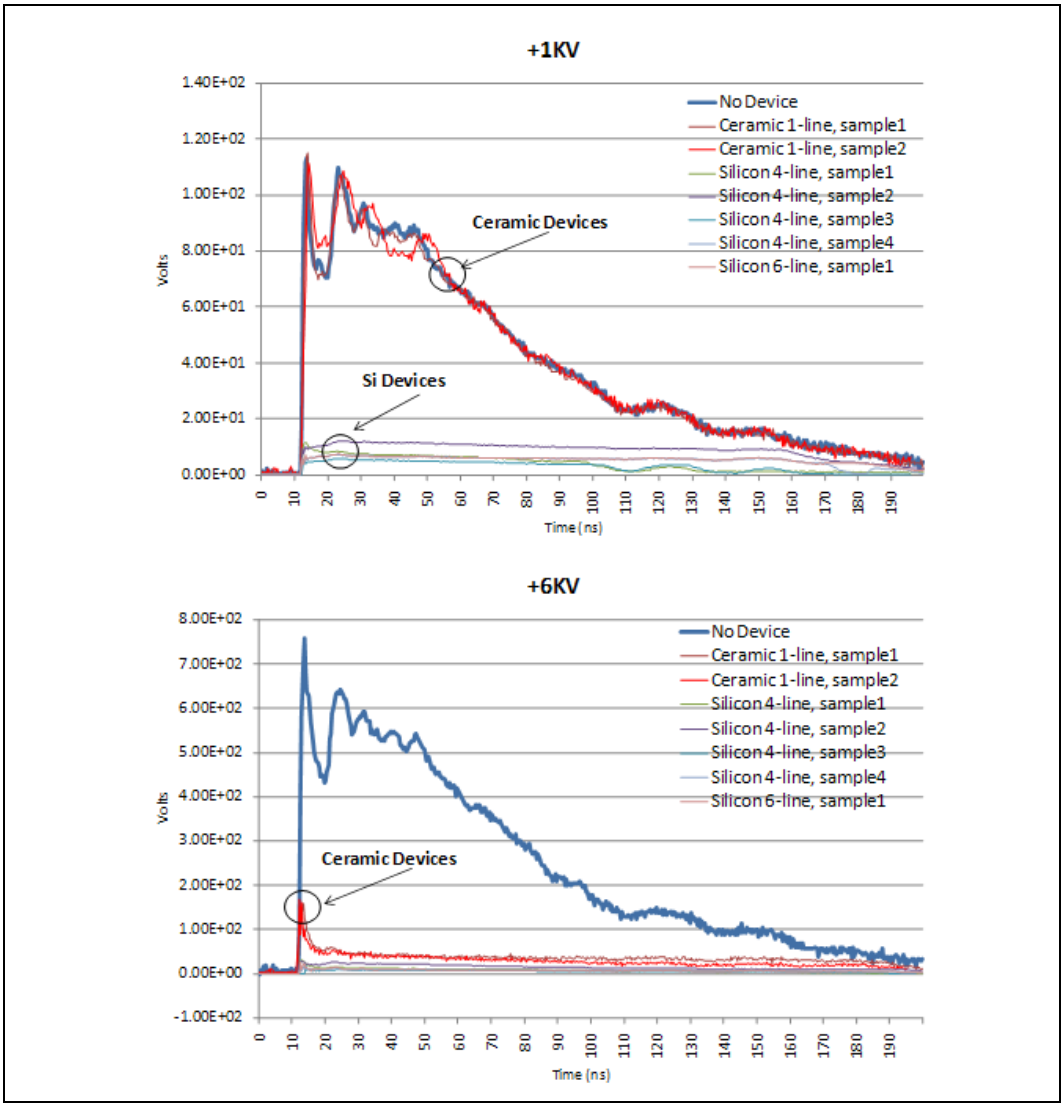


Intel recommends using Si technology ESD protection devices over ceramic/polymer ESD protection devices for USB 3.0 IC protection.

Figure 8-31 shows the peak voltages measured from the output of ESD protection devices when +1 kV and +6 kV contact discharges are injected on the input of the ESD devices. The suppression response from the negative discharges is not much different from the positive discharges although they are not shown here. The blue line represents no ESD protection output. As can be seen, most Si ESD devices suppress the voltage substantially but the ceramic/polymer ESD protection devices are still passing significant levels of voltage.

In summary, the selection of ESD protection device could be made as a trade-off between required ESD performance and signal integrity margin. It is recommended to use Si ESD protection devices and designers should watch out their wide variations of S-parameter performances. Intel recommends selecting an ESD device such that the combined insertion loss (CMC and ESD) is being less than -1.7 dB at 2.5 GHz, -3.5dB at 5 GHz and -6 dB at 7.5 GHz.

Figure 8-31. Output from No ESD (Blue), Ceramic ESD Devices, Si ESD Protection Devices



8.11 USB 3.0 Radio Frequency Interference Impact

At the high speeds of USB 3.0, there are known issues regarding interference with wireless devices when using improperly shielded cables and devices. More information can be found in the white paper shown in Table 8-9, "Reference Documents".

8.12 USB 3.0 Disabling and Termination Guidelines

If some of the USB 3.0 port(s) are not implemented on the platform:

- USB3_TX/RX_DP[3:0] signals may be left unconnected.

§ §

9 SPI Interfaces

9.1 Serial Peripheral Interface (SPI) General Introduction

The Serial Peripheral Interface is a 4-pin interface that provides a potentially lower-cost alternative for system flash versus the Firmware Hub on the LPC bus. The Serial Peripheral Interface is used to support up to two SPI compatible flash devices via two independent chip select pins. Each SPI flash device can be up to 64 MBytes (512 Mbits). The SoC drives the SPI interface clock at either 17 MHz (default), 30 MHz, or 48 MHz. Descriptor mode is required for all platforms. Refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*.

9.2 Serial Peripheral Interface (SPI) Signal Description

Table 9-1. SPI Signals

Signal name	Direction	Shared	Description
SPI_CLK	O	Yes	SPI Clock. The bus owner during idle will drive the SPI Clock signal low.
SPI_MOSI_IO[0]	I/O	Yes	SPI Master OUT Slave IN. Data output pin.
SPI_MISO_IO[1]	I/O	Yes	SPI Master IN Slave OUT. Data input pin.
SPI_IO[3:2]	I/O	Yes	Extended SPI I/O to 4-bit data.
SPI_CS_N[1:0]	O	Yes	SPI Chip Select 0 and 1. Used as the SPI bus request signal for the Flash device.
SPI_TPM_CS_N	O	Yes	SPI Trusted Platform Module (TPM) Chip Select. Used as the TPM dedicated request signal.

9.3 Serial Peripheral Interface (SPI) Topology Guidelines

This section contains details for layout and routing guidelines for SPI interface. SPI flash must be directly connected to the SPI bus of SoC. For specific flash design guide, please also refer to the datasheet provided by flash vendor.

General Design Notes for SPI Interface

- Stackup: hybrid stack-up with material types IT150DA for microstrip layers and IT180I for prepeg an stripline layers allows 2.5 mils dielectric thickness for microstrip and 3 mils dielectric thickness for stripline.
- Resistor tolerance is ± 5%
- 10 layer transitions on general routing are allow
- For 1 or 2 load topologies the SPI minimum Quick Switch/Mux electrical requirements for this guideline are valid. The Quick switch/Mux is intended to choose from different Host drivers (SoC or other type of host device). The Quick switch/Mux can be located any place along the L1 segment.

9.3.1 Single Device Topology Guidelines

Figure 9-1. Single Device Routing Guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

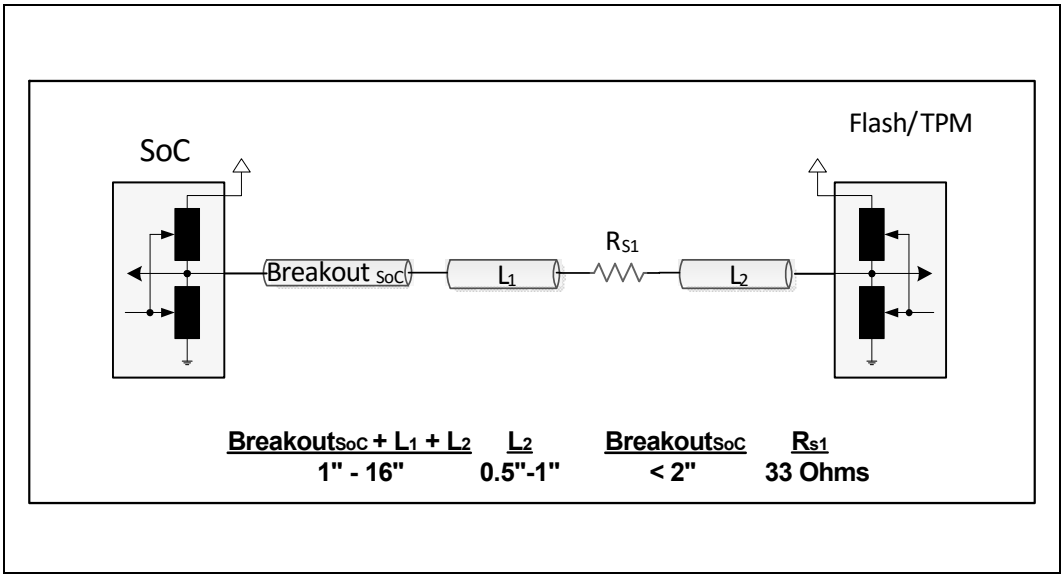


Figure 9-2. Single Device Routing Guidelines for SPI_CS0_N and SPI_CLK

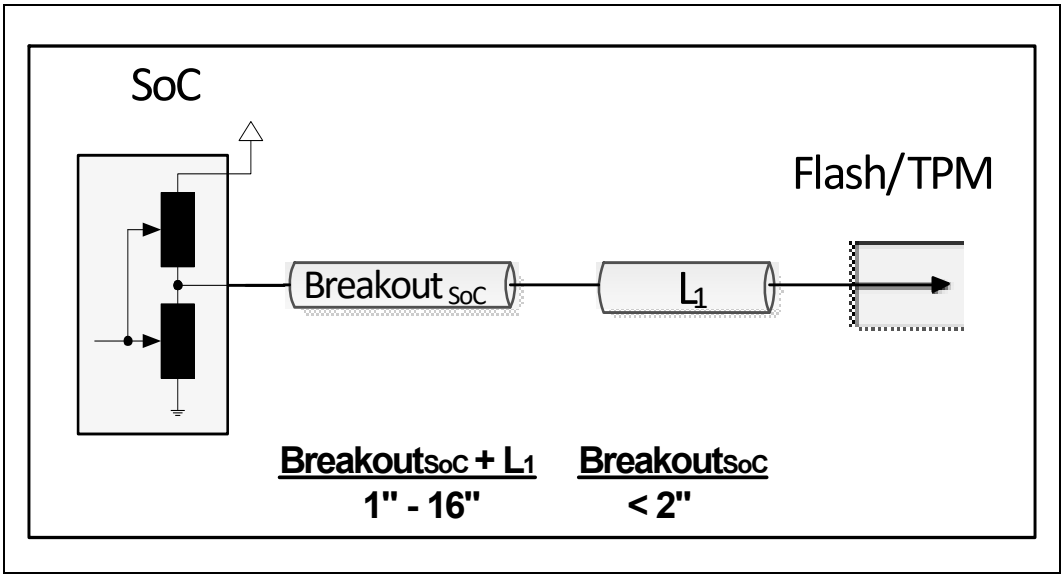


Table 9-2. Single Device Routing Guidelines For SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L2	all			500	1000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	1000	16000	GND
	stripline	3.87	50 Ω ± 10%			GND

Table 9-3. Single Device Routing Guidelines for SPI_CS0_N and SPI_CLK

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	1000	16000	GND
	stripline	3.87	50 Ω ± 10%			GND

Table 9-4. Single Device Layout Recommendations for SPI_MISO_IO, SPI_MOSI_IO, SPI_IO[3:2], SPI_CS0_N and SPI_CLK: Trace Spacing (Mils)

Routing Section	Layer	P3V3 and P1V8 Aggressors			P1V0 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5	5
	stripline	8	4	5	13	4	5	4	4	5	5

- SPI clock and data lines must be length matched to within ± 250 mils.
- SPI clock & chip select lines must be length matched to within ± 250 mils.

Table 9-5. Requirements with 1 load with Quick Switch or Multiplexer

1 LOAD TOPOLOGY	
Propagation Delay	0.25ns (C_{load} = 50 pF)
R_{ON}	5 Ω to 7 Ω (VIN = 0V) 10 Ω to 15 Ω (VIN = 2.4V)

9.3.2 Dual SPI Devices Guidelines

Figure 9-3. Dual Devices STAR Routing Guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

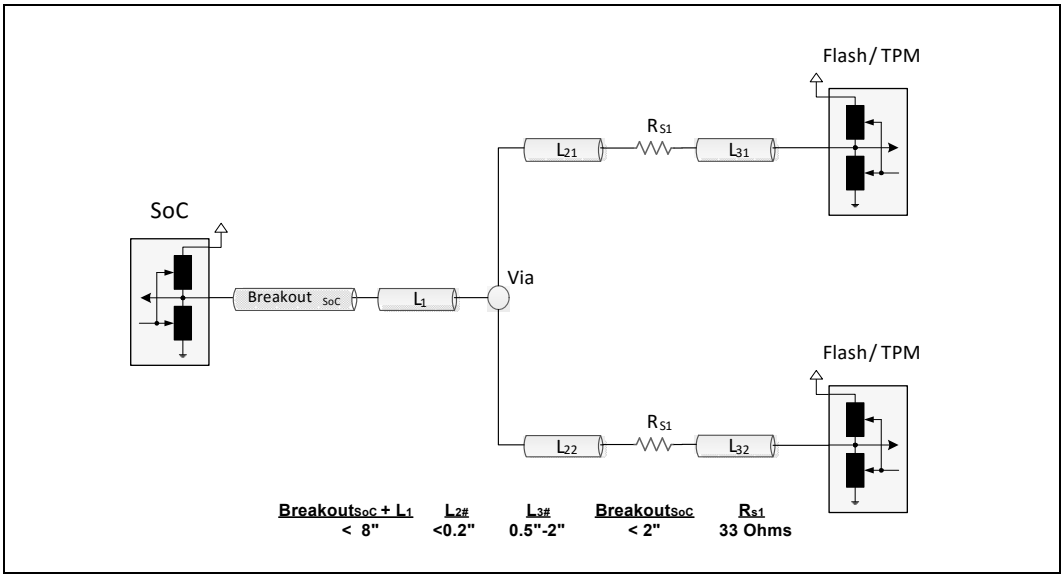


Figure 9-4. Dual Devices DAISY CHAIN Routing Guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

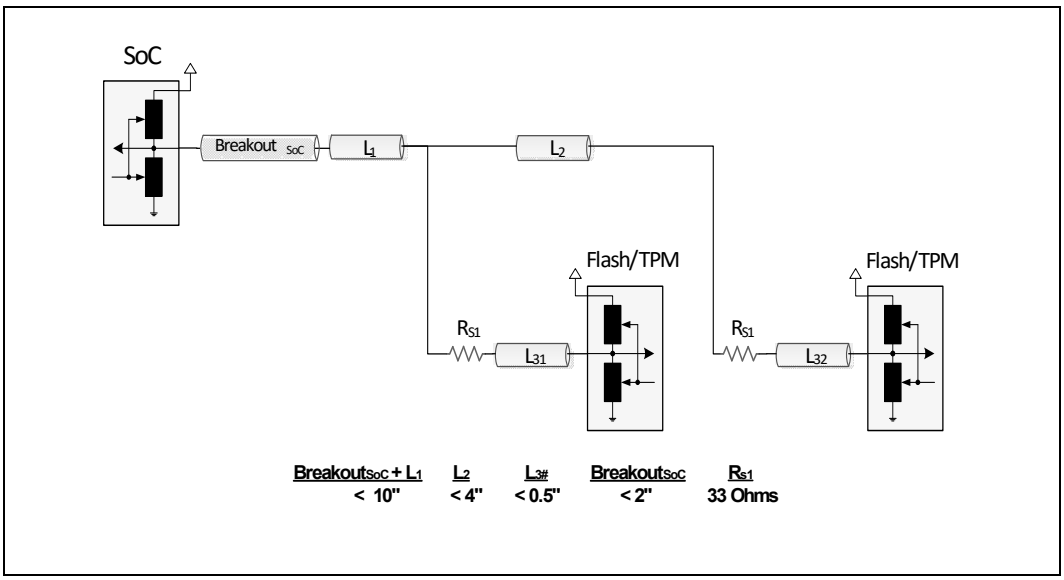


Table 9-6. Dual Devices STAR Routing Guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1	all			0	8000	GND
L2#	all			0	200	GND
L3#	all			500	2000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	1000	12400	GND
	stripline	3.87	50 Ω ± 10%	500	12400	GND

Table 9-7. Dual Devices DAISY CHAIN routing guidelines for SPI_MISO_IO, SPI_MOSI_IO, and SPI_IO[3:2]

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1	all			0	8000	GND
L2	all			0	4000	GND
L3#	all			0	500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	15000	GND
	stripline	3.87	50 Ω ± 10%	0	15000	GND

Table 9-8. Dual Devices Layout Recommendations for SPI_MISO_IO, SPI_MOSI_IO, SPI_IO[3:2] Star and Daisy Chain topologies: Trace Spacing (Mils)

Routing Section	Layer	P3V3 and P1V8 Aggressors			P1V0 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5	5
	stripline	8	4	5	13	4	5	4	4	5	5

Figure 9-5. Dual Devices STAR Routing Guidelines for SPI_CLK

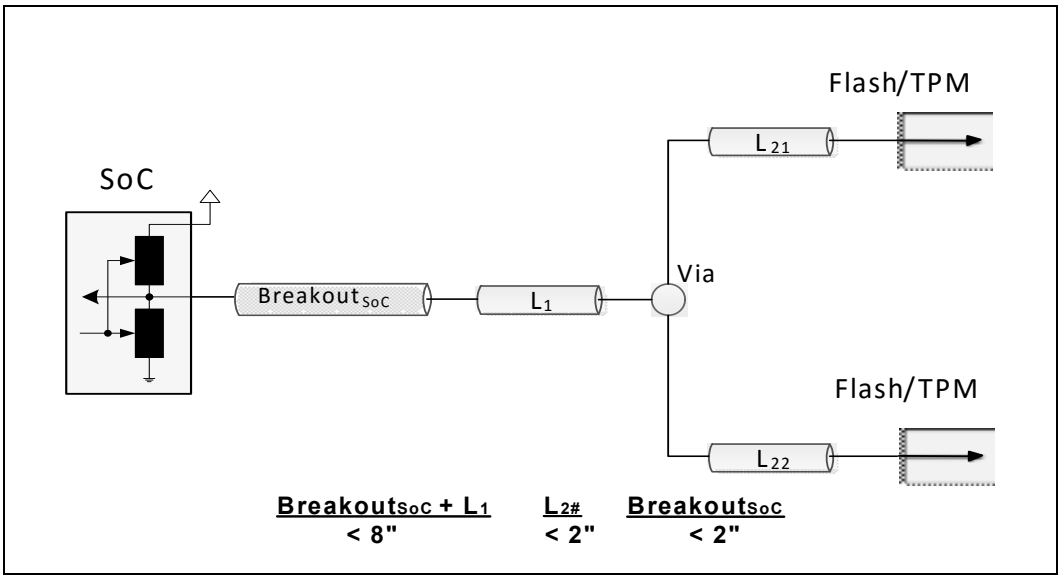


Figure 9-6. Dual Devices DAISY CHAIN Routing Guidelines for SPI_CLK

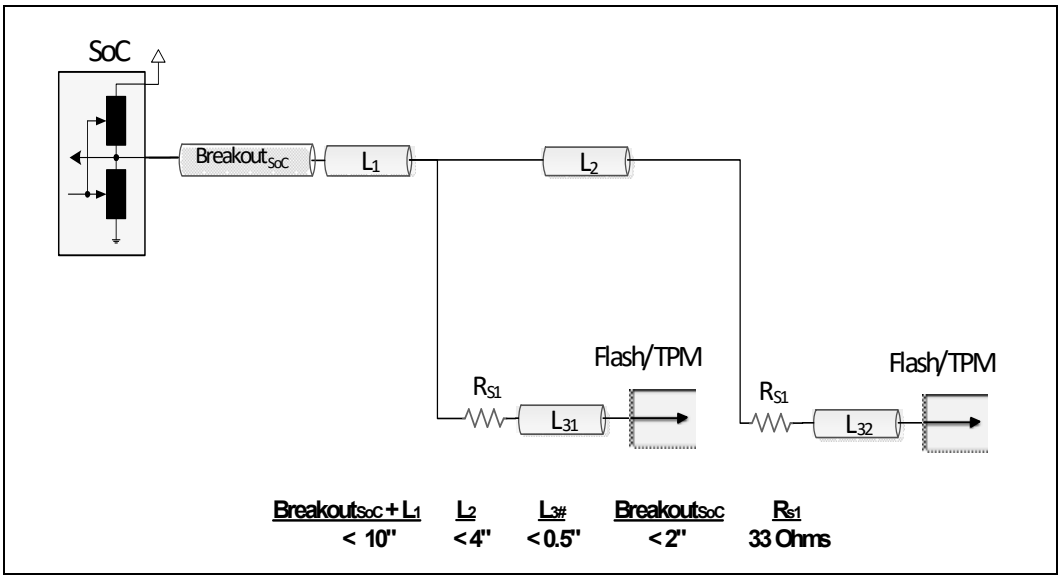


Table 9-9. Dual Devices STAR Routing Guidelines for SPI_CLK

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1	all			0	8000	GND
L2#	all			0	2000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	12000	GND
	stripline	3.87	50 Ω ± 10%			GND

Table 9-10. Dual Devices DAISY CHAIN routing guidelines for SPI_CLK

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1	all			0	10000	GND
L2	all			0	4000	GND
L3#	all			0	500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	15000	GND
	stripline	3.87	50 Ω ± 10%	0	15000	GND

Table 9-11. Dual Devices Layout Recommendations for SPI_CLK Star and Daisy Chain Topologies: Trace Spacing (Mils)

Routing Section	Layer	P3V3 and P1V8 Aggressors			P1V0 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5	5
	stripline	8	4	5	13	4	5	4	4	5	5

SPI_CLK & SPI_MOSI_IO (including all the Master Output Pins during Dual and Quad I/O Operation) must be length matched to within 500 mils.

SPI_CLK & SPI_CS_N must be length matched to within ± 250 mils.

SPI branches need to have length matching of ± 100 mils.

Table 9-12. Requirements with 2 loads with Quick Switch or Multiplexer

2 LOAD TOPOLOGY	
Propagation Delay	0.25ns (C_{load} = 50 pF)
R_{ON}	5 Ω to 7 Ω (VIN = 0V) 10 Ω to 15 Ω (VIN = 2.4V)

9.3.3 Terminating Unused SPI Signals

If the SPI interface is not implemented on the platform all SPI signals may be left unconnected.

9.3.4 SPI Dual Footprint - SO8 and SO16 Packages

Although the SPI interface is comprised of a 4 signal bus, SPI devices may be found in both 8-pin and 16-pin SOIC packages. This section contains an example of an SO8 and SO16 dual footprint to accommodate both packages on the motherboard. Refer to the vendor(s) data sheet for package details.

Figure 9-7. SPI Dual Footprint for SO8 and SO16 Packages

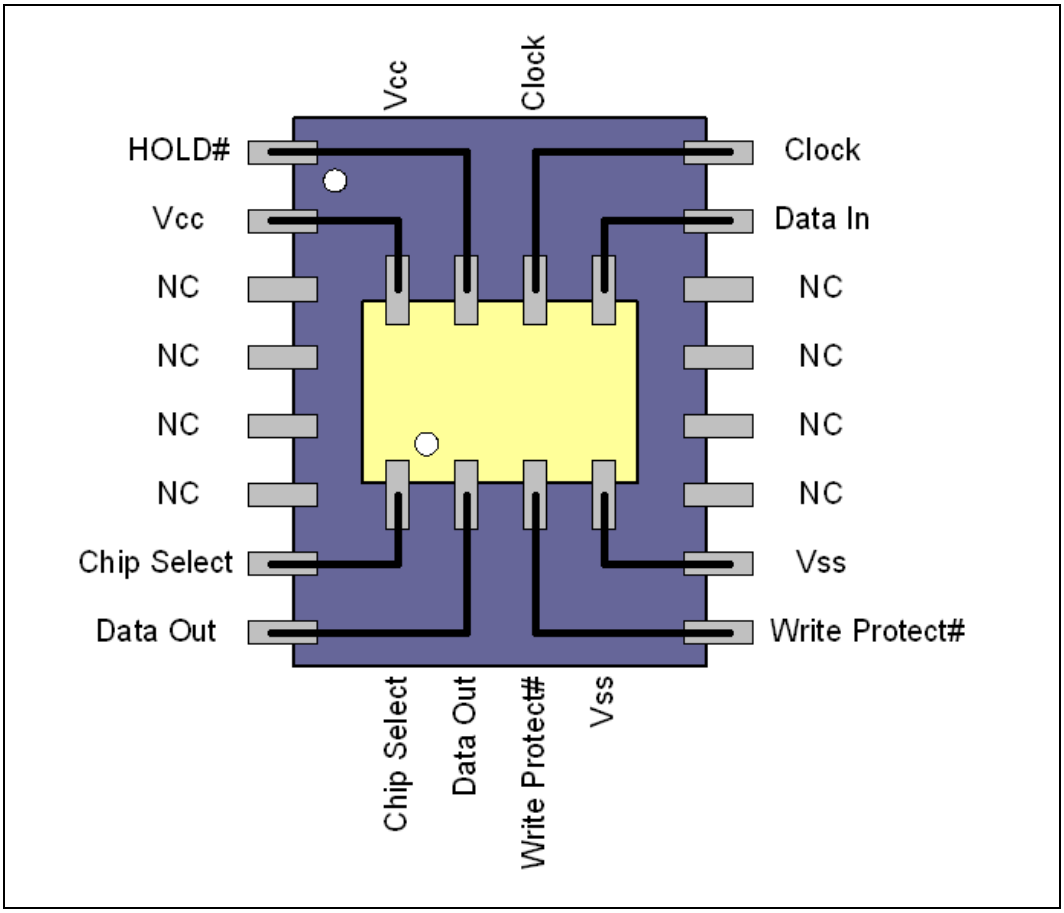


Table 9-13. Serial Flash Vendors

Vendor	Website
ATMEL	http://www.atmel.com/
MACRONIX	http://www.mxic.com.tw
SST/MICROCHIP	http://www.microchip.com
NUMONYX/MICRON	http://www.micron.com/
WINBOND	http://www.winbond.com/
SPANSION	http://www.spansion.com/
EON	http://www.eonssi.com/
AMIC	http://www.amictechnology.com
GIGADEVICE	http://www.gigadevice.com
FIDELIX	http://www.fidelix.co.kr/
Chingis Technology	http://www.chingistek.com/
PMC	http://www.pmcflash.com/

Note: OEMs must fully validate any SPI flash device to ensure compatibility with their platforms. This should not be considered a complete list of SPI vendors and is not an indication of Intel approved devices or vendors. Please contact your preferred flash vendor directly to determine if they have a compatible device.

9.4 TPM Support

The SoC only supports one dedicated TPM on the system. The TPM attached to the SoC may be using LPC or SPI.

There are some rules for TPM support:

- Soft Strap #30 tells the SoC to enable TPM on SPI or LPC interfaces.
- Soft Strap #10 tells the SoC what clock frequency to use when talking to TPM on SPI.
- TPM requires the support for the interrupt routing. TPM interrupt is completely independent from the SPI controller.

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10 Embedded Multimedia Card (eMMC) Interface

The Embedded Multi-Media Controller (eMMC) of SoC is meeting the eMMC v5.0 specification.

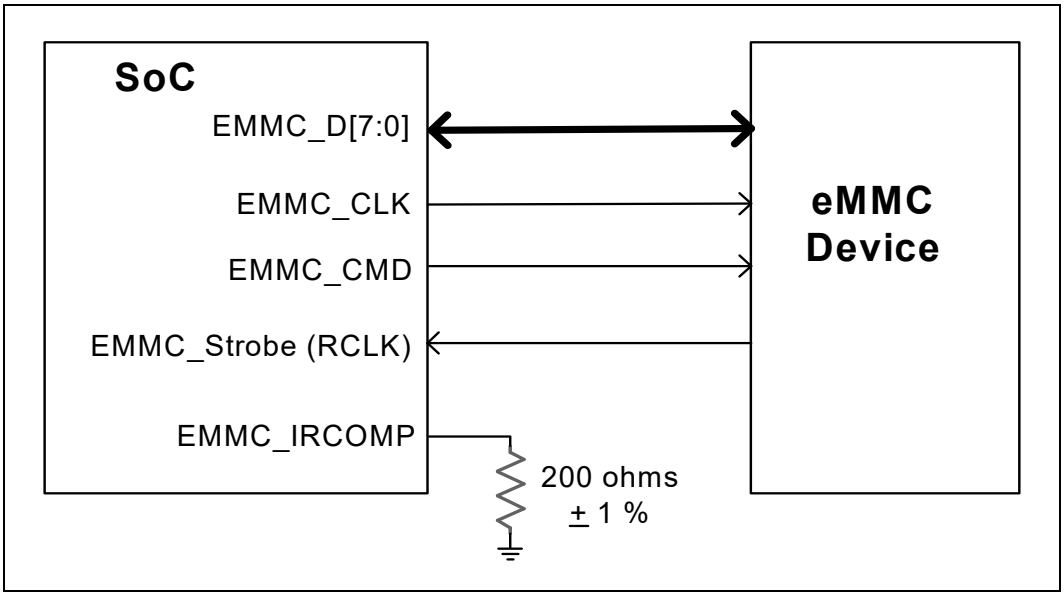
General Design Guide Lines

- Maximum number of vias is 2.
- Add a GND stitching via within 50 mils of a signal layer transition via.
- Routing can be either stripline or microstrip, but all eMMC signals must be on the same layer.
- Stack up: A hybrid stack-up with material type IT150DA for microstrip layers and IT180I for prepreg and stripline layers plus 2.5 mil dielectric thickness for microstrip and 3 mil thickness for stripline.
- Length match the DATA to DATA signals within 250 mils from the die bump up to the eMMC down device (Includes PKG length).
- Length match CMD signals to CLK and RCLK (Strobe) within 250 mils from the die bump up to the eMMC down device (Includes PKG length).
- Resistor tolerance is ± 5%.
- To drive 6” of routing the device to be used should have a Rise/Fall time of less than 0.8ns when driving a 15ps test load, it should have a drive strength of 40 Ω or less, and a device capacitance < 3pF.
- No more than 3 NC balls should be soldered on the breakout of the eMMC device.
- Data to Data Spacing can be reduced down to the following for no more than 10% of the total routing.
  - Microstrip 3*h*
  - Stripline 2*h*
- The Spacing from Clock to Data and other MISC IO signals can be reduced down to the following for no more than 10% of the total routing.
  - Microstrip 5*h*
  - Stripline 3*h*

Table 10-1. eMMC Signals

Signal name	Direction	Shared	Description
EMMC_CLK	O	Yes	EMMC Clock.
EMMC_CMD	I/O	Yes	EMMC command. The platform requires a 20 kΩ pull-up resistor, tied to 1.8V for this signal.
EMMC_D[7:0]	I/O	Yes	EMMC data bus. The platform requires a 20 kΩ pull-up resistor, tied to 1.8V for these signals.
EMMC_IRCOMP	I/O	No	RCOMP for the eMMC interface: The platform requires a 200 Ω ± 1% resistor connected to ground (Vss).
EMMC_STROBE (RCLK)	I	Yes	This signal is a read strobe sometimes referred to as the read or return clock (RCLK) because the EMMC_CLK signal is taken and sent to the SoC with data on a read cycle.

Figure 10-1. eMMC Interface Topology



Note: 20 kΩ pull-ups are required for EMMC_D[7:0] and EMMC_CMD.

Figure 10-2. EMMC_CLK To Down Device Topology

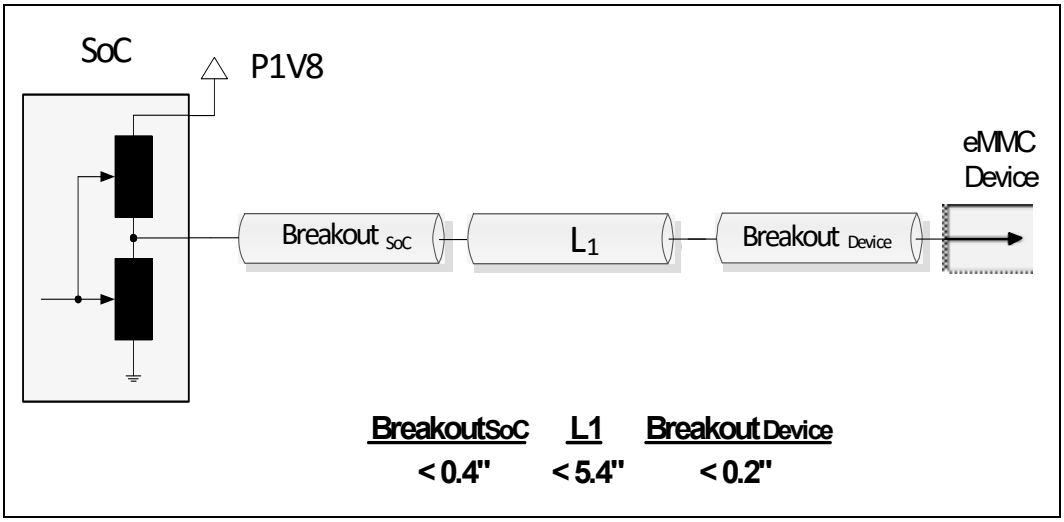


Table 10-2. EMMC_CLK Routing Guidelines To A Down Device

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	5400		GND
	stripline	3.87	50 Ω ± 10%				GND
Entire Signal				0	6000	2	GND

Table 10-3. EMMC_CLK Layout Recommendations To A Down Device: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-3. EMMC_STROBE (RCLK) for Down Device Topology

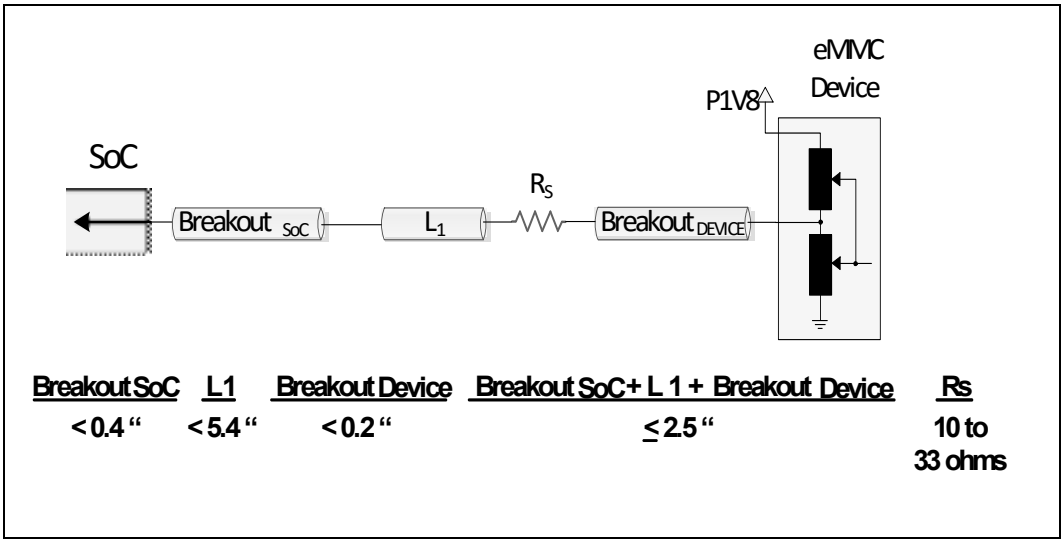


Table 10-4. EMMC_STROBE (RCLK) Routing Guidelines To A Down Device

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	5400		GND
	stripline	3.87	50 Ω ± 10%				GND
Entire Signal				0	6000	2	GND

Table 10-5. EMMC_STROBE (RCLK) Layout Recommendations To A Down Device: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-4. EMMC_CMD and EMMC_D to Down Device Topology

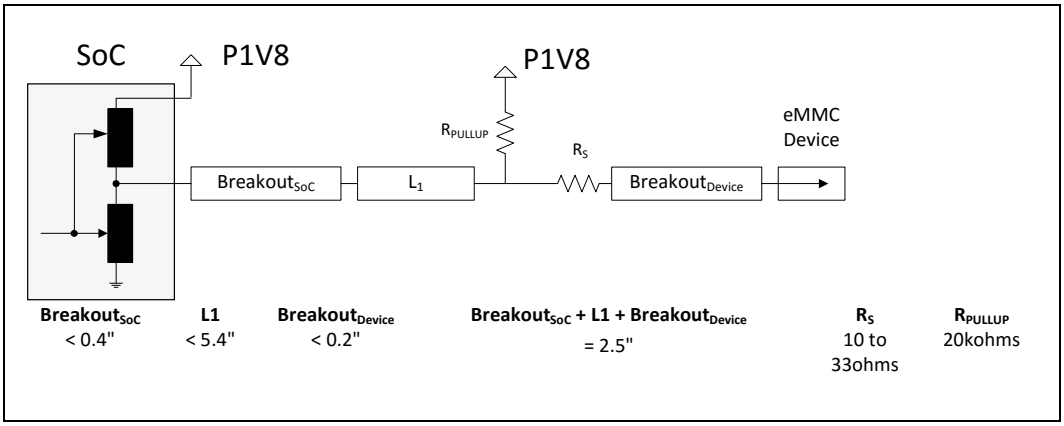


Table 10-6. EMMC_CMD and EMMC_D Routing Guidelines To A Down Device

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	5400		GND
	stripline	3.87	50 Ω ± 10%				GND
Entire Signal				0	6000	2	GND

Table 10-7. EMMC_CMD and EMMC_D Layout Recommendations To A Down Device: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-5. EMMC_CLK Topology To A Connector

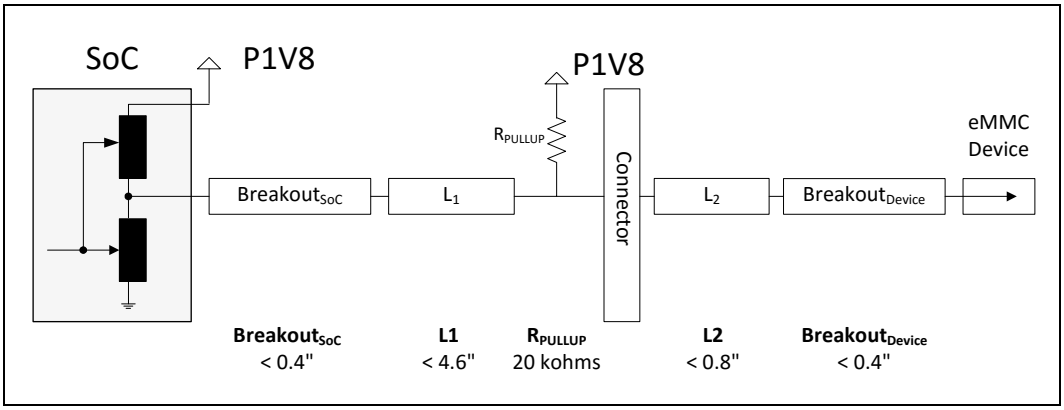


Table 10-8. EMMC_CLK Routing Guidelines To A Connector

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	4600		GND
	stripline	3.87	50 Ω ± 10%				GND
L2	microstrip		50 Ω ± 15%	0	800		GND
	stripline		50 Ω ± 10%				GND
Entire Signal				0	6000	4	GND

Table 10-9. EMMC_CLK Layout Recommendations To A Connector: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
L2	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-6. EMMC_STROBE (RCLK) Topology To A Connector

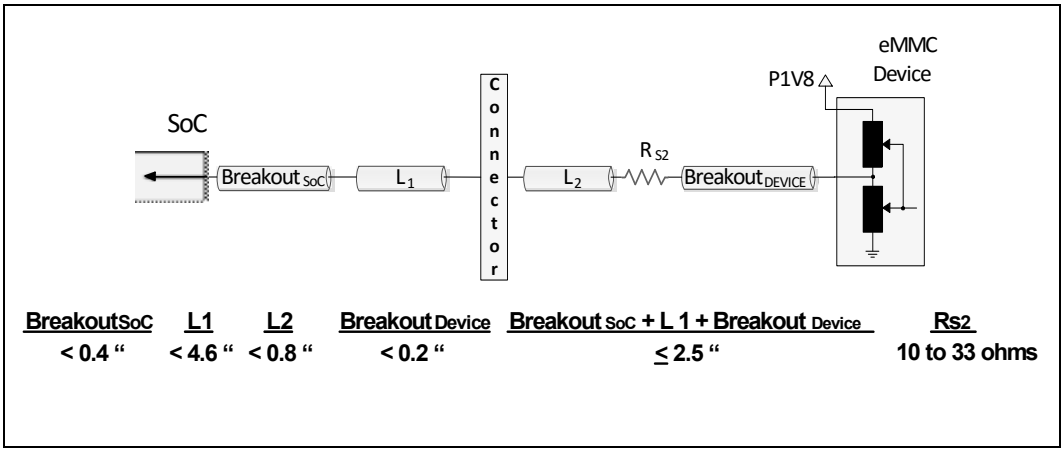


Table 10-10. EMMC_STROBE (RCLK) Routing Guidelines To A Connector

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	4600		GND
	stripline	3.87	50 Ω ± 10%				GND
L2	microstrip		50 Ω ± 15%	0	800		GND
	stripline		50 Ω ± 10%				GND
Entire Signal				0	6000	4	GND

Table 10-11. EMMC_STROBE (RCLK) Layout Recommendations To A Connector: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
L2	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-7. EMMC_CMD and EMMC_D Topology To A Connector

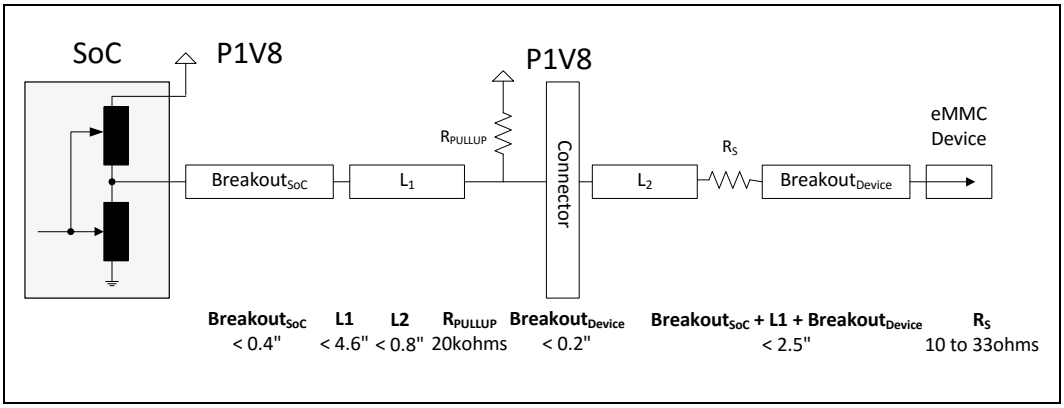


Table 10-12. EMMC_CMD and EMMC_D Routing Guidelines To A Connector

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Via Count	Reference
				min	max		
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	400		GND
	stripline	3.5	52 Ω ± 10%				GND
$Breakout_{Device}$	microstrip	3.5	54 Ω ± 15%	0	200		GND
	stripline	3.5	52 Ω ± 10%				GND
L1	microstrip	4.1	50 Ω ± 15%	0	4600		GND
	stripline	3.87	50 Ω ± 10%				GND
L2	microstrip		50 Ω ± 15%	0	800		GND
	stripline		50 Ω ± 10%				GND
Entire Signal				0	6000	4	GND

Table 10-13. EMMC_CMD and EMMC_D Layout Recommendations To A Connector: Trace Spacing (Mils)

Routing Section	Layer	Type eMMC DATA & CMD			Type eMMC Clk			P1V0, P1V8, P3V3 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
$Breakout_{Device}$	microstrip	4	4	5	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	4	4	5	
L1	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
L2	microstrip	7H	8	10	7H	8	10	7H	8	10	5	4	5	
	stripline	5H	8	10	5H	8	10	5H	8	10	4	4	5	
Entire Signal														5

Figure 10-8. EMMC_IRCOMP circuit

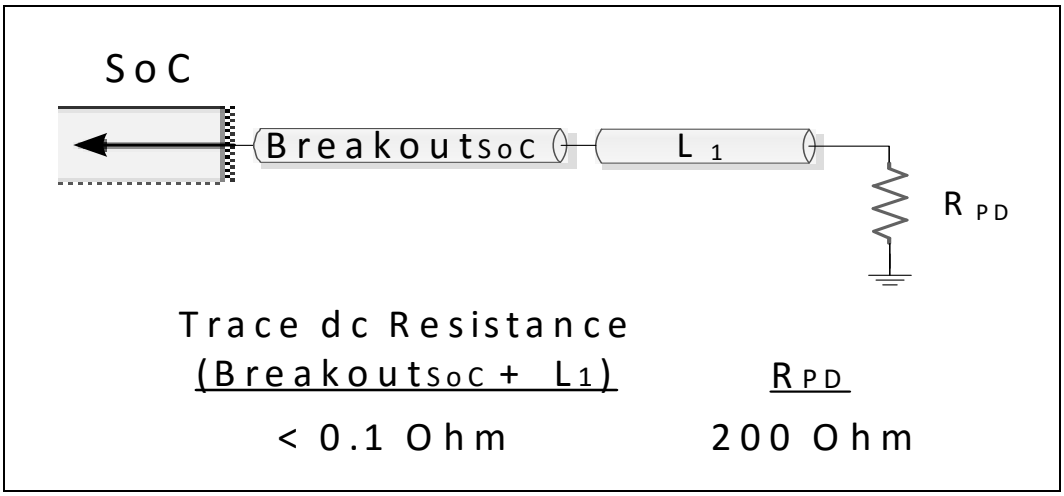


Table 10-14. EMMC_IRCOMP Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	P3V3 and P1V8 Aggressors			P1V0 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5	5
	stripline	8	4	5	13	4	5	4	4	5	5

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11 System Management Bus Interfaces

The SoC provides multiple System Management Bus (SMBus) controller. The Interfaces comply to SMBus Specification version 3.0. The controllers include Legacy SMBus, Host SMBus, Platform Environment Control Interface (PECI) SMBus, Three Intel ME SMBus, LAN SMBus and Three Innovation Engine SMBus.

Host SMBus controllers are also capable of operating in a mode to communicate with I2C compatible devices.

Table 11-1. Signal Names

Signal Name	Direction	Shared	Description
SMB_LEG_CLK	I, O-OD	Yes	**SMBus Clock (SMBCLK)**
SMB_LEG_DATA	I, O-OD	Yes	**SMBus Data (SMBDAT)**
SMB_LEG_ALRT_N	I, O-OD	Yes	**SMBus Alert (SMBALERT#):** This signal wakes the system or generates a System Management Interrupt (SMI).
SMB_HOST_CLK	I, O-OD	Yes	**SMBus Clock (SMBCLK)**
SMB_HOST_DATA	I, O-OD	Yes	**SMBus Data (SMBDAT)**
SMB_PECI_CLK	I, O-OD	Yes	**SMBus Clock (SMBCLK)**
SMB_PECI_DATA	I, O-OD	Yes	**SMBus Data (SMBDAT)**

11.1 SMBus Design Considerations

The total bus capacitance and device capabilities must be considered when designing the SMBus segments. Routing the SMBus to the PCI slots is more challenging since capacitance may be added on the bus. This extra capacitance has a large effect on the bus time constant which affects the bus rise and fall times.

General Design Considerations are listed as the following:

- The device class (high/low power), as with most designs, use primarily high-power devices.
- The amount of the Suspend Well current available, i.e., minimizing the Suspend Well load.
- The SMBUS channels share the same on-chip design requiring 3.3V to operate. This includes the IE and ME SMBus channels.
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally, the limiting agent for the resistor size is the SMBus device current sinking ability. The pull-up resistor cannot be made so large that the bus time constant (Resistance x Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance for a physical segment is 400 pF. This encompasses both physical routing and devices/connectors loading.
- The SMBus devices that operate in Suspend to RAM (SUS mode) must be powered by the Suspend Well supply.
- Intel recommends that the I^2C devices be powered by the VCC_CORE supply. During an SMBus transaction in which the device is sending information to the SoC processor, the device does not release the SMBus if the SoC processor receives an asynchronous reset. VCC_CORE allows the BIOS to reset the device if necessary. The SMBus 2.0-compliant devices have a timeout capability which makes them less susceptible to this I^2C issue. This allows flexibility in choosing a voltage supply.
- If the SMBus is connected to PCIe*, it must be connected to all PCIe slots.

Figure 11-1. SMBus Layout Configuration

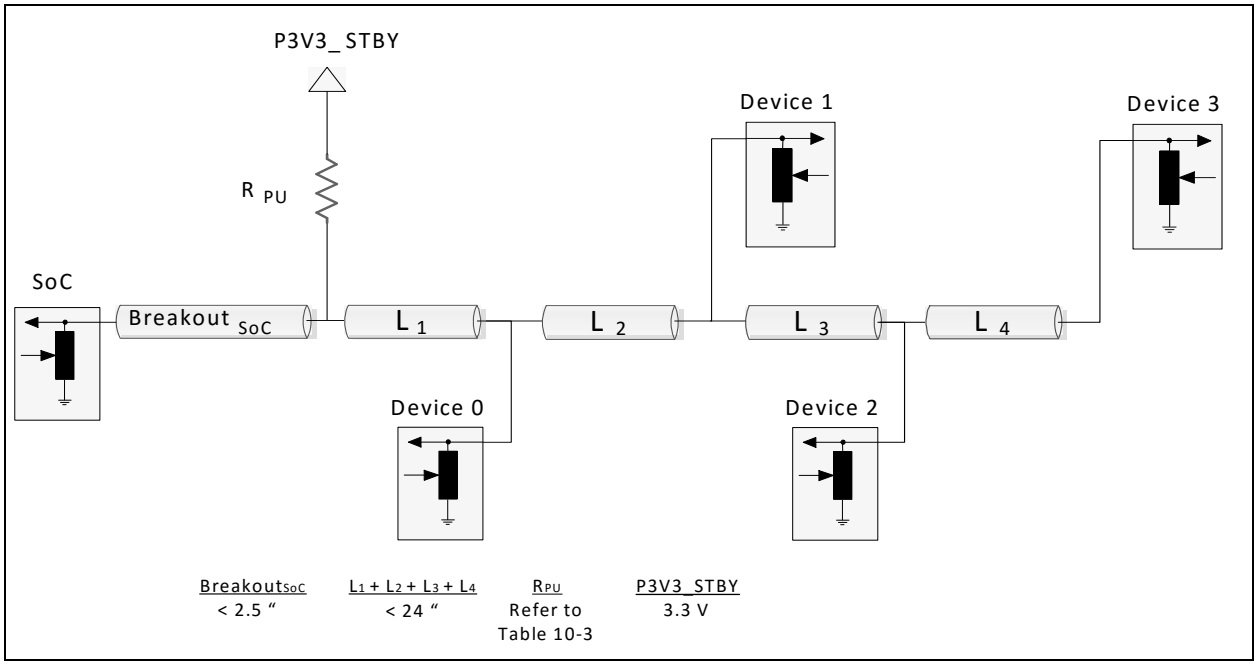


Table 11-2. SMBus Layout Recommendations (for all SoC SMBus signals SMBCLK, SMBDATA, and SMBALERT#)

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1+L2+L3+L4	all			0	24000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	26500	GND
	stripline	3.87	50 Ω ± 10%	0	26500	GND

Notes:
1. Route using a daisy chain topology. No stubs allowed.
2. For speeds above 400 kHz all elements on the bus assume a Ron of 20 Ω.
3. If the driver is weaker than 20 Ω then the pull-up and series resistors will need to be adjusted to comply with rise time and Vil/Vih specifications.
4. Use high-speed routing rules to minimize noise the effects on a worst case Vol at the translator output and the minimum Vil at the receiver.
5. For capacitance calculations use 10 pF for driver elements and 2.8 pF per inch of trace length.

Table 11-3. SMBus Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Table 11-4. Capacitance Estimates for Calculating R_{PU} Values

Capacitance	Pull-up range (100 kHz)	Pull-up range (400 kHz)	Pull-up range (1000 kHz)
10 pF to 40 pF	1.1 kΩ to 9 kΩ	2.2 kΩ	1.0 kΩ to 1.2kΩ
40 pF to 100 pF	1.2 kΩ to 7.2 kΩ	0.6 kΩ to 2.6 kΩ	750 Ω
100 pF to 200 pF	1.2 kΩ to 4.0 kΩ	0.6 kΩ to 1.3 kΩ	500 Ω
200 pF to 300 pF	1.2 kΩ to 2.6 kΩ	0.6 kΩ to 0.9 kΩ	320 Ω
300 pF to 400 pF	1.2 kΩ to 2 kΩ	0.6 kΩ	240 Ω

Notes:
1. Use 3.3 pF per routed inch.
2. Use 10 pF per active device connected.
3. Use 40 pF for a PCIe* active card.
4. Use 2 pF per DIMM connector.
5. The pull-up resistor tolerance is ± 5%.

11.1.1 Legacy SMBus Connections To DDR4

Intel provides the following example to connect the shared Legacy SMBus to SDA and SCL pins for DDR4 serial presence detect (SPD) application.

The example here is using voltage translator: PCA9617. Customers can use other parts for this purpose. If a different voltage translator is used, customers need to contact the part vendor for the design guide details.

Figure 11-2. Legacy SMBus to the Voltage Translator Layout Configuration

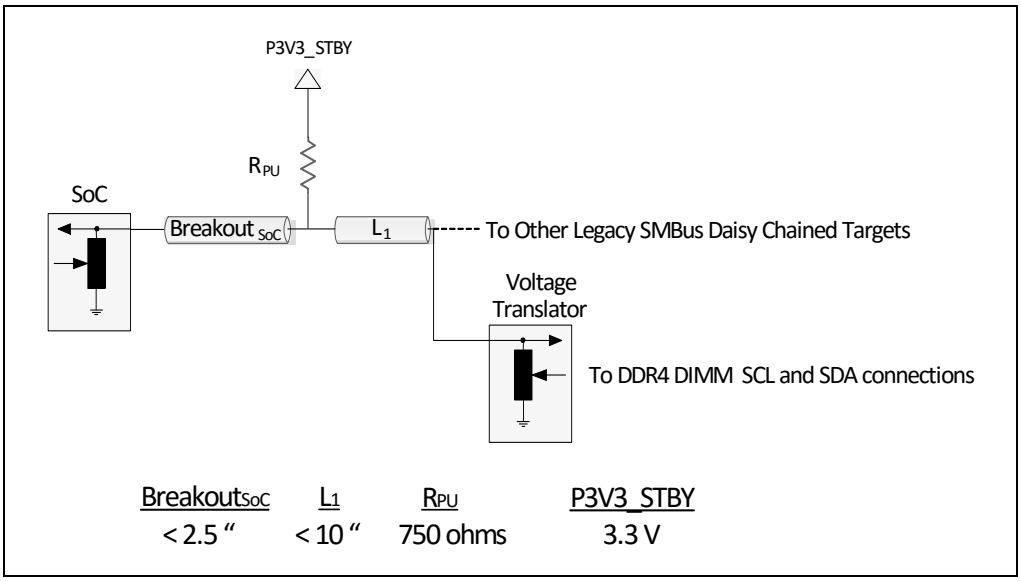


Table 11-5. Legacy SMBus to Voltage Translator Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	12500	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Route using a daisy chain topology. No stubs allowed.
2. Length matching to 250 mils is required between DDR_SCL and DDR_SDA traces.
3. Resistor tolerance is ± 5%.

Table 11-6. Legacy SMBus to Voltage Translator Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 11-3. Legacy SMBus - Voltage Translator to 4 x DIMM Layout Configuration

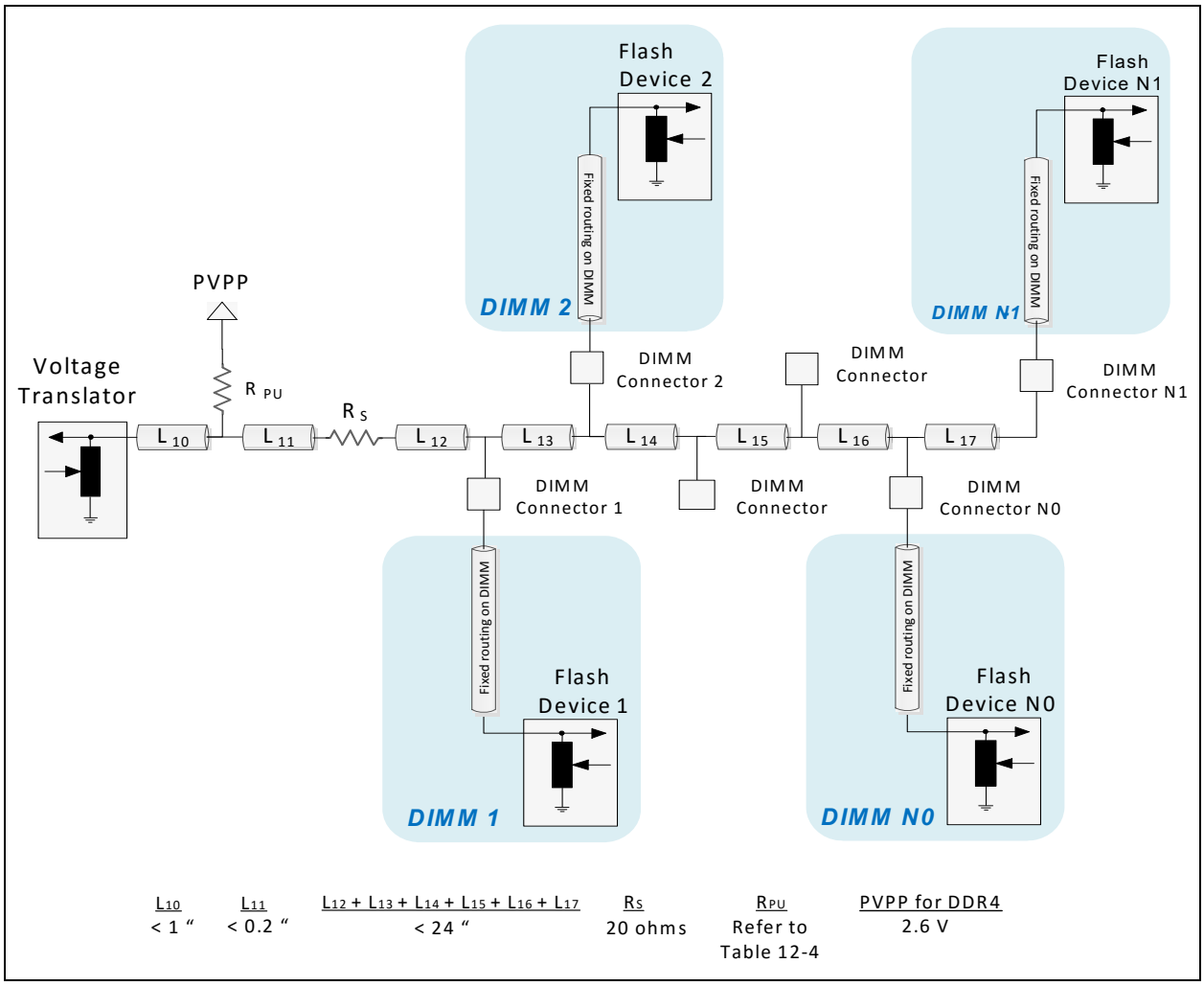


Table 11-7. Legacy SMBus - Voltage Translator to DIMM Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
L10	microstrip	3.5	54 Ω ± 15%	0	1000	GND
	stripline	3.5	52 Ω ± 10%			GND
L11	all			0	200	GND
L12 - L17		4.0		0	24000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	25200	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Route using a daisy chain topology. No stubs allowed.
2. Length matching to 250 mils is required between DDR_SCL and DDR_SDA traces.
3. For speeds above 400 kHz all elements on the bus assume a Ron of 20 Ω.
4. If the driver is weaker than 20 Ω then the pull-up and series resistors will need to be adjusted to comply with rise time and Vil/Vih specifications.
5. Use high-speed routing rules to minimize noise the effects on a worst case Vol at the translator output and the minimum Vil at the receiver.
6. For capacitance calculations use 10 pF for driver elements and 2.8 pF per inch of trace length.

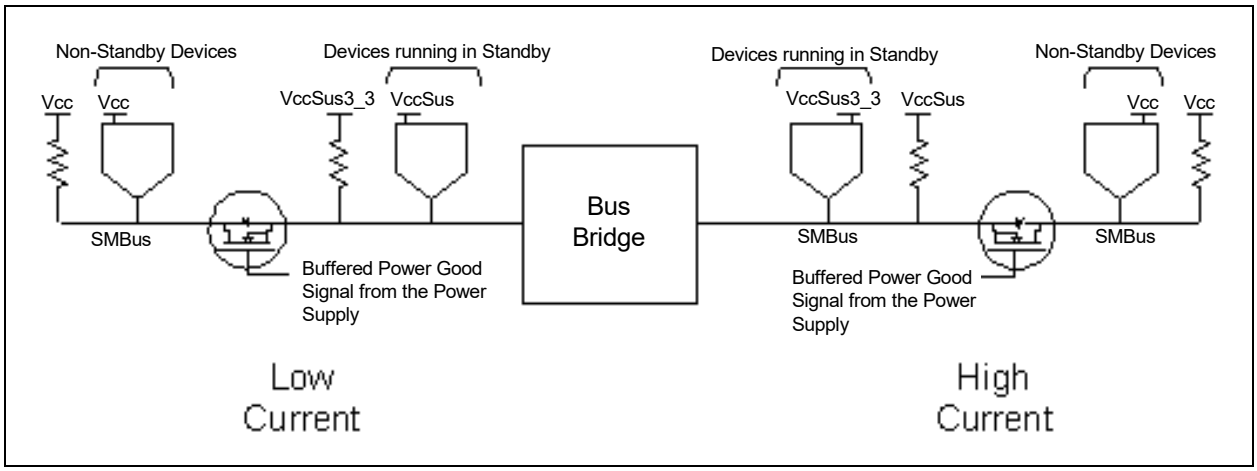
Table 11-8. Legacy SMBus - Voltage Translator to DIMM Layout Recommendations

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
L10	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

11.2 High/Low-power Mixed Architecture

This design allows for current isolation of the high- and low-current devices while also allowing the SMBus devices to communicate while in S3. The VCC_SUSPEND leakage is minimized by keeping the nonessential devices on the core supply. This is accomplished with the use of a FET to isolate the devices powered by the core and suspend supplies.

Figure 11-4. High/Low-Power Mixed VCC_SUSPEND/ VCC_CORE Architecture



The additional considerations for a mixed architecture are:

- The bus bridge must be powered by VCC_SUSPEND.
- Devices that are powered by the VCC_SUSPEND well must not drive into the other devices that are off. This is accomplished with the bus switch.
- The bus bridge can be a device like the Philips* PCA9515.

11.3 Calculating the Physical Segment Pull-Up Resistor

Table 11-9 is provided as a reference for calculating the value of the pull-up resistor that is used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus-bridge device like the Philips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 11-9. Bus Capacitance Reference Chart

Device	No. of devices/ trace length	Capacitance includes	Capacitance (pF)
SoC	1	Pin Capacitance	12
CK-µS	1	Pin Capacitance	6
DIMMs		Pin Capacitance (10 pF) + 1” worth of trace capacitance (2 pF/inch) per DIMM and 2-pF connector capacitance per DIMM	28
SMBus Trace Length in Inches	=24	3.3 pF per inch of trace length	79.2
	=36		118.8
	=48		158.4

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12 Real-Time Clock (RTC)

The RTC module in the SoC provides a battery backed-up data and time keeping device with two banks of static RAM with 128 Bytes each.

- Keeping the date and time
- Storing system data in its RAM when the system is powered down

The SoC RTC module requires an external oscillating source of 32.768 kHz connected on the RTC_X1_PAD and RTC_X2_PAD balls.

Figure 12-5 shows the external circuitry that comprises the oscillator of the SoC RTC.

Note: If the design does not support an RTC battery, the VRTC circuitry is not needed and the VCCRTC_3P3_G3 pin must be tied to the V3P30 rail. The 32.768 kHz clock generator circuit is needed for the SoC.

Table 12-1. RTC Signals

Signal Names	Direction	Shared	Description
RTC_X1_PAD	I	No	**Crystal/Input 1:** This signal is connected to a 32.768KHz crystal (max 50K ESR). If using an external oscillator, this signal Vih must be within the range of 0.8V to 1.5V (1.5V max).
RTC_X2_PAD	O	No	**Crystal Output 2:** this signal is connected to the 32.768KHz crystal (Max 50K ESR). If using an external oscillator, this signal should be left floating.
BVCCRTC_EXTPAD	I,O	No	**Internal VRM Filter:** Connect filter capacitor between this signal and ground.
COREPWROK	I	No	**Core Power OK:** When asserted this active-high input signal indicates that all of the platform board Voltage Regulators (VRs) supplying the SoC core power rails have been stable for at least 10 ms. COREPWROK can be driven asynchronously. When COREPWROK is de-asserted, the SoC asynchronously asserts the active-low PMU_PLTRST_N signal.
INTRUDER_N	I	No	**Intruder Detect:** This signal can be used to disable the system if the box is detected open.
RSMRST_N	I	No	**Resume (SUS Power Well) Reset:** When high, this pin indicates that all SUS power rails are valid and stable. A number of hard strap options are set when RSMRST_N assets. See Chapter 4, "Strapping and Configuration in the Denverton SoC Product Family Preliminary EDS.
RTEST_N	I	No	**RTC Battery Test:** RTC Battery Test: An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. If the battery is missing/weak, this signal appears low (asserted) at boot just after the suspend power rail (V3P3) is up since it will not have time to meet Vih when V3P3A is high. Upon booting, BIOS should recognize that RTCRCT# was asserted and clear CMOS RAM. ***Note:*** Unless CMOS is being cleared (only to be done in the G3 power state) or the battery is low, the signal input must always be high when all other RTC power planes are on.
SRTCRST_N	I	No	**RTC Reset:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. When asserted, this signal resets all register bits in the RTC well. ***Notes:*** 1. Unless registers are being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the signal should go high (de-asserted) before the RSM_RST_N signal goes high (de-asserted).
VCCRTC_3P3_G3	I	No	Battery backed power supply for the RTC IP block.

The SoC uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTC_X2_PAD signal. Internal to the processor, the RTC_X1_PAD signal is amplified to drive internal logic and generate a free-running-full-swing-clock output for system use. This output clock is called PMU_SUSCLK.

This is illustrated in Figure 12-1.

Figure 12-1. RTC_X1_PAD and PMU_SUSCLK Relationship in the SoC

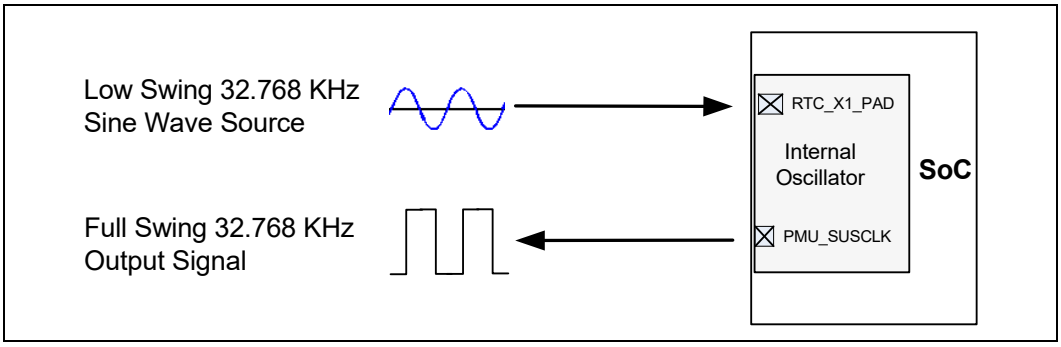


Figure 12-2. RTC and RTC Well Signals Generic Connections

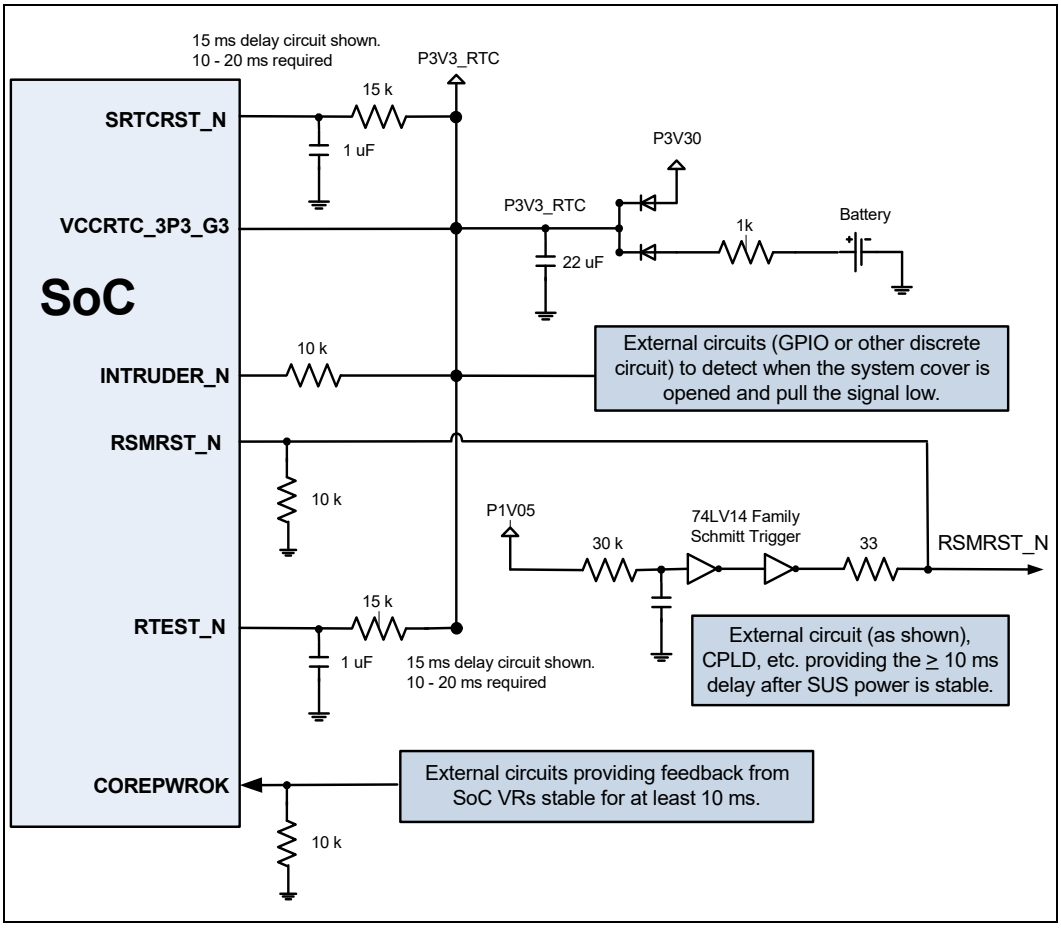
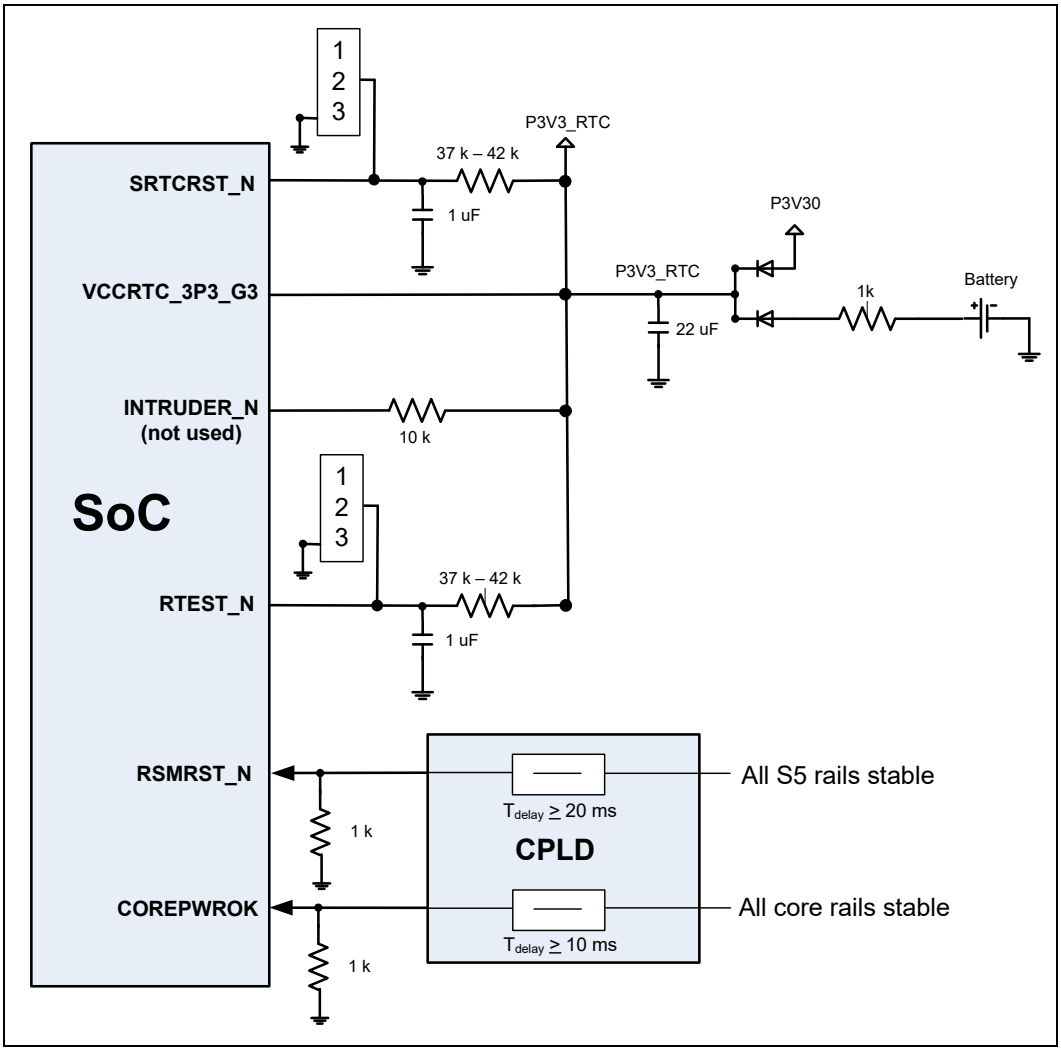


Figure 12-3. Harcuvar and Cormorant Lake RTC and RTC Well Signals



Note: The resistor value used on Harcuvar and Cormorant Lake schematic for SRTCRST_N and RTEST_N is 15K. The measurement shows Trtc timing cannot meet the timing request (10ms <Trtc <20ms) in power sequence Figure 33-1 and 33-2 of document #558579 *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*. The test shows the resistor value needs to be updated to 37K~42K on CRB to meet minimum 10ms request. With violation, Unstable G3 boot up issue might be seen.

Figure 12-4. Aspen Cove RTC and RTC Well Signals

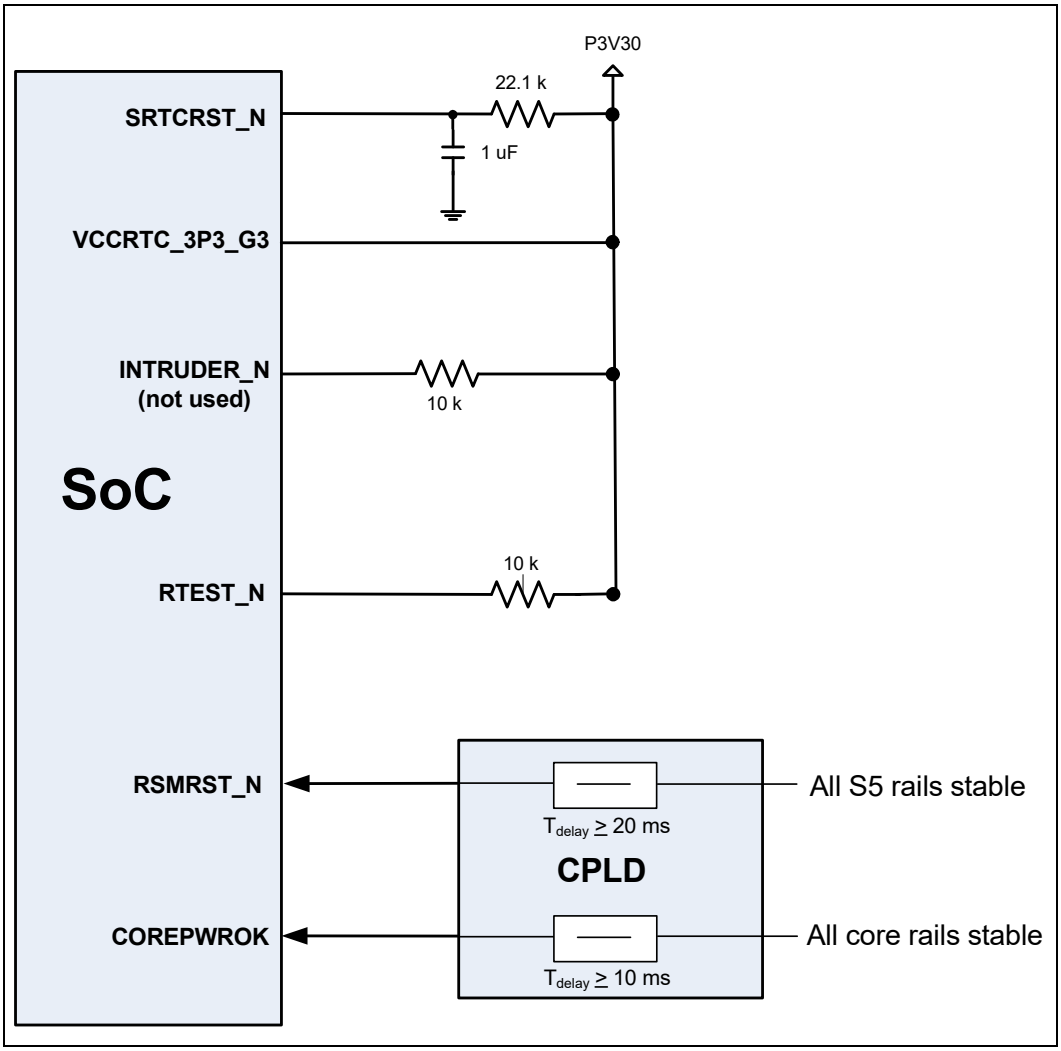
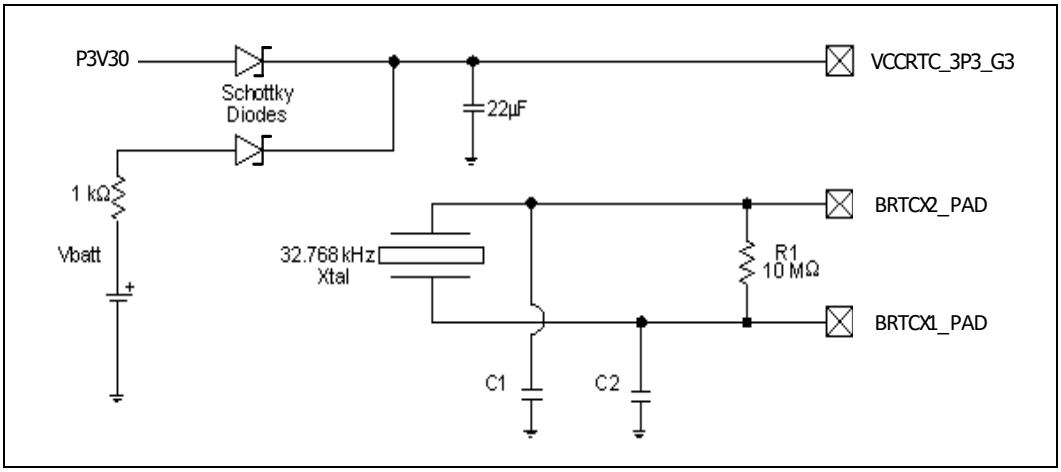


Figure 12-5. External Circuitry for the SoC RTC XTAL and Battery



Notes:

1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on a crystal load of 12.5 pF.
2. Reference designators are arbitrarily assigned.
3. Vbatt is the voltage provided by the battery.
4. VCCRTC_3P3_G3, RTC_X1_PAD, and RTC_X2_PAD are the SoC pads.
5. VCCRTC_3P3_G3 powers the SoC RTC well.
6. RTC_X1_PAD is the input to the internal oscillator.
7. RTC_X2_PAD is the feedback for the external crystal.

12.1 RTC Layout Considerations

Since the RTC circuit is sensitive and requires highly accurate oscillation, reasonable care must be taken during the layout and routing of the RTC circuit. Some recommendations are:

- Reduce the trace capacitance by minimizing the RTC trace length. A trace length less than 1 inch on each branch (from the crystal terminal to the RTC_Xn_PAD ball) is recommended.
- Keeping routing on the RTC circuit basic to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the boards' material.
- Reduce the trace signal coupling by avoiding routing of adjacent high speed signals close to RTC_X1_PAD and RTC_X2_PAD.
- Using a ground guard plane is highly recommended.

The oscillator Vcc is clean; use a filter, such as a RC low-pass or a ferrite inductor.

Table 12-2. RTC Routing Guidelines

Signal name	Layer	Impedance	Width (W) (mils)	Spacing (S) (mils)	Length	Figure	Notes
RTC_X1_PAD RTC_X2_PAD	microstrip	50 Ω ± 15%	4	15	0-1”	Figure 12-5	1
	stripline	50 Ω ± 10%	4.5	15			

Notes:
1. The W represents the width of signal; the S represents the spacing to any other signal.
2. After 250 mil breakout distance from SoC, keep traces separated from each other and other traces by at least 15 mils.

12.2 External Capacitors

To maintain the RTC accuracy, the external capacitor values C_1 and C_2 are chosen to provide the manufacturer specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, the socket (if used), and the package.

The following equation is used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1}) \bullet (C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = the crystal load capacitance. This value is obtained from the Crystal* Specification.
- Cin1, Cin2 = the input capacitances at the BRTCX1_PAD and BRTCX2_PAD balls of the SoC. Cin1= Cin2 = 1-2 pF.
- C_{trace1}, C_{trace2} = the trace length capacitances measured from the crystal terminals to the BRTCX1_PAD and BRTCX2_PAD balls. These values depend on the characteristics of the board material, the width of signal traces, and the length of the traces. A typical value, based on a 5-mil wide trace and a ½-ounce copper pour, is approximately equal to:

  C_{trace} = trace length • 3.8 pF/inch
- $C_{parasitic}$ = the crystal parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the Crystal part. See the Crystal Specification to obtain this value.

Ideally, C1 and C2 are chosen such that C1 = C2. Using the equation of C_{load} above, the value of C1 and C2 is calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. C2 is chosen such that C2 > C1. In this case, C1 is trimmed to obtain the 32.768 kHz.

In certain conditions, both C1 and C2 values are shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1 and C2 values are smaller than the theoretical values, the RTC oscillation frequency is higher.

The following example illustrates the use of the practical values of C1 and C2 where the theoretical values cannot guarantee the accuracy of the RTC in a low-temperature condition.

Example:

According to a required 12-pF load capacitance of a typical crystal used with the SoC, the calculated values of C1 = C2 is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C, the frequency stability of a crystal gives –23 ppm (assuming a 0 ppm at 25 °C). The RTC circuit oscillates at 32.767246 kHz instead of 32.768 kHz.

If the values of C1 and C2 are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at a higher frequency at room temperature (+23 ppm), but the circuit oscillates closer to 32.768 kHz at 0 °C. The 6.8-pF value of C1 and C2 is the **practical value**.

Note: The temperature dependency of the crystal frequency is a parabolic relationship (ppm/degree-C squared). The effect of changing the crystal frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature). See the Crystal* datasheet for more details.

12.3 RTC External Battery Connection

The RTC requires an external battery connection to maintain functionality and RAM while the SoC is not powered by the system.

Example batteries include the Duracell* 2032, 2025, or 2016 (or equivalent). These devices offer many years of operation. Batteries are rated by their storage capacity. The battery life is calculated by dividing the capacity by the average current required. If, for example, the battery storage capacity is 170 mAh (assumed usable) and the average current required is 6 µA, the battery life is at least:

- 170,000 µAh/6 µA = 28,333 h = 3.2 years

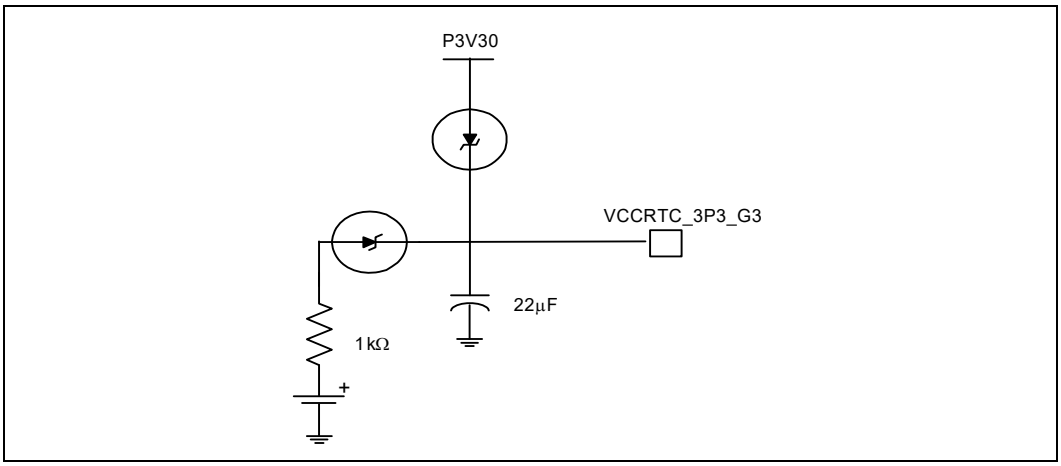
The voltage of the battery affects the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

Note: SoC RTC maximum current may draw up to 9.5uA. Please use this value to design expected battery life.

When the RTC battery is supported on the system, it must be connected to the SoC via an isolation Schottky diode circuit. The Schottky diode circuit allows the SoC RTC well to be powered by the battery when the system power is off or powered by the system power when available. To do this, the diodes are set to be reverse biased when the system power is not available.

Figure 12-6 is an example of a diode circuit used.

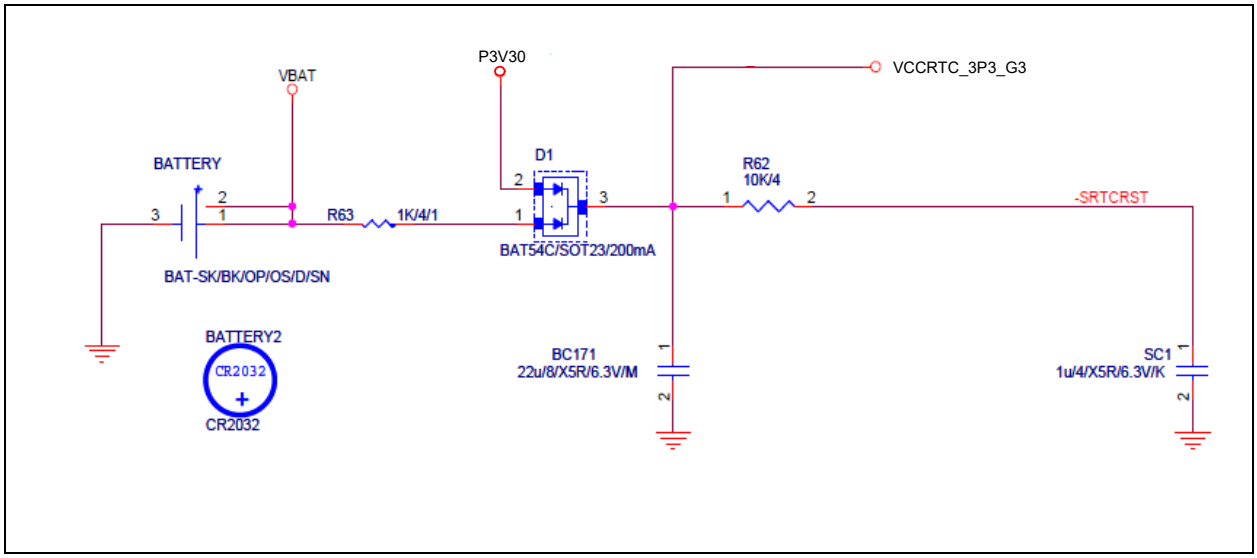
Figure 12-6. Schottky Diode Circuit to Connect RTC External Battery



A standby power supply can be designed to provide continuous power to the RTC when available. This significantly increases the RTC battery life, thereby the RTC accuracy.

12.4 Clearing Battery-Backed RTC RAM

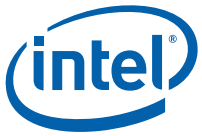
Figure 12-7. SRTCRST_N External Circuit for the SoC RTC



Clearing CMOS RAM should be done by using a jumper on RTCRST_N or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC_PWR_STS bit (D31:F0:A4h Bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this Bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor.

Note: RC values must be tuned to ensure they meet the tRTC timing of 10ms <= tRTC <= 20ms.



12.5 Real Time Clock (RTC) Design Without Battery

RTC battery is used as back up CMOS storage and other specific functionality inside the SoC when the standby power is not available. Some applications and system designs do not support RTC battery.

The platform can be operated with or without an RTC battery installed. An SoC internal circuit will detect if the battery voltage is fed into the RTC. The internal circuit will route the input into the P3V3 sustain rail. There is no additional circuitry needed on a platform level.

12.6 PMU_SUSCLK

PMU_SUSCLK is a square waveform output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTC_X1_PAD (largest voltage swing), the PMU_SUSCLK duty cycle is between 30–70%. If the duty cycle is beyond the 30–70% range, it indicates a poor oscillation signal on RTC_X1_PAD and RTC_X2_PAD.

PMU_SUSCLK can be probed directly using a normal probe (50 Ω input impedance probe) and is an appropriate signal to check the RTC frequency to determine the accuracy of the SoC RTC clock.

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13 I/O Interfaces

13.1 Miscellaneous I/O Signal

Miscellaneous I/O signal integrity require the following basic board design practices.

- Following the spacing rules provided for each signal. Violation of these rules will increase crosstalk.
- Avoid routing over voids. When routing over split planes use a decoupling capacitor between the two planes within 150 mils of the trace. At each split crossing use a 0.1 μF capacitor for decoupling.
- Ground reference all signal traces.
- Miscellaneous signals do not always follow the same rules of differential pair, intra-pin field routing. Be sure to follow the routing rules provided.

For board designs that do not follow the routing guidelines provided, simulations must be run to confirm that the design meets functional, DC, and AC specifications.

13.1.1 High Speed I/O

The high speed I/O can be configured to be PCIe, SATA, or USB 3.0.

After configured to be specific interface, please refer to the specific chapter for more detailed design guide.

Table 13-1. Signal Names and Descriptions

Signal Names	Direction	Shared	Description
HSIO_RX_DP[19:0] HSIO_RX_DN[19:0]	I, Differential	Yes	**High-Speed** I/O **Lane Read Data** - These 20 sets of differential receivers are configured by the customer as PCI Express Root Ports, SATA Ports, and/or USB 3.0 Ports.
HSIO_TX_DP[19:0] HSIO_TX_DN[19:0]	O, Differential	Yes	**High-Speed** I/O **Lane Write Data** - These 20 sets of differential drivers are configured by the customer as PCI Express Root Ports, SATA Ports, and/or USB 3.0 Ports.
HSIO_COMPREF_DP HSIO_COMPREF_DN	O, Differential	No	**High-Speed** I/O **Common Lane Compensation Pins** - The platform board must provide a 100 Ω, 1% resistor connected from the DP pin to the DN pin.
HSIO_IRCOMP	I,O	No	**HSHV_IRCOMP** - Special compensation resistor to support 3.3V shared by all of the High-Speed I/O Lane interfaces. The platform board must provide a 100-Ω, 1% resistor connected from this pin to VSS.

13.1.2 THERMTRIP_N

The THERMTRIP_N allows a minimum of 1.5:1 trace spacing ratio if the same ground reference plane is kept from the processor to the external controller.

Intel recommends THERMTRIP_N connect to THERMTRIP_N of the Gunning Transceiver Logic (GTL) device, a FPGA, a FET, or a BJT. If THERMTRIP_N is routed to an optional system receiver rather than a 1.05V compliant receiver and the interface voltage of the optional system receiver does not support a 1.05V voltage swing, then a voltage translation circuit must be used.

Note: If THERMTRIP_N is NOT used (this is not recommended since it puts the system at risk of thermal damage), then THERMTRIP_N must be terminated with a 50 Ω pull-up resistor to VCCP.

Figure 13-1. Routing Illustration THERMTRIP_N

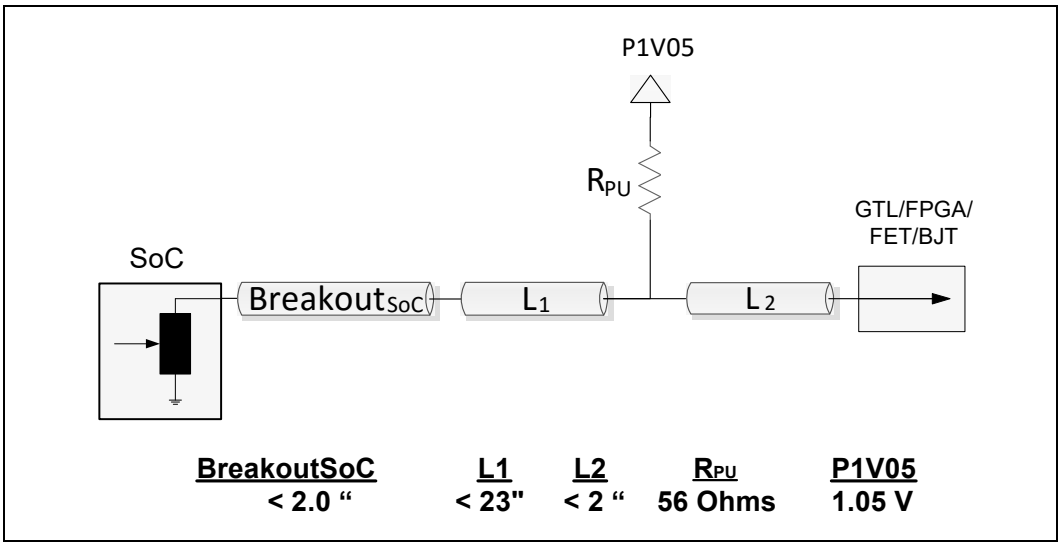


Table 13-2. THERMTRIP_N Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	23000	GND
L2	all			0	2000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. **THERMTRIP_N:** The value of R_{pu} is 56 Ω ± 5%.
2. A riser connector is added anywhere inside the L_1 length.

Table 13-3. THERMTRIP_N Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.3 PROCHOT_N

PROCHOT_N allows a system design to protect various external components (usually VRs) from overheating. A voltage translation may be necessary to reference the signal to 1.05V from some devices.

Figure 13-2. PROCHOT_N STAR Routing Illustration

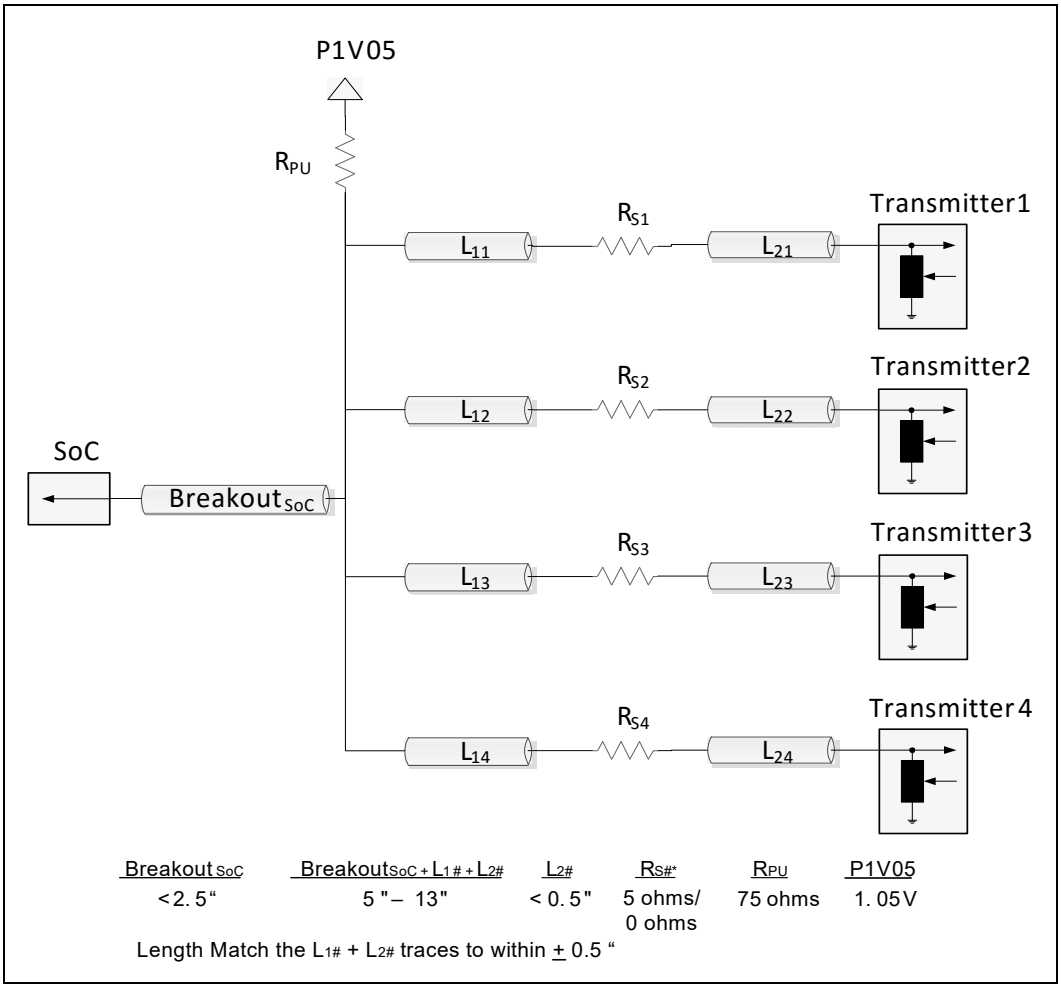


Table 13-4. PROCHOT_N STAR Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1# + L2#	all			5000	13000	
L2#	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Overshoot/undershoot at a GTL device assumes at least 1.5V/-0.5V capability.
2. The transceiver devices are GTL, FPGA, FET, or BJT so long as they adhere to the 10-Ω R_{ON} requirement.
3. A riser connector may be included anywhere inside the L1# trace.
4. Pull-ups may be added as external stubs near the SoC with a total stub length of <1”.
5. Rs#* = 5 ohms if the transmitter Ron is less than 20 ohms.

Table 13-5. PROCHOT_N Layout Recommendations for STAR Topology: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-3. PROCHOT_N Daisy Chain Routing Illustration

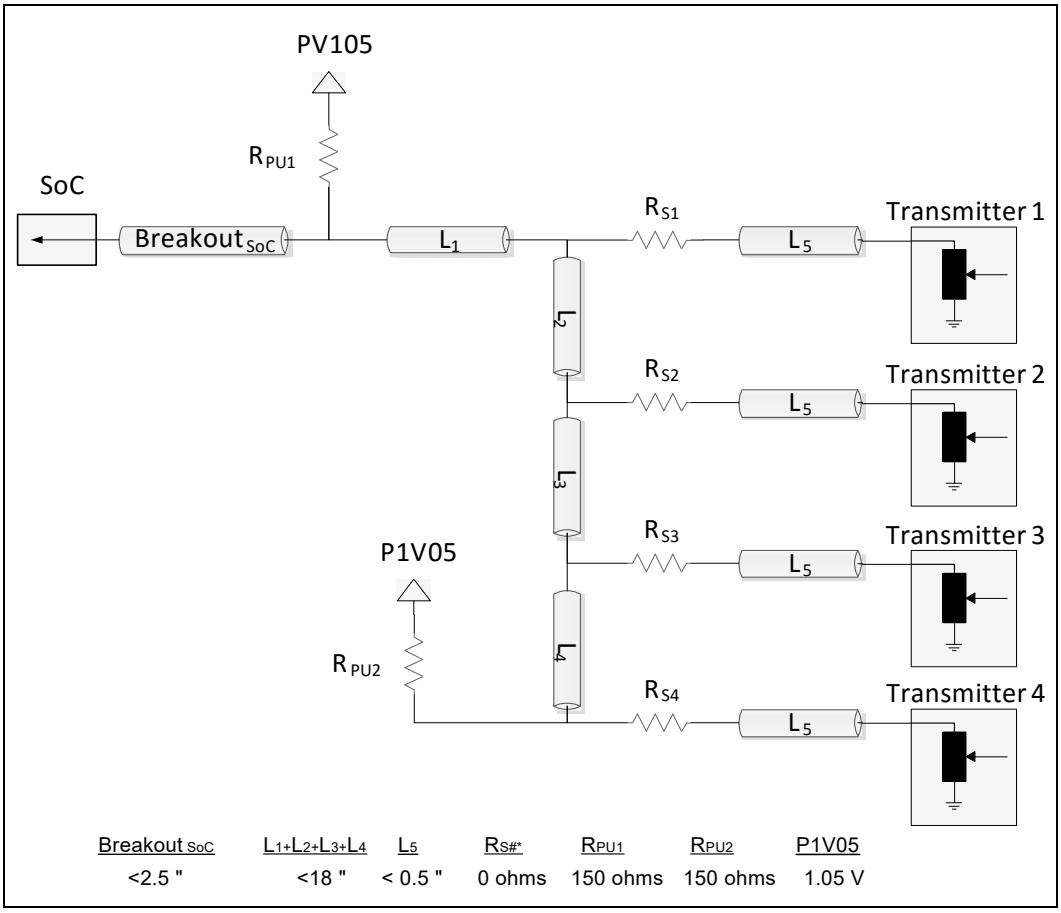


Table 13-6. PROCHOT_N Daisy Chain Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1 +L2 + L3 +L4	all			0	18000	
L5	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Overshoot/undershoot at a GTL device assumes at least 1.5V/-0.5V capability.
2. The transceiver devices are GTL, FPGA, FET, or BJT so long as they adhere to the 10-Ω R_{ON} requirement.
3. A riser connector may be included anywhere inside the L21 to L2N trace.
4. Pull-ups may be added as external stubs near the SoC with a total stub length of <1”.
5. Rs#* = 5 ohms if the transmitter Ron is less than 20 ohms.

Table 13-7. PROCHOT_N Layout Recommendations for Daisy Chain Topology: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.4 MEMHOT_N

The MEMHOT_N allows system design to protect various DIMM components from overheating. A voltage translation may be necessary to reference the signal to 1.05V for some devices.

Figure 13-4. MEMHOT_N STAR Routing Illustration

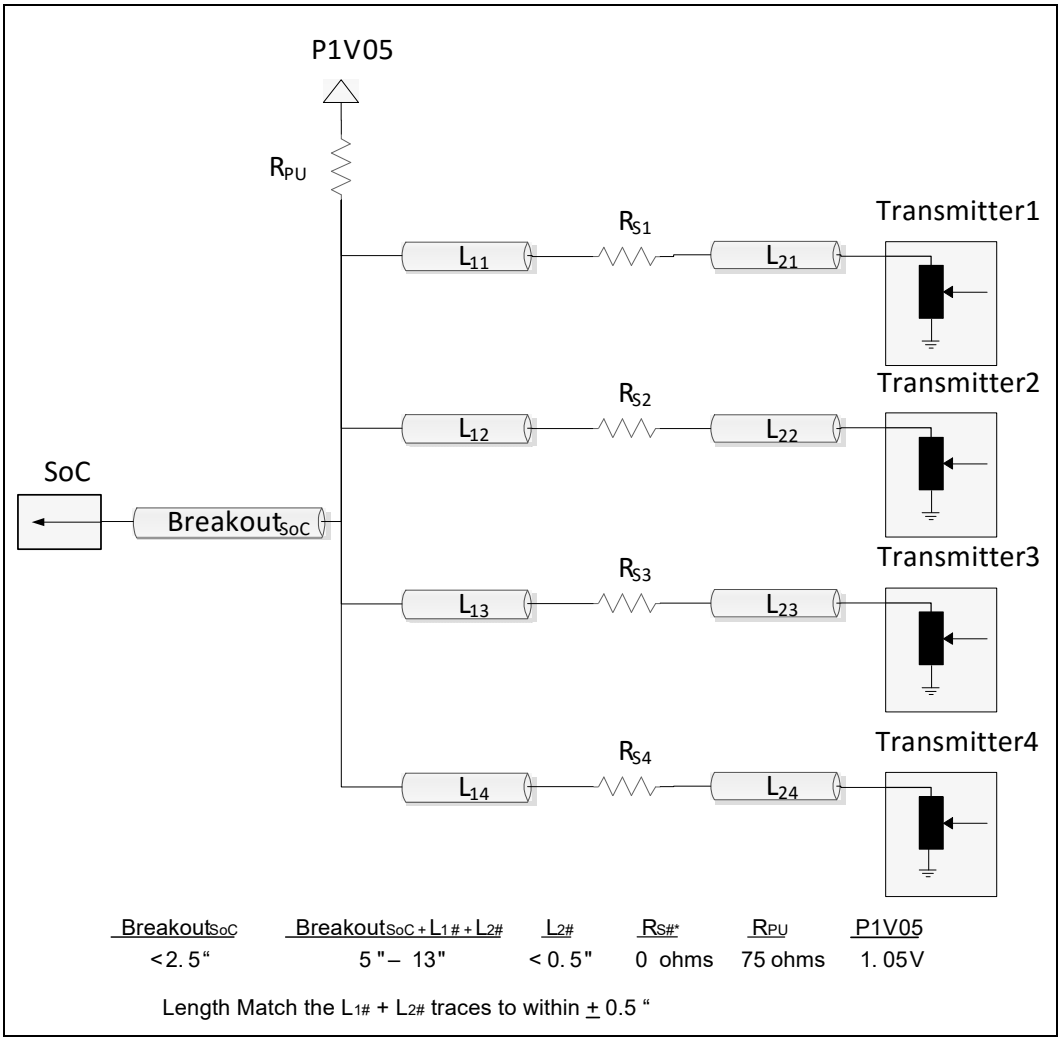


Table 13-8. MEMHOT_N STAR Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1# +L2#	all			5000	13000	
L2#	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Length match L1# + L2# branches. Match the length of every branch to ± 0.5”.
2. The resistor R_{pu} value is 75 Ω ± 5%.
3. Overshoot/undershoot at a GTL device assumes at least 1.5V/-0.5V capability.
4. The transceiver devices are GTL, FPGA, FET, or BJT so long as they adhere to the 10-Ω R_{ON} requirement.
5. A riser connector may be included anywhere inside the L1# trace.
6. Pull-ups may be added as external stubs near the SoC with a total stub length of <1”.
7. Rs#* = 5 ohms if the transmitter Ron is less than 20 ohms.

Table 13-9. MEMHOT_N Layout Recommendations for STAR Topology: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-5. MEMHOT_N Daisy Chain Routing Illustration

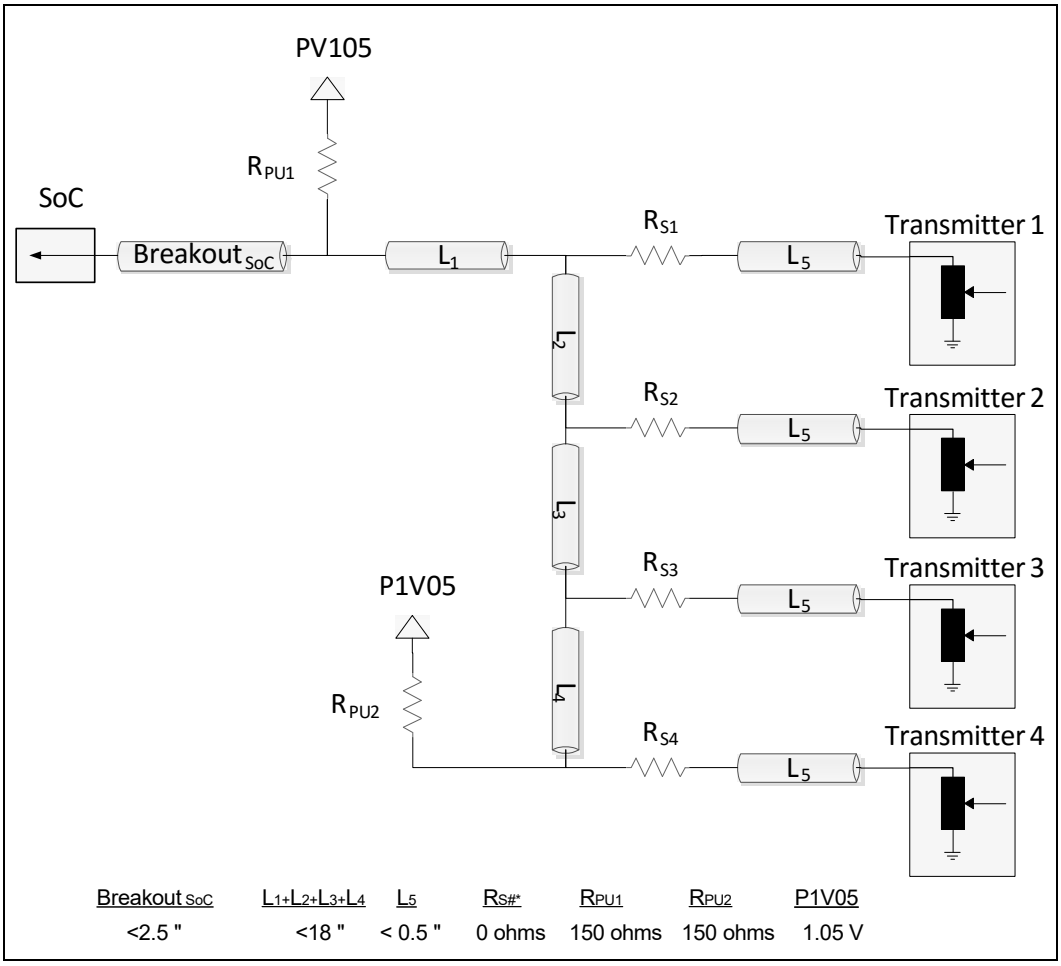


Table 13-10. MEMHOT_N Daisy Chain Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1 +L2 + L3 + L4	all			0	18000	
L5	all			0	500	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Overshoot/undershoot at a GTL device assumes at least 1.5V/-0.5V capability.
2. The transceiver devices are GTL, FPGA, FET, or BJT so long as they adhere to the 10-Ω R_{ON} requirement.
3. A riser connector may be included anywhere inside the L21 to L2N trace.
4. Rs#* = 5 ohms if the transmitter Ron is less than 20 ohms.

Pull-ups may be added as external stubs near the SoC with a total stub length of < 1”.

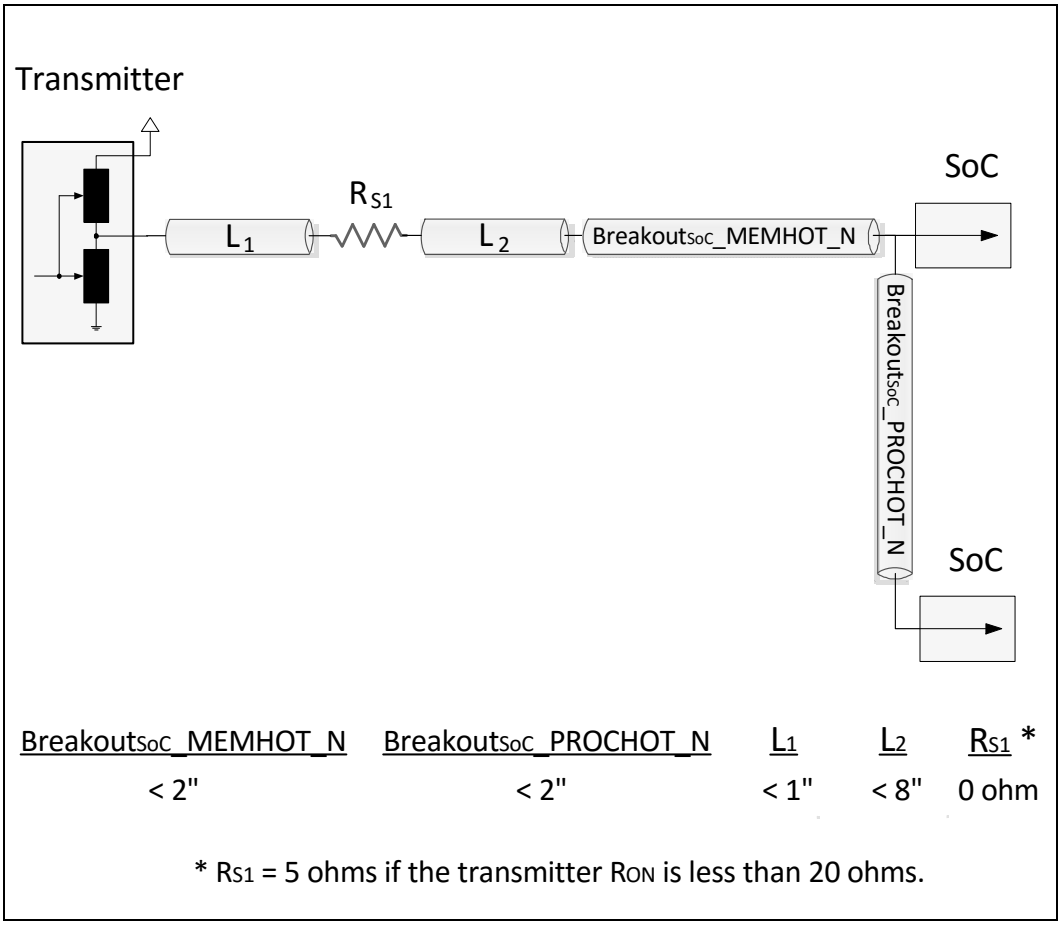
Table 13-11. MEMHOT_N Layout Recommendations for Daisy Chain Topology: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.5 PROCHOT_N and MEMHOT_N CMOS Daisy Chain for a Dual SoC System (Input Only)

For a dual SoC configured board it may be more convenient to draw a single trace to the SoCs for PROCHOT_N and MEMHOT_N. This can be done only with these signals as inputs.

Figure 13-6. PROCHOT_N and MEMHOT_N Daisy Chain (input only) Routing Illustration



$Breakout_{SoC}$_MEMHOT_N	$Breakout_{SoC}$_PROCHOT_N	L_1	L_2	R_{S1} *
< 2"	< 2"	< 1"	< 8"	0 ohm

* R_{S1} = 5 ohms if the transmitter R_{ON} is less than 20 ohms.

Table 13-12. PROCHOT_N and MEMHOT_N Daisy Chain (input only) Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$_MEMHOT_N $Breakout_{SoC}$_PROCHOT_N	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	1000	GND
L2	all			0	8000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Intel uses a hybrid stack-up with material types IT150DA for microstrip layers and IT180I for prepeg and stripline layers: 2.5 mils dielectric thickness on microstrip and 3 mils dielectric thickness on stripline.
2. Resistor tolerance: 5%.
3. Transceiver devices may be GTL, FPGA, FET or BJT.

Table 13-13. PROCHOT_N and MEMHOT_N Daisy Chain (input only) Topology: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$_MEMHOT_N $Breakout_{SoC}$_PROCHOT_N	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.6 COREPWROK

The signal for the SoC COREPWROK input pin originates in the platform power control circuitry.

Figure 13-7. COREPWROK Routing Illustration: SoC CMOS Input

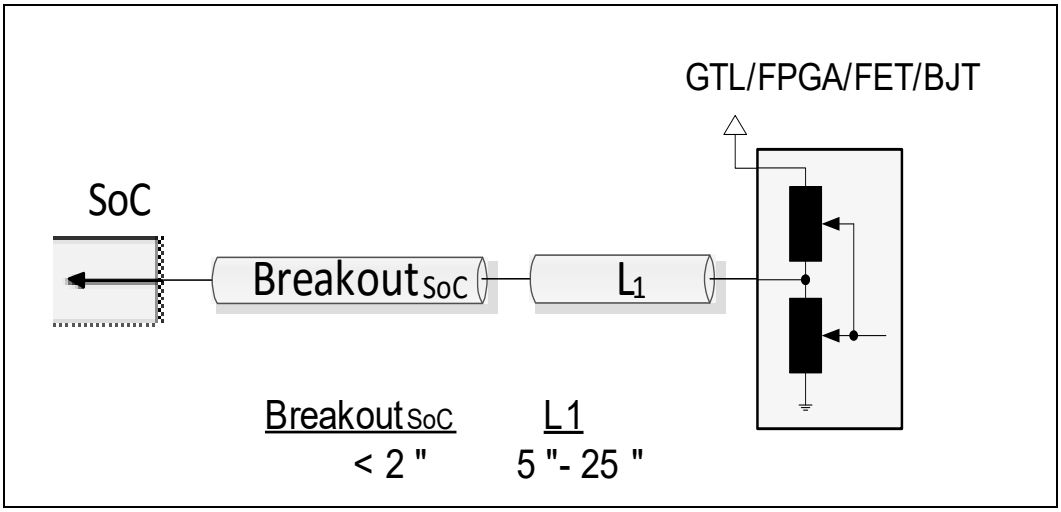


Table 13-14. COREPWROK Layout Recommendations: SoC CMOS Input

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-15. COREPWROK Layout Recommendations for CMOS Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.7 SVID_CLK, SVID_DATA, and SVID_ALERT_N

13.1.7.1 SVID_CLK Signal

The SVID clock signal is ground referenced. Do not route the SVID clock under phase nodes or high-side MOSFET nodes that generate noise. Avoid routing over voids.

Note: The SVID interface is not asynchronous. The SVID_CLK, SVID_DATA and SVID_ALERT signals encompass the synchronous SVID bus.

Figure 13-8. SVID_CLK Routing Illustration

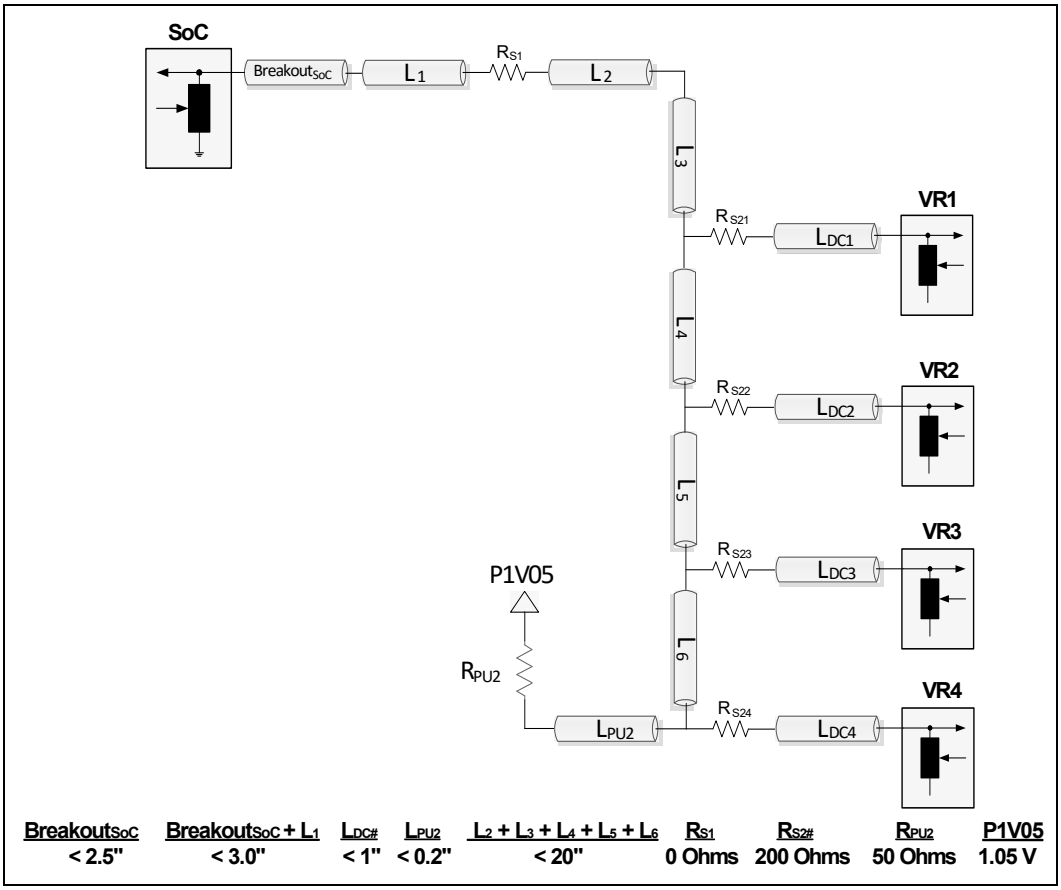


Table 13-16. SVID_CLK Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
$Breakout_{SoC}$ + L1	all			0	3000	
LDC#	all			0	1000	
LPU2	all			0	200	
L2+L3+L4+L5+L6				0	20000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	27200	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. The routing impedance is 50 Ω. ± 15%.
3. The trace-length matching requirement between SVID_CLK and SVID_DATA is < 250 mils.

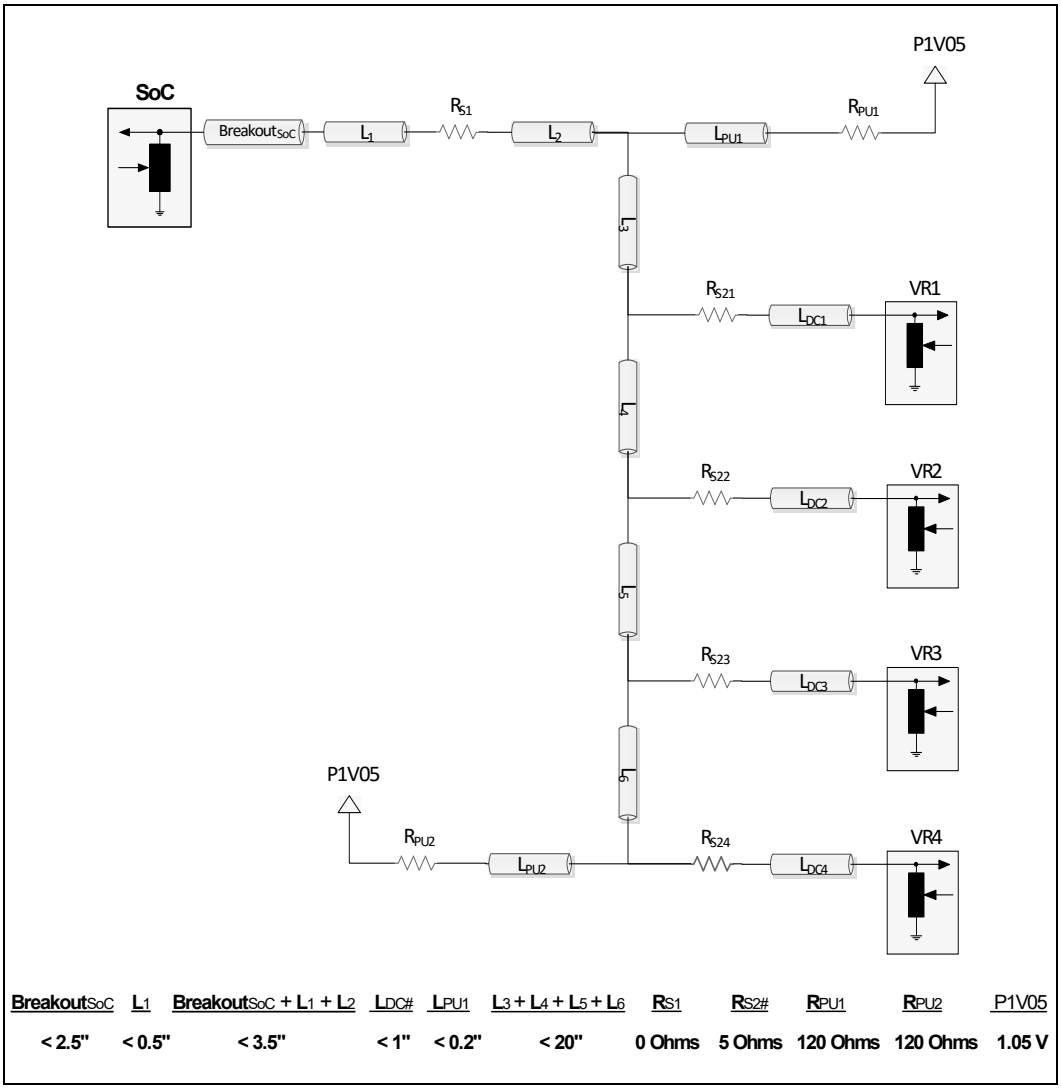
Table 13-17. SVID_CLK Layout Recommendations for CMOS Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	13.5	4	5	15	4	5	5	4	5
	stripline	12	4	5	13	4	5	4	4	5

13.1.7.2 SVID_DATA Signal

The SVID_DATA signal is ground referenced. Do not route SVID_DATA under phase nodes or high-side MOSFET nodes that generate noise. SVID_DATA is routed between the SVID_ALERT_N and the SVID_CLK lines. Avoid routing over voids.

Figure 13-9. SVID_DATA Routing Illustration



BreakoutSoC	L1	BreakoutSoC + L1 + L2	LDC#	LPU1	L3 + L4 + L5 + L6	RS1	RS2#	RPU1	RPU2	P1V05
< 2.5"	< 0.5"	< 3.5"	< 1"	< 0.2"	< 20"	0 Ohms	5 Ohms	120 Ohms	120 Ohms	1.05 V

Table 13-18. SVID_DATA Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	500	
$Breakout_{SoC}$ + L1 + L2	all			0	3500	
LDC#	all			0	1000	
LPU#	all			0	200	
L3+L4+L5+L6				0	20000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	27900	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. The routing impedance is 50 Ω. ± 15%.
3. The trace-length matching requirement between SVID_CLK and SVID_DATA is ≤ 250 mils.
4. Assuming a hybrid stack up with materials type IT150DA for microstrip layers and IT180I for prepeg and stripline layers you can use 2.5mils dielectric thickness on microstrip and 3 mils dielectric thickness on stripline. Assuming 1080 stack up material use 2.5 mils dielectric thickness for microstrip and 3 mils dielectric thickness for stripline.
5. Use a low inductance path for VIO termination voltage to termination resistors: 10 mils is the minimum trace width allowed. Place the bypass termination voltage as close as possible to the termination resistor with 10 µF and 0.1 µF capacitors to ground (bypass is required unless supplied from a full plane).

Table 13-19. SVID_Data Layout Recommendations for CMOS Input: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	13.5	4	5	15	4	5	5	4	5
	stripline	12	4	5	13	4	5	4	4	5

13.1.7.3 SVID_ALERT_N Signal

Figure 13-10. SVID_ALERT_N Routing Illustration

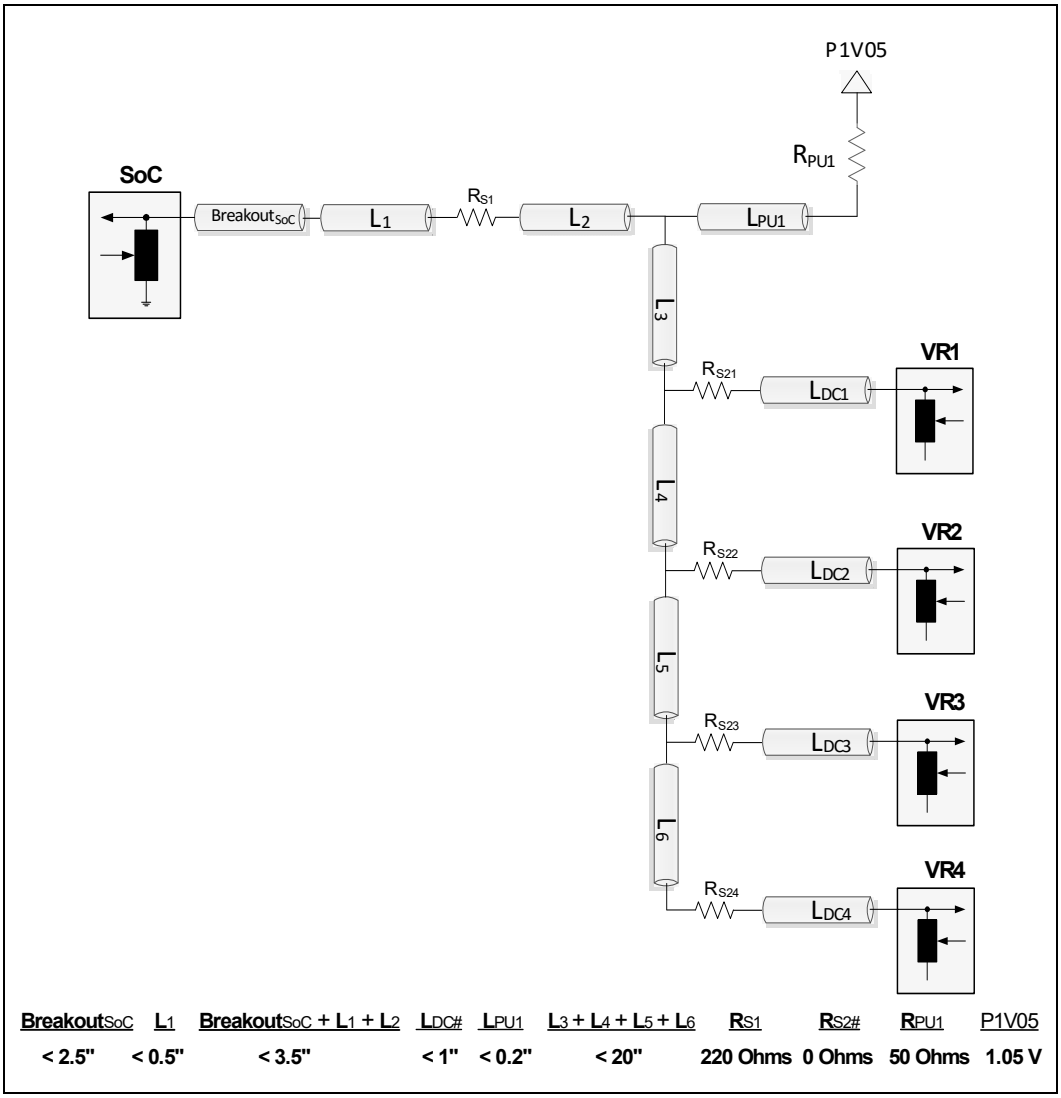


Table 13-20. SVID_ALERT_N Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2500	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	500	
$Breakout_{SoC}$ + L1 + L2	all			0	3500	
LDC#	all			0	1000	
LPU#	all			0	200	
L3+L4+L5+L6				0	20000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	27700	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. The routing impedance is 50 Ω. ± 15%.
3. The trace-length matching requirement between SVID_CLK and SVID_DATA is ≤ 250 mils.
4. Assuming a hybrid stack up with materials type IT150DA for microstrip layers and IT180I for prepeg and stripline layers you can use 2.5mils dielectric thickness on microstrip and 3 mils dielectric thickness on stripline. Assuming 1080 stack up material use 2.5 mils dielectric thickness for microstrip and 3 mils dielectric thickness for stripline.
5. Use a low inductance path for VIO termination voltage to termination resistors: 10 mils is the minimum trace width allowed. Place the bypass termination voltage as close as possible to the termination resistor with 10 µF and 0.1 µF capacitors to ground (bypass is required unless supplied from a full plane).

Table 13-21. SVID_ALERT_N Layout Recommendations for CMOS Input: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	13.5	4	5	15	4	5	5	4	5
	stripline	12	4	5	13	4	5	4	4	5

13.1.8 CPU_RESET_N, ERROR_N[0], ERROR_N[1], ERROR_N[2], MCERR_N, and IERR_N

Figure 13-11. CPU_RESET_N, ERROR_N[0], ERROR_N[1], ERROR_N[2], MCERR_N, and IERR_N Routing Illustration

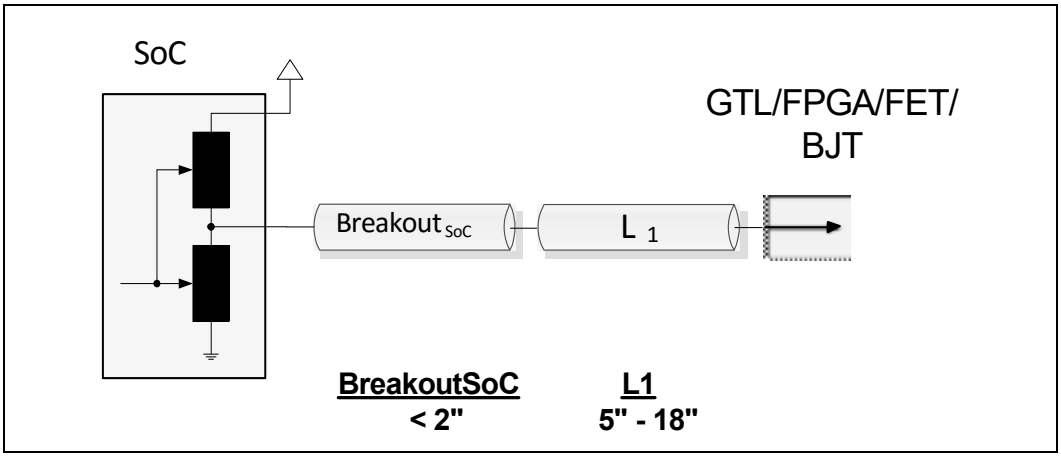


Table 13-22. CPU_RESET_N, ERROR_N[0], ERROR_N[1], ERROR_N[2], MCERR_N, and IERR_N Layout Recommendations: SoC CMOS Output

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	18000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-23. CPU_RESET_N, ERROR_N[0], ERROR_N[1], ERROR_N[2], MCERR_N, and IERR_N Layout Recommendations for CMOS Output: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.1.9 ADR_TRIGGER and ADR_COMPLETE

These asynchronous DRAM refresh signals are available if there is a battery backup application in the system. If the signals are not used for ADR nor as GPIOs, leave these pins as no connect (NC).

Note: Although the ADR_TRIGGER signal is described as Open-Drain in the EDS, no external pull-up is required on the SoC side.

Figure 13-12. ADR_TRIGGER Routing Illustration

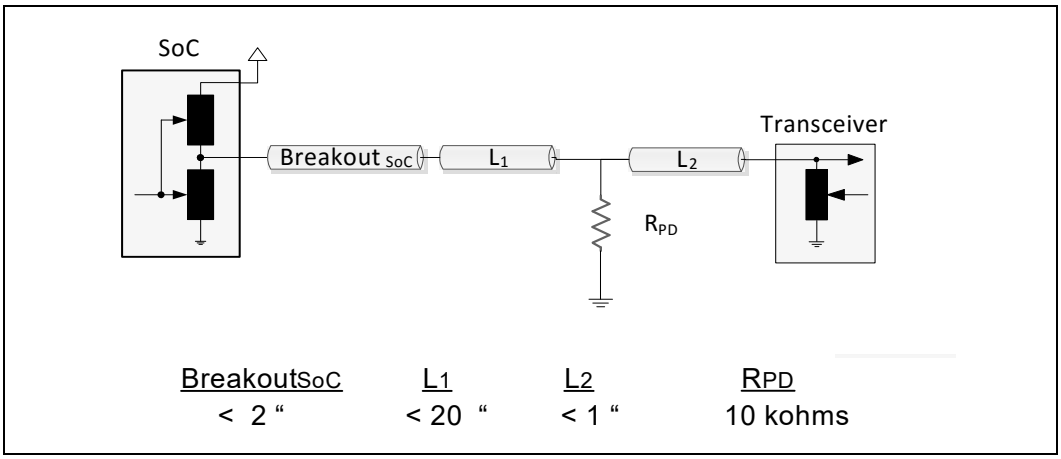


Table 13-24. ADR_TRIGGER Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all				20000	GND
L2	all			0	1000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-25. ADR_TRIGGER Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

ADR_COMPLETE is a CMOS signal configured in a point-to-point connection.

Figure 13-13. ADR_COMPLETE Routing Illustration

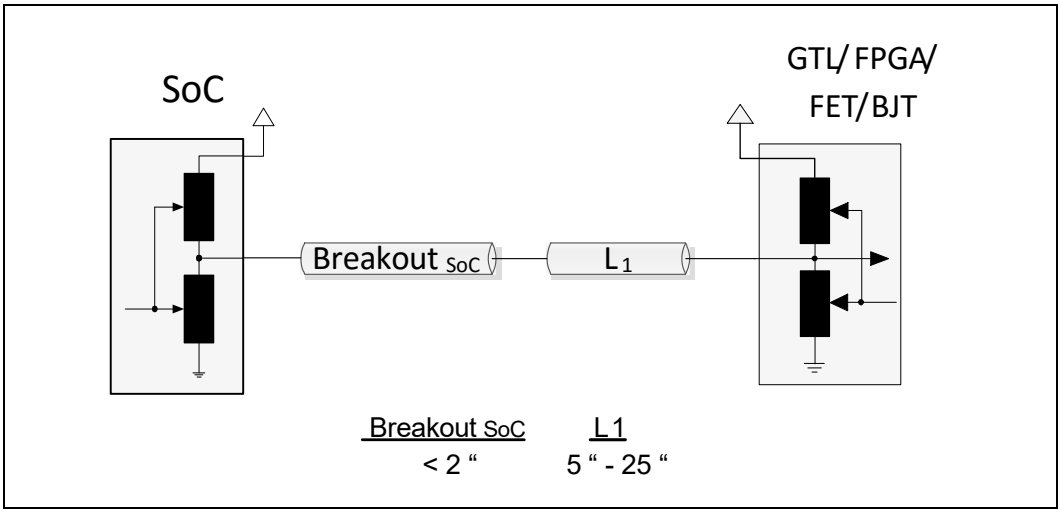


Table 13-26. ADR_COMPLETE Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. 10 layer transitions on general routing are allowed.
3. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 13-27. ADR_COMPLETE Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.2 LPC Interface

The Low Pin Count interface is not asynchronous. The LPC interface, used for connection of various legacy components, is synchronous to the LPC bus operating at a clock frequency of 24 MHz.

Note: LPC devices are assume to comply to the max and min voltages of 7.1V and -3.5V within the PCI specification. If not, then add serial resistor of 33 Ω as close as possible to the LPC device on all signals driving out of the SoC.

Table 13-28. Signal Names and Descriptions

Signal Names	Direction	Shared	Description
LPC_AD[3:0]	I,O-Tri	Yes	Multiplexed command, address, and data
LPC_FRAME_N	O	Yes	**Frame:** Indicates start of a new cycle and termination of a broken cycle. The SoC provides a 20-kΩ Pull-Up (PU) resistor on this signal pin.
LPC_CLKOUT[1:0]	O	Yes	**Clock:** Same 24-MHz clock for LPC bus interface. The SoC provides a 20-kΩ Pull-Down (PD) resistor on each of these signal pins.
LPC_CLKRUN_N	I,O-Tri	Yes	**Clock Run:** As an input, this active-low signal is generated by LPC peripherals that need the LPC_CLKOUT for a period of time beyond the four clocks guaranteed at the end of a transfer cycle. The SoC, as the central resource that generates the LPC_CLKOUT, monitors the LPC_CLKRUN_N signal to regulate its frequency for low-power operation. As an output, the SoC provides a sustained tri-state signal. When the SoC drives the LPC_CLKRUN_N signal low (asserted), it indicates the LPC_CLKOUT is operating at its normal frequency. When driven high (deasserted), the SoC indicates a stopped or very-slow clock frequency. The platform board must provide a Pull-Up (PU) resistor to sustain a logic-high voltage when the SoC and attached LPC peripherals float this tri-state bus.
LPC_SERIRQ	I,O-Tri	Yes	**Serialized IRQ:** SERIRQ is an active-low sustained tri-state bus, synchronized with the LPC_CLKOUT signal. As the Serialized Interrupt Host Controller, the SoC drives this pin low for a periods of time, high for a periods of time, and other times floats this pin. The external agents attached to this pin provide the interrupt IRQ and I/O Check indications through low and high signaling, and float this line when they do not own the bus cycle. Electrically, LPC_SERIRQ conforms with the sustained tri-state parameters defined in the PCI Local Bus Specification, Revision 3.0. The platform board must provide a Pull-Up (PU) resistor to sustain a logic-high voltage when the SoC and attached agents float this tri-state bus.
ESPI_IRCOMP	I,O	No	
Boot BIOS Strap	I	Yes	
LPC Decode Select	I	Yes	
VCC_LPC_ESPI_3P3_1P8	I (Voltage)	n/a	The platform must supply V3P30 to this voltage-supply pin.

Figure 13-14. LPC_CLK Routing Illustration: LPC_CLKOUT[1:0]

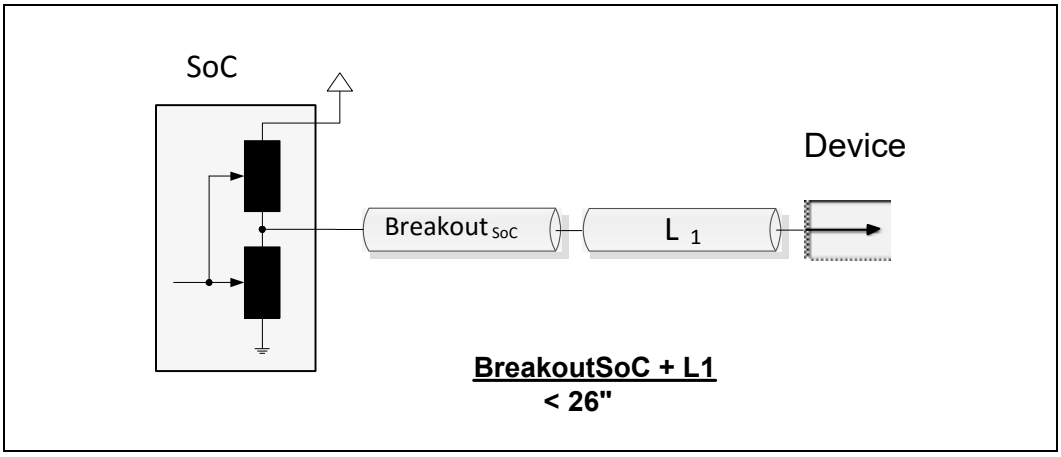


Table 13-29. LPC_CLK Layout Recommendations: LPC_CLKOUT[1:0]

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	
	stripline	3.5	52 Ω ± 10%			
$Breakout_{SoC}$ + L1	all			0	26000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	26000	
	stripline	3.87	50 Ω ± 10%			

Table 13-30. LPC_CLK Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.2.1 LPC_AD[3:0] Design Recommendations

LPC_AD[3:0] can use two topologies for layout: star or daisy chain configurations. It is recommended to leave these signals as not connected N/C when this interface is not used.

Figure 13-15. LPC_AD[3:0]: Star Routing Illustration

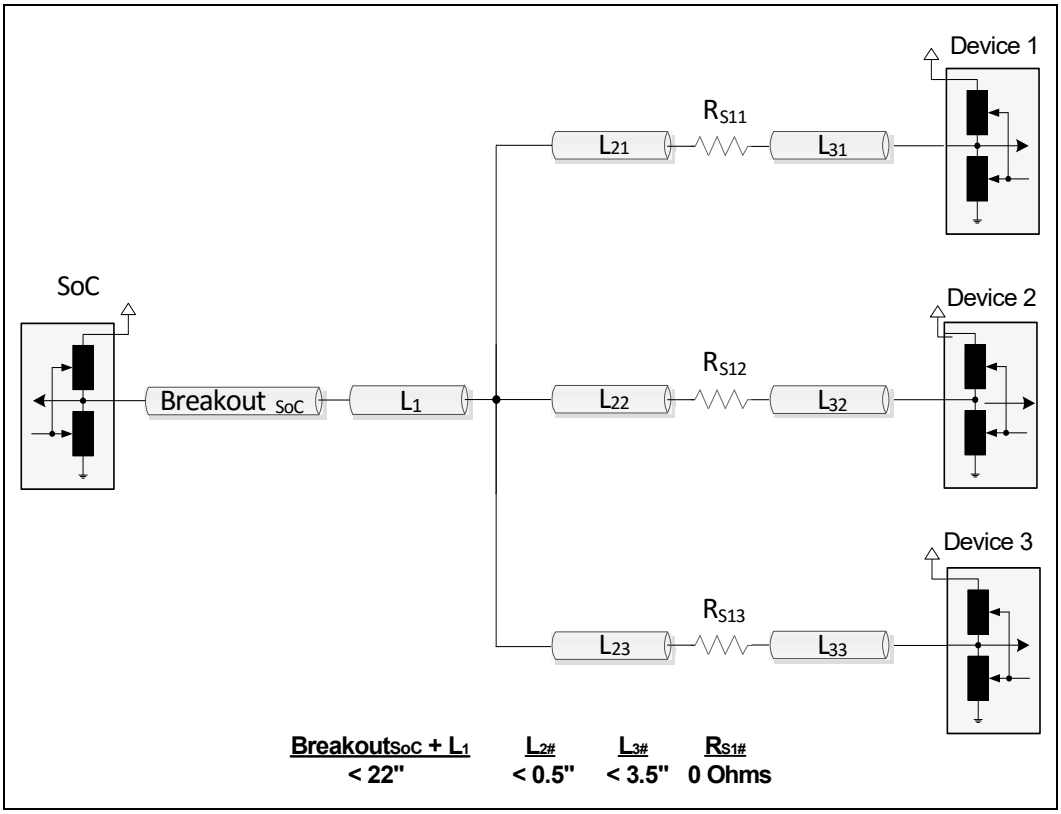


Table 13-31. LPC_AD[3:0]: Star Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%			
	stripline	3.5	52 Ω ± 10%			
$Breakout_{SoC}$ + L1	all			0	22000	GND
L2#				0	500	
L3#				0	3500	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	34000	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor tolerance: 5%.
2. 10 layer transitions on general routing are allowed.
3. Serial resistor: For LAD signals, serial resistors of 33 Ω should be added to compensate drivers with Ron of less than 50 Ω.
4. Length match relative to the LPC_CLK within 0.25".

Table 13-32. LPC_AD[3:0] Star Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-16. LPC_AD[3:0]: Daisy Chain Routing Illustration

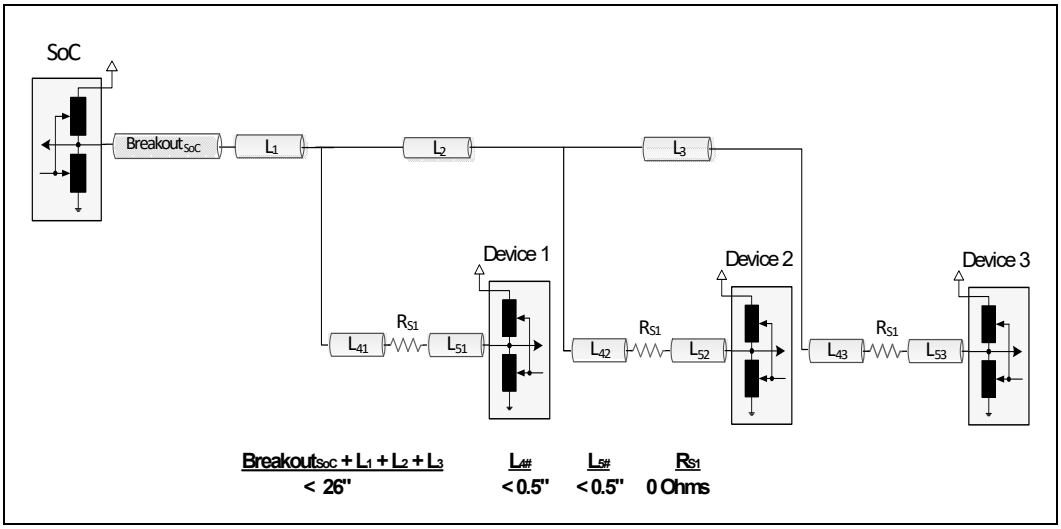


Table 13-33. LPC_AD[3:0]: Daisy Chain Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%			
	stripline	3.5	52 Ω ± 10%			
$Breakout_{SoC}$ + L1 +L2 + L3	all			0	26000	GND
L4#				0	500	GND
L5#				0	500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	29000	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor tolerance: 5%.
2. 10 layer transitions on general routing are allowed.
3. Serial resistor: For LAD signals, serial resistors of 33 Ω should be added to compensate drivers with Ron of less than 50 Ω.
4. Length match relative to the LPC_CLK within 0.25".

Table 13-34. LPC_AD[3:0] Daisy Chain Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.2.2 LPC_FRAME_N Design Recommendations

LPC_FRAME can use two topologies for layout: star or daisy chain configurations.

Figure 13-17. LPC_FRAME_N: Star Routing Illustration

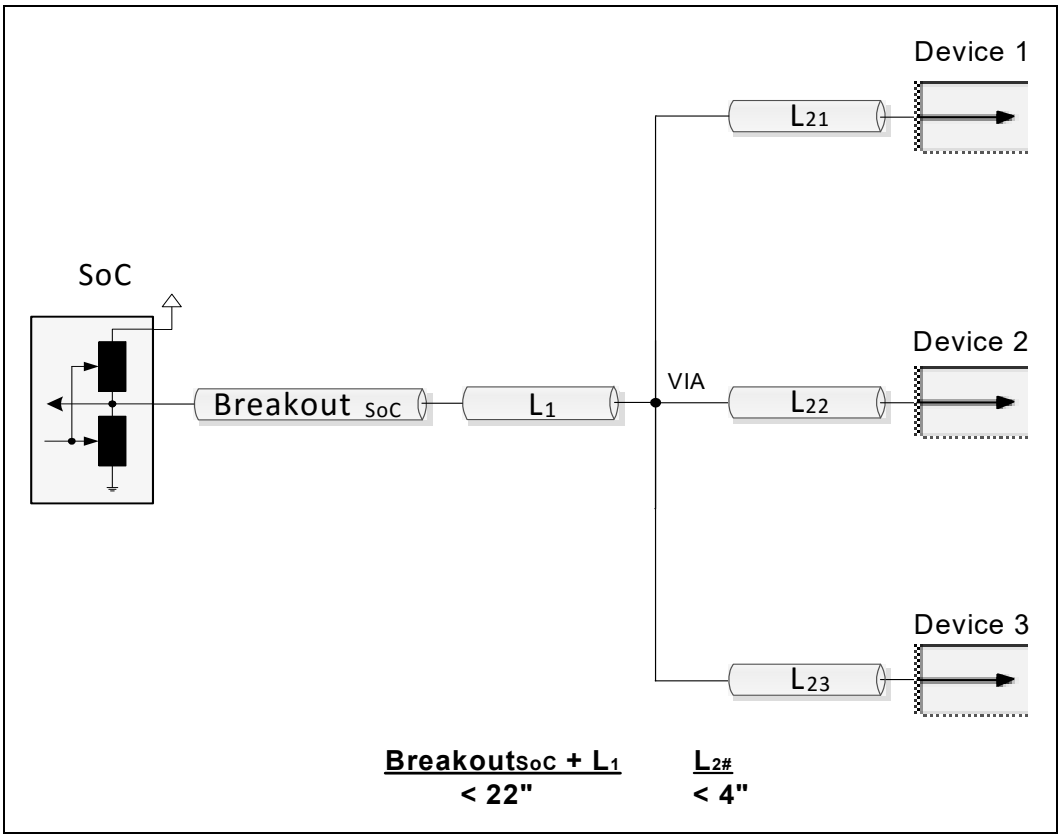


Table 13-35. LPC_FRAME_N: Star Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%			
	stripline	3.5	52 Ω ± 10%			
$Breakout_{SoC}$ + L1	all			0	22000	GND
L2#				0	4000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	34000	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor tolerance: 5%.
2. 10 layer transitions on general routing are allowed.
3. Length matching requirement between signals is < 0.25”.

Table 13-36. LPC_FRAME Star Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-18. LPC_FRAME_N: Daisy Chain Routing Illustration

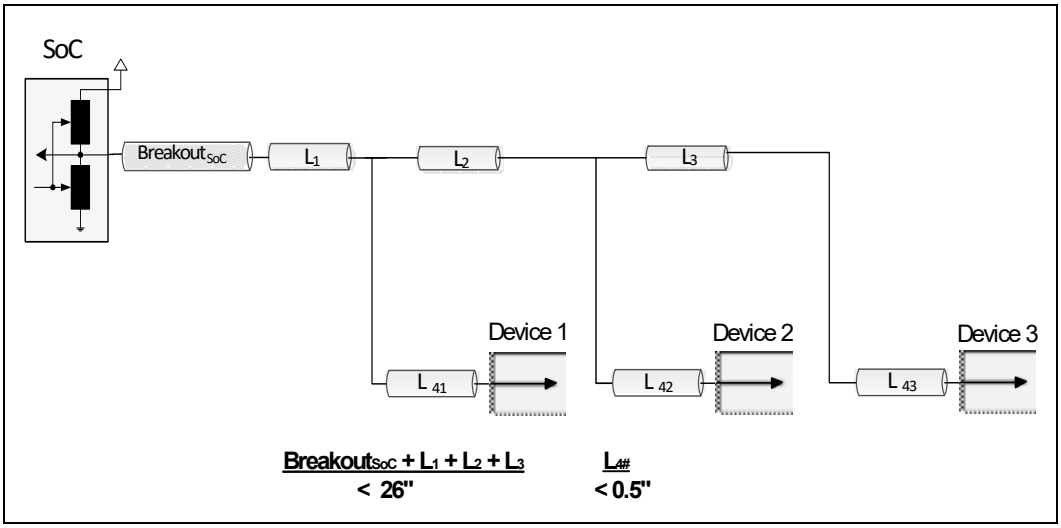


Table 13-37. LPC_FRAME_N: Daisy Chain Layout Recommendations

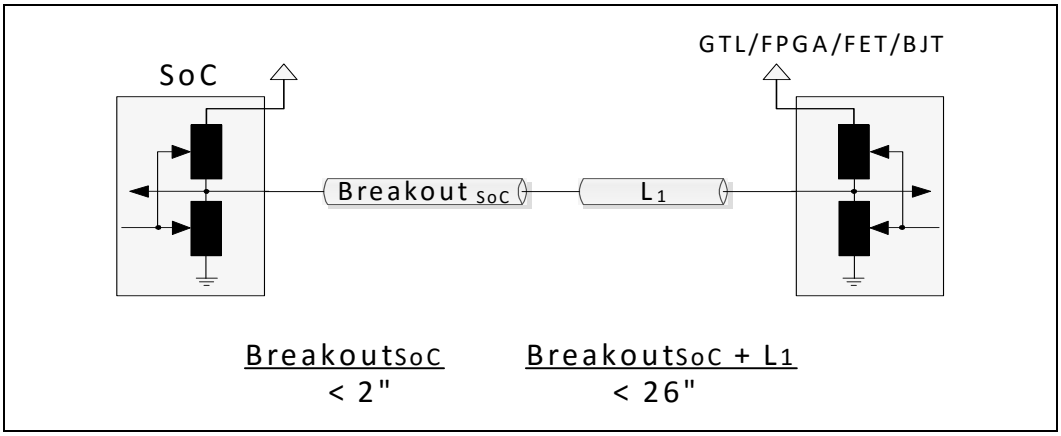
Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%			
	stripline	3.5	52 Ω ± 10%			
$Breakout_{SoC}$ + L1 +L2 + L3	all			0	26000	GND
L4#				0	500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	27500	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor tolerance: 5%.
2. 10 layer transitions on general routing are allowed.
3. Serial resistor: For LAD signals, serial resistors of 33 Ω should be added to compensate drivers with Ron of less than 50 Ω.
4. Length match relative to the LPC_CLK within 0.25".

Table 13-38. LPC_FRAME Daisy Chain Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-19. LPC_SERIRQ Routing Illustration: SoC IO CMOS Point-to-Point



Note: The LPC_SERIRQ signal can be set to a tri-state level. The pull-up resistor (not shown in Figure 13-19) can be placed as close as possible to the SoC before any branch or bifurcation of the topology to achieve this. This is required since the PU (10 kΩ - 20 kΩ) has to hold the signal from floating when the SoC releases it.

Table 13-39. LPC_SERIRQ Layout Recommendations: SoC IO CMOS Point-to-Point

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			
L1	all			0	26000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	26000	
	stripline	3.87	50 Ω ± 10%			

1. Length match relative to the LPC_CLK within 0.25".

Table 13-40. LPC_SERIRQ SOC IO CMOS Point-to-Point topology Layout Recommendations: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	15	4	5	10	4	5	5	4	5
	stripline	13	4	5	8	4	5	4	4	5

13.3 PMU Interface

For the PMU signal descriptions, see the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*.

Table 13-41. PMU Signal Descriptions

Signal	I/O Type	Technology	Rail
PMU_PLTRST_N/GPIO[87]	O	LVTTL	P3V3
PMU_PWRBTN_N/GPIO[85]	I	LVTTL	P3V3
PMU_RESETBUTTON_N/GPIO[86]	I	LVTTL	P3V3
PMU_SLP_S3_N/GPIO[83]	O	LVTTL	P3V3
PMU_SLP_S45_N/GPIO[82]	O	LVTTL	P3V3
PMU_SUSCLK/GPIO[80]	O	LVTTL	P3V3
PMU_WAKE_N/GPIO[84]	I	LVTTL	P3V3
SUS_STAT_N/ GPIO[88]	O	LVTTL	P3V3
SUSPWRDNACK/ GPIO[79]	O	LVTTL	P3V3
RSMRST_N	I	LVTTL	P3V3
ADR_COMPLETE (Section 13.1.9)	IO	LVTTL	P3V3

Figure 13-20. RSMRST_N, PMU_WAKE_N, PMU_PWRBTN_N, PMU_RESETBUTTON_N Routing Illustration: SoC CMOS Input

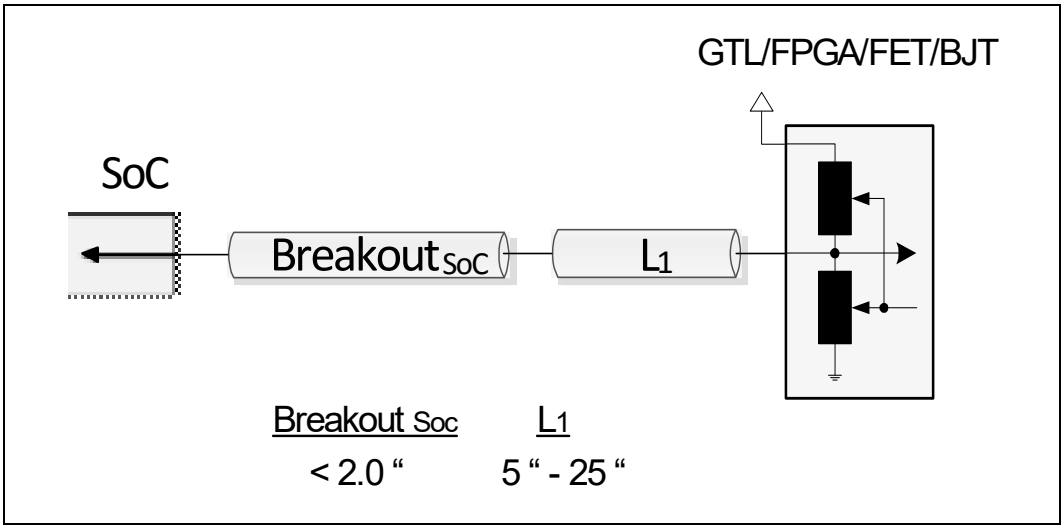


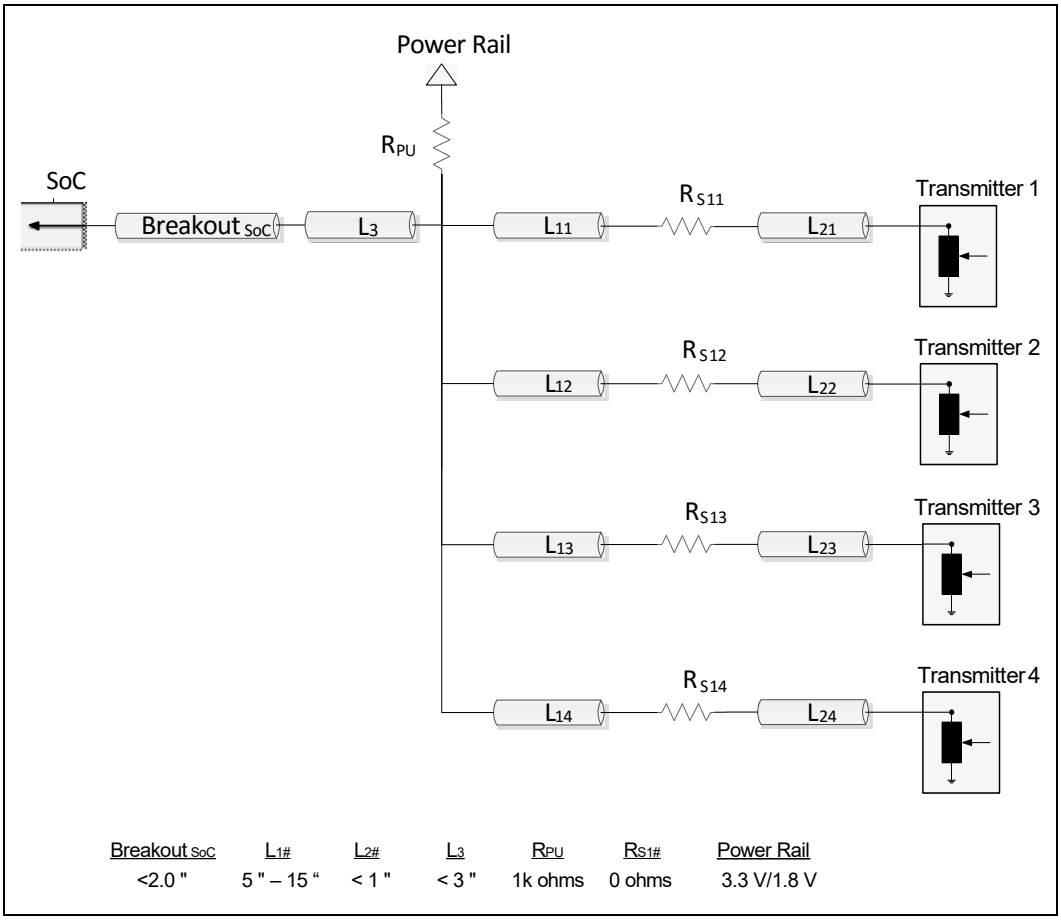
Table 13-42. RSMRST_N, PMU_WAKE_N, PMU_PWRBTN_N, PMU_RESETBUTTON_N Layout Recommendations: SoC CMOS Input

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%	0	2000	GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-43. RSMRST_N, PMU_WAKE_N, PMU_PWRBTN_N, PMU_RESETBUTTON_N Layout Recommendations for CMOS Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-21. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N Routing Illustration: SoC Star_OD Input



Note: These signals are SoC CMOS input signals. The OD signals are driven from the Transmitters. The power rail and pull up resistor should be chosen based on the Transmitter requirement. Refer to the device data sheet. A voltage translator may be needed to tie the signal to the right level for the SoC.

Table 13-44. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N SoC Star_OD Input Layout Recommendations

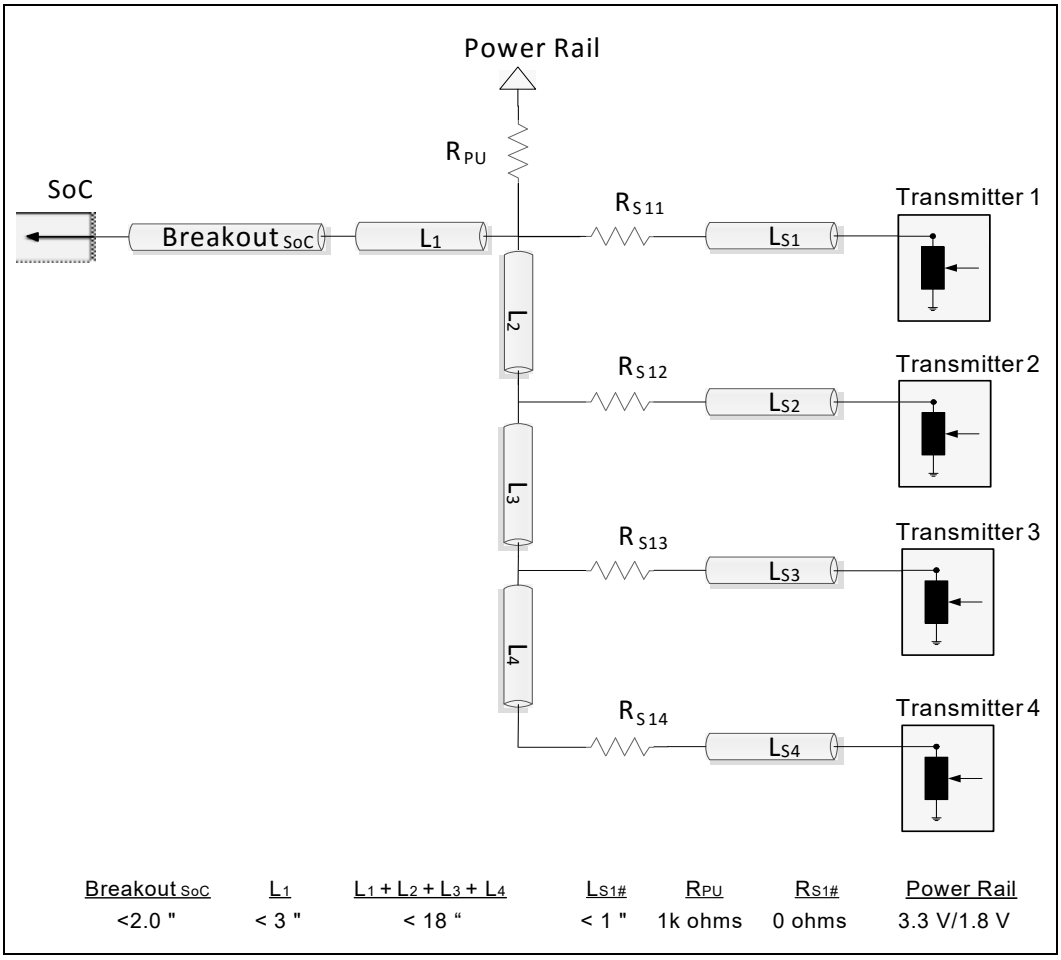
Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1#	all			5000	15000	
L2#	all			0	1000	
L3				0	3000	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. Transceiver devices may be GTL, FPGA, FET, or BJT.

Table 13-45. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N Layout Recommendations for STAR, Daisy Chain, and CMOS Topologies: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-22. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N Routing Illustration: SoC OD Daisy Chain Input



Note: These signals are SoC CMOS input signals. The OD signals are driven from the Transmitters. The power rail and pull up resistor should be chosen based on the Transmitter requirement. Refer to the device data sheet. A voltage translator may be needed to tie the signal to the right level for the SoC.

Table 13-46. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N: SoC OD Daisy Chain Input Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	
	stripline	3.5	52 Ω ± 10%			
L1	all			0	3000	GND
L1+L2+L3+L4				0	18000	GND
L5#				0	1000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-47. PMU_PWRBTN_N, PMU_RESETBUTTON_N, and PMU_WAKE_N Layout Recommendations for SoC OD Daisy Chain Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-23. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Routing Illustration

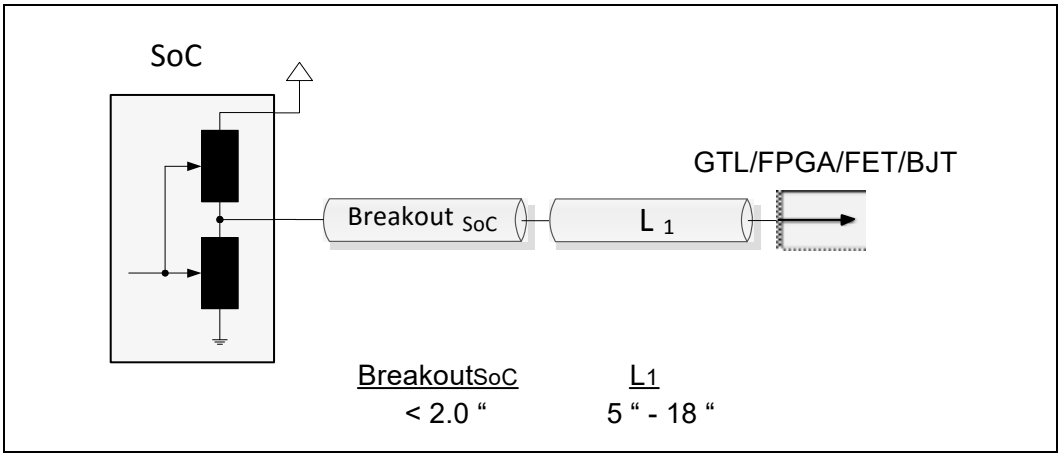


Table 13-48. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Layout Recommendations: SoC CMOS Output

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	18000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%			
	stripline	3.87	50 Ω ± 10%			

Table 13-49. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Layout Recommendations for CMOS Output: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-24. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Routing Illustration: SoC Star CMOS Output

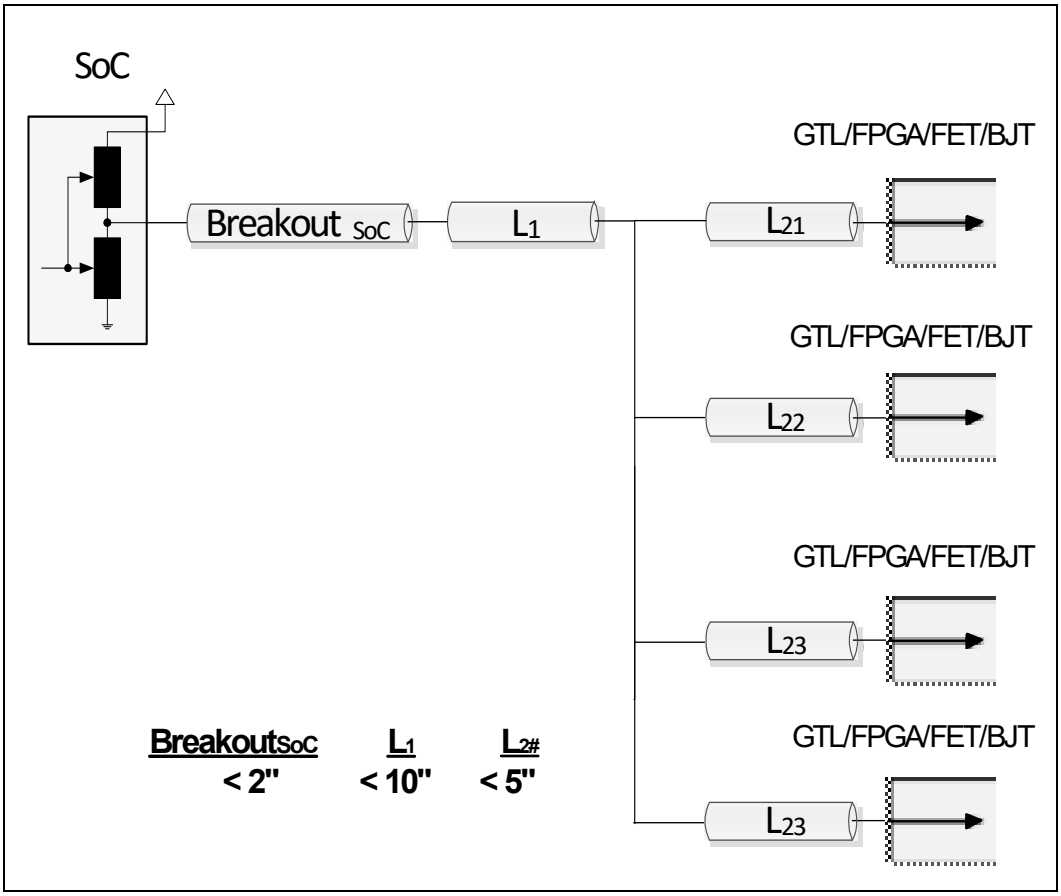


Table 13-50. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N SoC Star_OD Output Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	
L2#	all			0	5000	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

1. Resistor tolerance is ± 5%.
2. Transceiver devices may be GTL, FPGA, FET, or BJT.

Table 13-51. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Layout Recommendations for STAR, Daisy Chain, and CMOS Topologies: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-25. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N Routing Illustration: SoC Daisy Chain CMOS Output

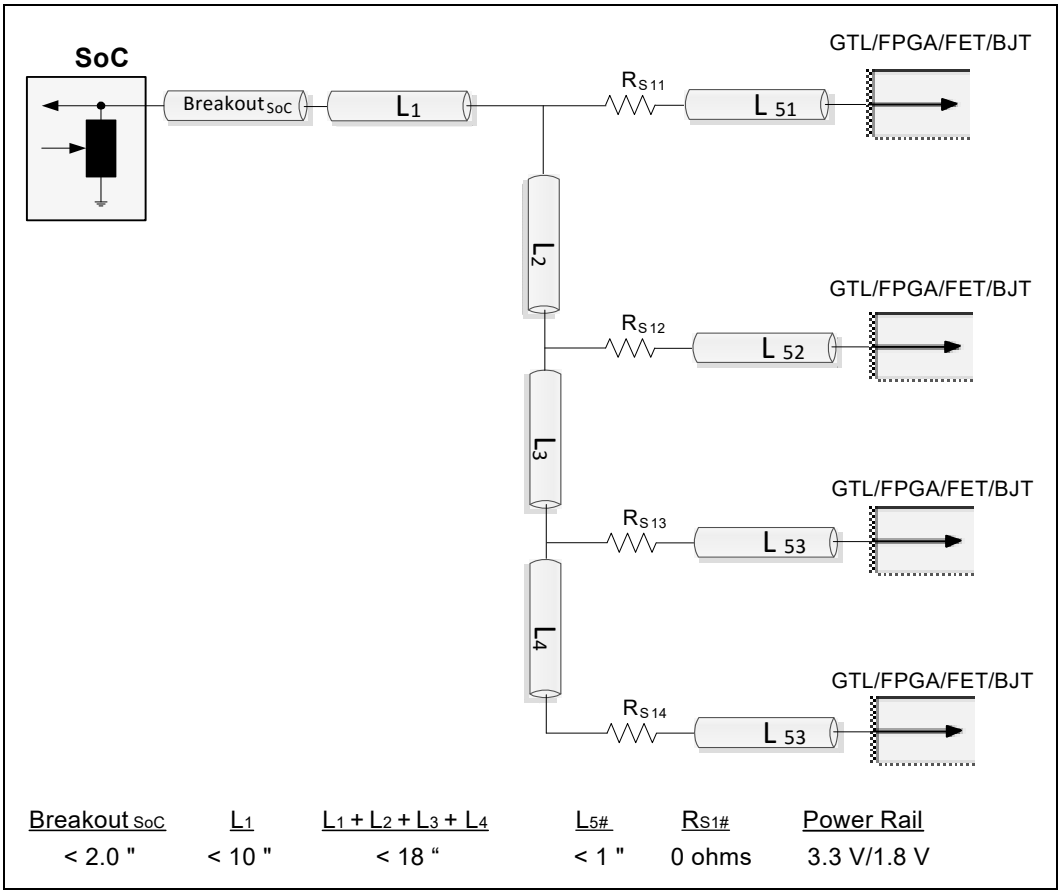


Table 13-52. SUSPWRDNACK, PMU_SUSCLK, PMU_SLP_S45_N, PMU_SLP_S3_N, PMU_PLTRST_N, and SUS_STAT_N SoC Daisy Chain_OD Output Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	
L1+L2+L3+L4	all			0	18000	
L5	all			0	1000	
Entire Signal	microstrip	4.1	50 Ω ± 15%			GND
	stripline	3.87	50 Ω ± 10%			GND

13.4 UART Interface

There are four high-speed UART interfaces in the SoC. The UART interfaces support a baud rate from 300 bps to 3.6864 Mbps. Only a maximum of three active UART interfaces allowed at any given time.

Table 13-53. UART Signals

Signal Name	Direction	Description
UART0		
UART0_RXD	I	UART0 Receive Data: Active-high input
UART0_TXD	O	UART0 Transmit Data: Active-high output
UART0_CTS	I	UART0 Clear to Send: Active-high input
UART0_RTS	O	UART0 Request to Send: Active-high output
UART1		
UART1_RXD	I	UART1 Receive Data: Active-high input
UART1_TXD	O	UART1 Transmit Data: Active-high output
UART1_CTS	I	UART1 Clear to Send: Active-high input
UART1_RTS	O	UART1 Request to Send: Active-high output
UART2		
UART2_RXD	I	UART2 Receive Data: Active-high input
UART2_TXD	O	UART2 Transmit Data: Active-high output
UART2_CTS	I	UART2 Clear to Send: Active-high input
UART2_RTS	O	UART2 Request to Send: Active-high output
UART Innovation Engine		
UART_IE_RXD	I	UART_IE Receive Data: Active-high input
UART_IE_TXD	O	UART_IE Transmit Data: Active-high output
UART_IE_CTS	I	UART_IE Clear to Send: Active-high input
UART_IE_RTS	O	UART_IE Request to Send: Active-high output

Note: All Innovation Engine (IE) related material detail can be found in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*.

Figure 13-26. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Routing Illustration: SoC CMOS Input

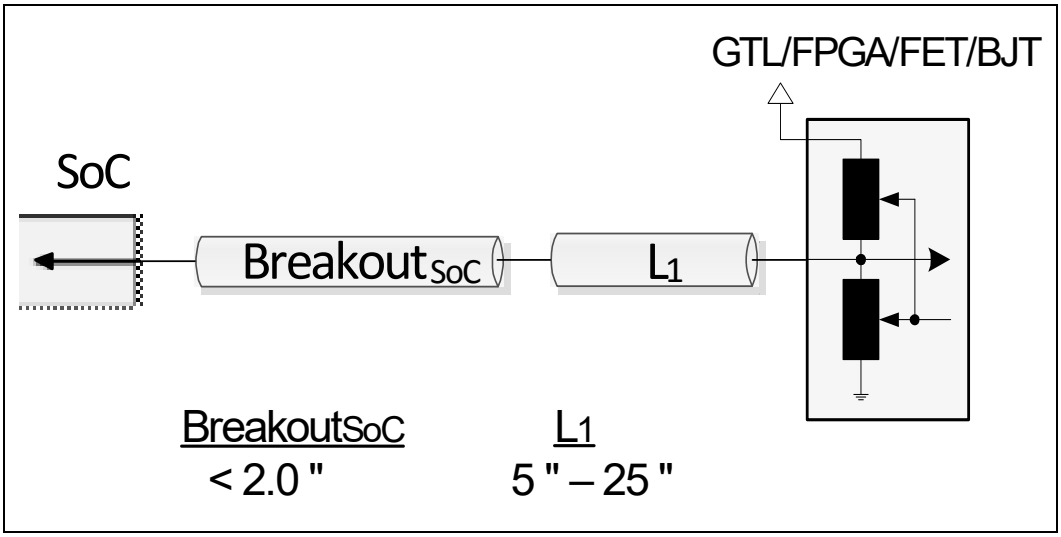


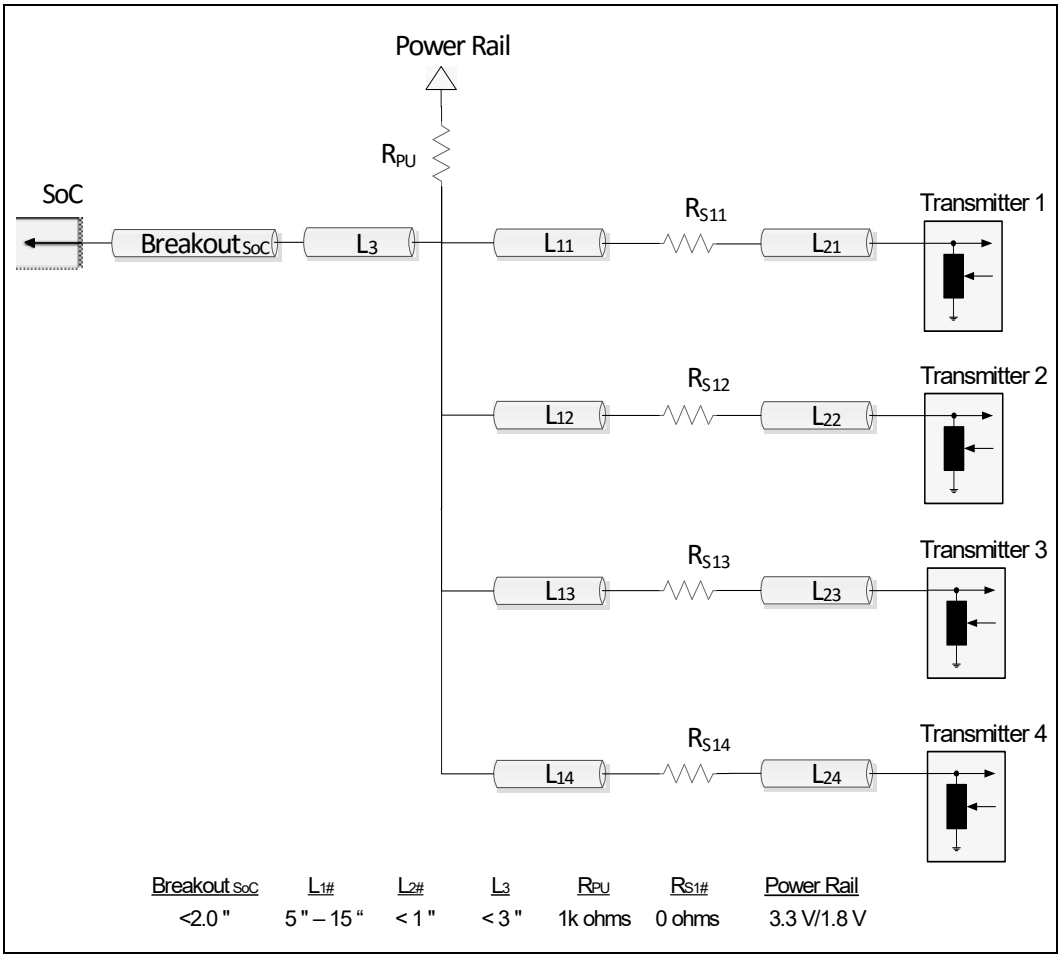
Table 13-54. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Layout Recommendations: SoC CMOS Input

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	7000	27000	
	stripline	3.87	50 Ω ± 10%			

Table 13-55. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Layout Recommendations for CMOS Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-27. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Routing Illustration: SoC Star OD Input



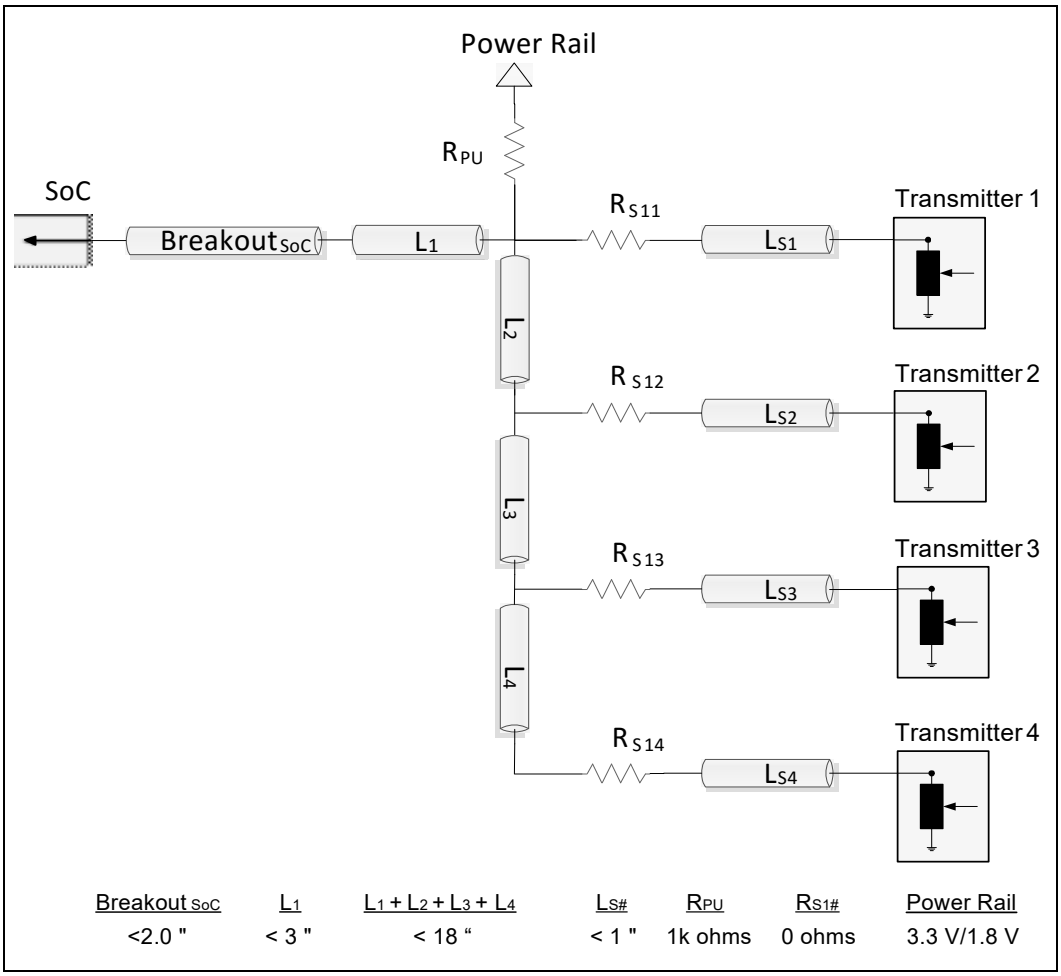
Note: These signals are SoC CMOS input signals. The OD signals are driven from the Transmitters. The power rail and pull up resistor should be chosen based on the Transmitter requirement. Refer to the device data sheet. A voltage translator may be needed to tie the signal to the right level for the SoC.

Table 13-56. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS SoC Star_OD Input Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1#	all			5000	15000	
L2#	all			0	1000	
L3				0	3000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	20000	68000	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. Transceiver devices may be GTL, FPGA, FET, or BJT.

Figure 13-28. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Routing Illustration: SoC Daisy Chain OD Input



Note: These signals are SoC CMOS input signals. The OD signals are driven from the Transmitters. The power rail and pull up resistor should be chosen based on the Transmitter requirement. Refer to the device data sheet. A voltage translator may be needed to tie the signal to the right level for the SoC.

Table 13-57. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS SoC Daisy Chain OD Input Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	3000	
L1+L2+L3+L4	all			0	18000	
LS#				0	1000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	24000	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. Transceiver devices may be GTL, FPGA, FET, or BJT.

Note: Rs1# will be 5 Ω if the length of the trace from Rpu to the active transmitter is less than 5 inches and the transmitter Ron is less than 20 Ω.

Table 13-58. UART#_RXD, UART#_TXD, UART#_CTS, UART_IE_RXD, UART_IE_CTS Layout Recommendations for STAR, Daisy Chain, and CMOS Topologies: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-29. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Routing Illustration

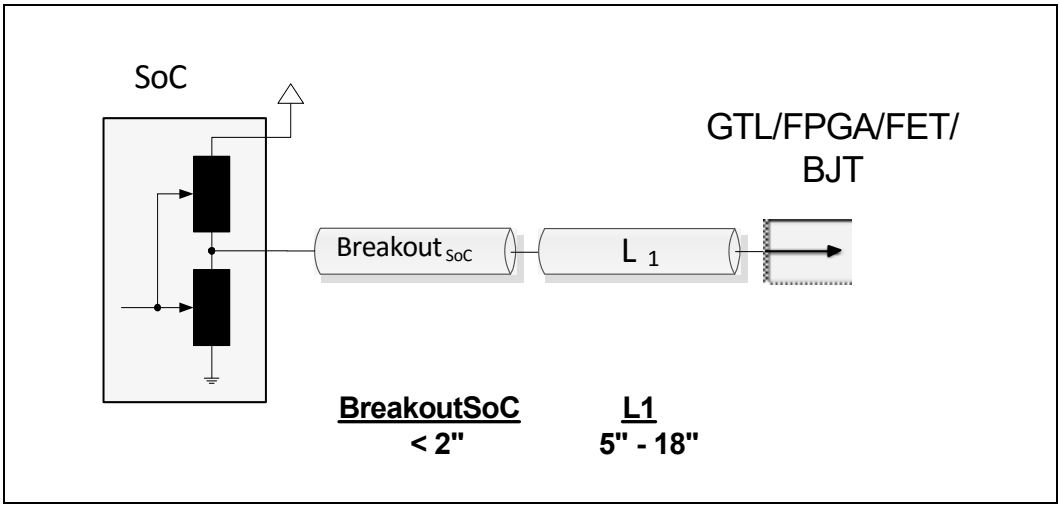


Table 13-59. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Layout Recommendations: SoC CMOS Output

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			5000	18000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	5000	20000	
	stripline	3.87	50 Ω ± 10%			

Table 13-60. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Layout Recommendations for CMOS Output: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-30. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Routing Illustration: SoC Star CMOS Output

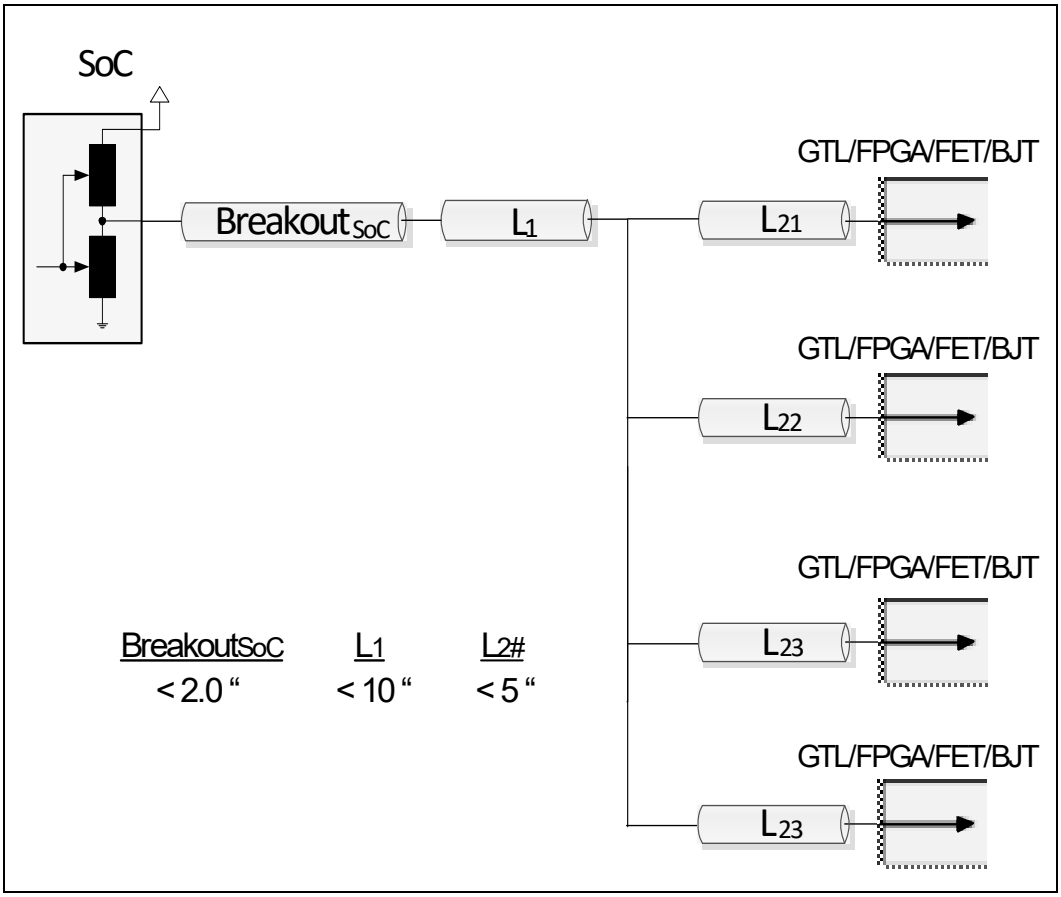


Table 13-61. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS SoC Star CMOS Output Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	
L2#	all			0	5000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	32000	GND
	stripline	3.87	50 Ω ± 10%			GND

Notes:
1. Resistor tolerance is ± 5%.
2. Transceiver devices may be GTL, FPGA, FET, or BJT.

Table 13-62. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Layout Recommendations for STAR, Daisy Chain, and CMOS Topologies: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-31. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS Routing Illustration: SoC Daisy Chain CMOS Output

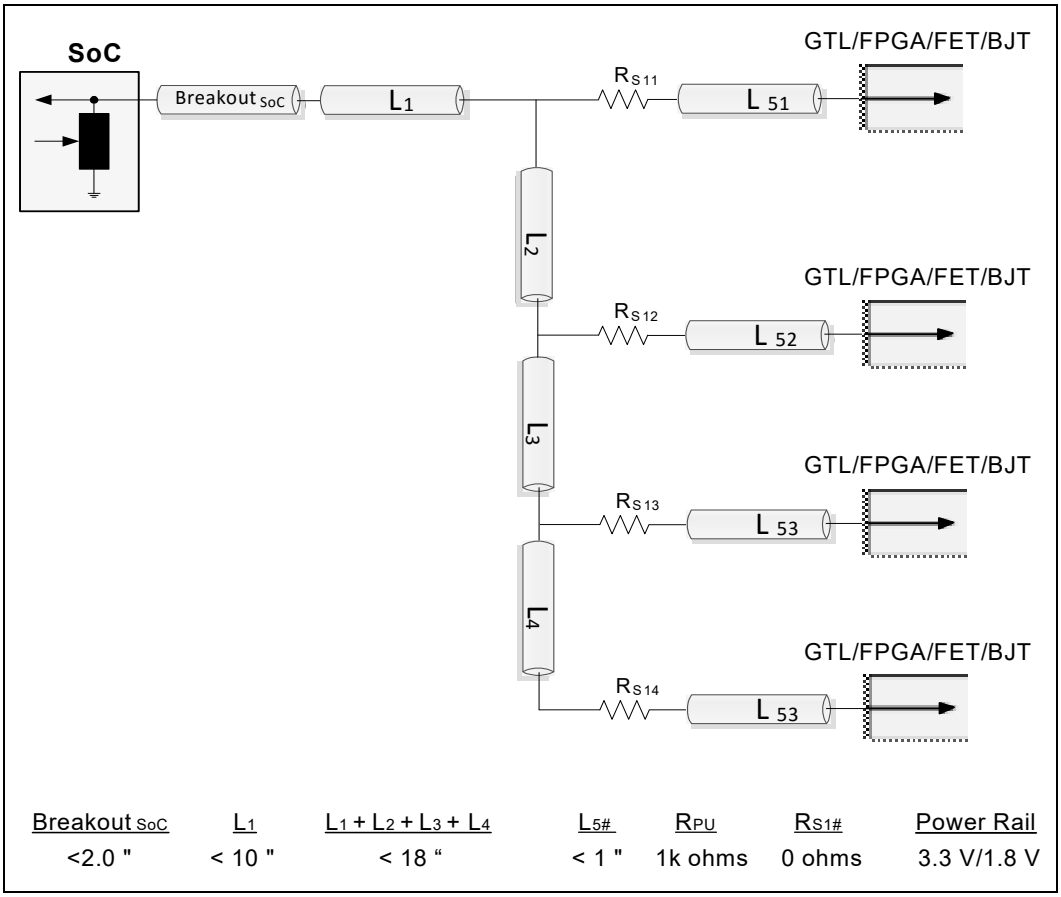


Table 13-63. UART#_RXD, UART#_TXD, UART#_RTS, UART_IE_TXD, UART_IE_RTS SoC Daisy Chain CMOS Output Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	
L1+L2+L3+L4	all			0	18000	
L5	all			0	1000	
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	24000	GND
	stripline	3.87	50 Ω ± 10%			GND

13.4.1 HSHV_IRCOMP Signal

The HSHV_IRCOMP is a special compensation resistor to support 3.3V shared by all of the High-Speed I/O (HSIO) Lane interfaces: PCIe, SATA, and USB. The platform board must provide a 100 Ω, 1% resistor connected from this pin to VSS.

Figure 13-32. HSHV_IRCOMP circuit

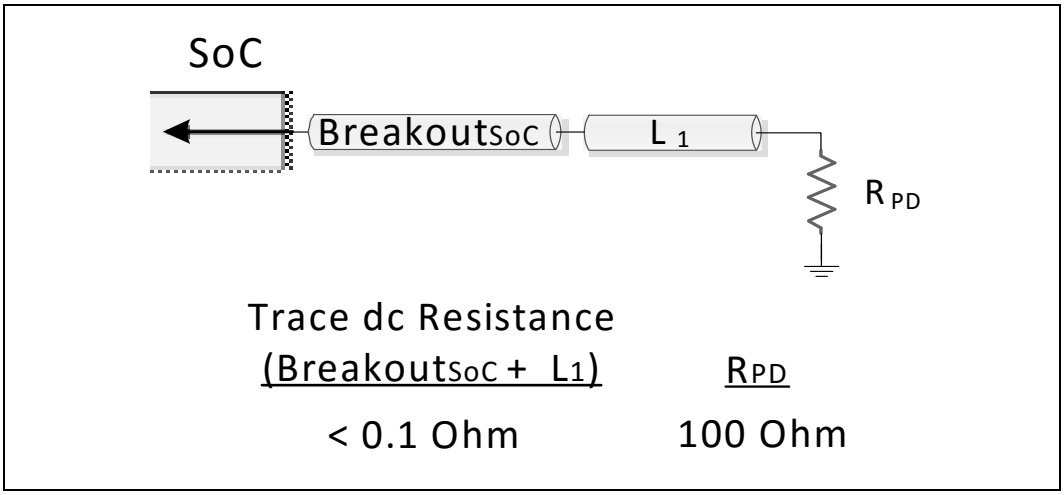


Table 13-64. HSHV_IRCOMP Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	P3V3 and P1V8 Aggressors			P1V0 Aggressors			Static_signals			
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Dist. to Plane edge
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5	
	stripline	4	4	5	4	4	5	4	4	5	
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5	5
	stripline	8	4	5	13	4	5	4	4	5	5

13.4.2 Fan Control Signals

Figure 13-33. FAN_TACH[3:0] Routing Illustration: SoC CMOS Input

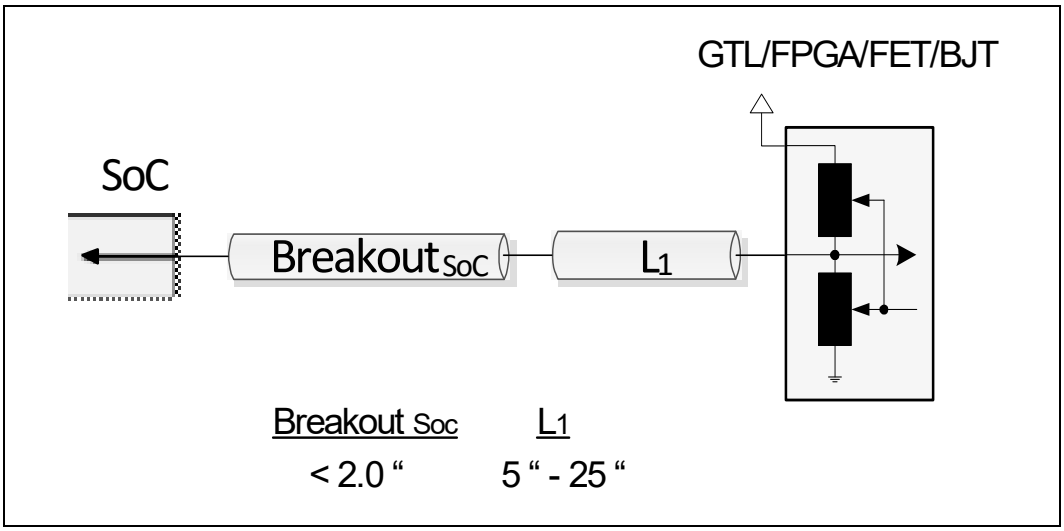


Table 13-65. FAN_TACH[3:0] Layout Recommendations: SoC CMOS Input

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%	0	2000	GND
L1	all			5000	25000	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	7000	27000	
	stripline	3.87	50 Ω ± 10%			

Table 13-66. FAN_TACH[3:0] Layout Recommendations for CMOS Input: Trace Spacing (mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

Figure 13-34. FAN_PWM [3:0] Routing Illustration: SoC Open Drain Output

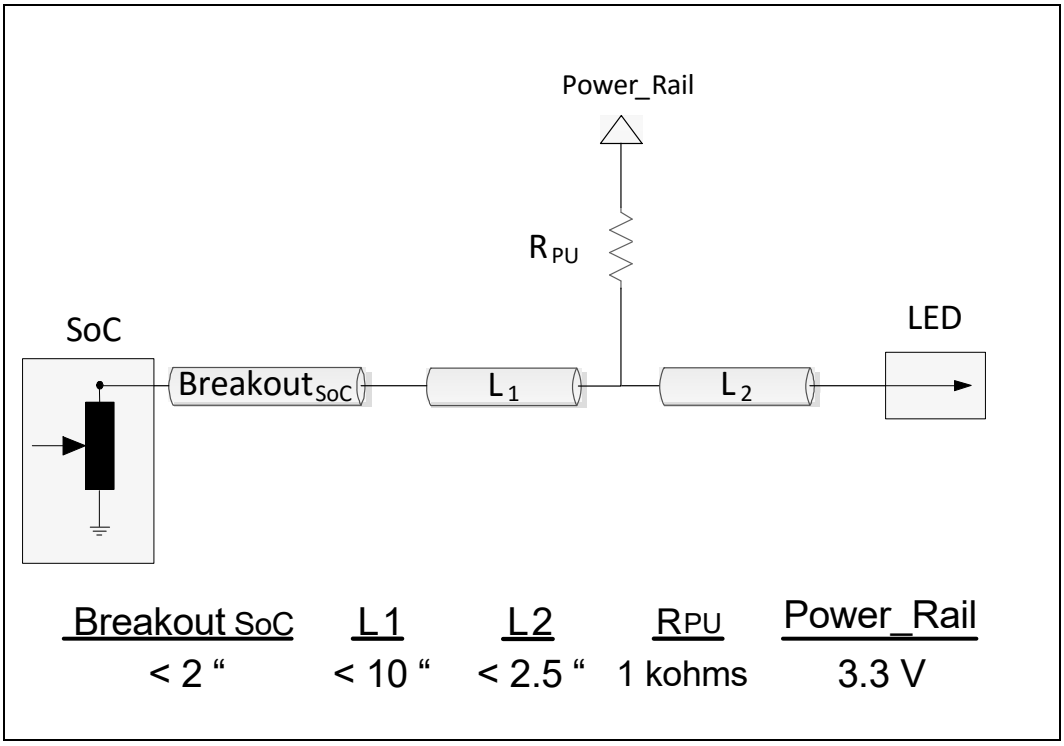


Table 13-67. FAN_PWM [3:0] Interface Layout Recommendations

Routing Section	Layer	Trace Width (mils)	Impedance	Length (mils)		Reference
				min	max	
$Breakout_{SoC}$	microstrip	3.5	54 Ω ± 15%	0	2000	GND
	stripline	3.5	52 Ω ± 10%			GND
L1	all			0	10000	GND
L2				0	2500	GND
Entire Signal	microstrip	4.1	50 Ω ± 15%	0	14500	
	stripline	3.87	50 Ω ± 10%			

Notes:
1. Resistor Tolerance is ± 5%.
2. This design uses a hybrid stack-up with material type IT150DA for microstrip layers and material type IT180I for prepreg and stripline layers with a 2.5 mil thick dielectric on microstrip and a 3 mil thick dielectric on stripline.

Table 13-68. FAN_PWM [3:0] Interface Layout Recommendations: Trace Spacing (Mils)

Routing Section	Layer	1V Aggressors			3.3V/1.8V Aggressors			Static Signals		
		Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via	Trace to Trace	Trace to Via	Via to Via
$Breakout_{SoC}$	microstrip	4	4	5	4	4	5	4	4	5
	stripline	4	4	5	4	4	5	4	4	5
Entire Signal	microstrip	10	4	5	15	4	5	5	4	5
	stripline	8	4	5	13	4	5	4	4	5

13.5 Debug Interface

Table 13-69 lists the signals associated with the debug port. For the design guidelines of the ITP (In Test Port) debug port refer to the Denverton and Denverton-NS SoC 60-Pin Debug Port Specification Design Guide, Document ID #556262. If not used, CTBTRIGOUT and CTBRIGINOUT should be left as no connect (NC).

Table 13-69. List of Debug Port Signals

Signal Name	Direction	Shared	Description
CTBTRIGINOUT	I/O	Yes	CTB Trigger: Signals for triggering an external logic analyzer based on internal SoC events.
CTBTRIGOUT	O	Yes	
CX_PRDY_N	O-OD	Yes	Debug Port Signals: For connection to a MIPI-60 header on the board, please check the *Denverton and Denverton-NS SoC 60-Pin Debug Port Specification Design Guide*.
CX_PREQ_N	I	Yes	
DFX_PORT[15:0]	O	Yes	
DFX_PORT_CLK[1:0]	O	Yes	
RTEST_N	I	No	RTC Battery Test: Active-low signal. An external RC circuit creates a time delay for the signal such that it goes high (VCCRTC voltage level) sometime after the battery voltage is valid. The RC time delay must be in the 10-20 ms range. This allows the SoC to detect when a new battery has been installed. This signal is internally asserted after the suspend power is up if the coin cell battery is weak. When active, this signal also resets some bits in the RTC power well that are otherwise not reset by PLTRST_N, RSMRST_N, or SRTCRST_N. ***Note:*** This signal may also be used as input signal into Debug Port for debug purposes.
Test Access Port 0			
TCK	I	No	Test Clock
TDI	I	No	Test Data Input
TDO	I/O-OD	No	Test Data Output
TMS	I	No	Test Mode Select
TRST_N	I	No	Test Reset
Test Access Port 1			
TCK	I	No	Test Clock
TDI	I	No	Test Data Input
TDO	I/O-OD	No	Test Data Output
TMS	I	No	Test Mode Select
TRST_N	I	No	Test Reset

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14 Platform Reset Considerations

This chapter describes platform-level requirements to bring the SoC out of reset successfully in various operating modes/conditions. It is intended to aid the understanding of what happens when various types of resets occur as they relate to board design and to be able to employ some of the secondary functions of the reset-related signals. The chapter will also offer practical advice on dealing with reset and sequencing issues based on Intel's history with board designs.

14.1 Requirements for Bringing the SoC Out of Reset

The SoC silicon is an amalgamation of several uniquely designed blocks each with their own power rail and reset signal requirements. A system designer has to coordinate many electrical elements on board for these platform elements to come out of reset and operate correctly: run software, IO interfaces that respond to input correctly, etc. This section describes the order and timing requirements of these elements and provides implementation examples that have been employed successfully in production systems.

Please note that the power and reset logic of the SoC is fundamental to all system operation. The requirements in the following sections, therefore, need to be followed completely with no exceptions. If any of the requirements are not followed (an ordering requirement among reset signals is not followed for example) then the system will not operate correctly and may present a wide range of symptoms: the SoC may not exit S5 during a cold reset, the board could exhibit a variety of memory errors, the PCI/PCIe devices may be inaccessible, or the SoC may experience "random hangs" during what should be normal board operation.

It is very important to review the requirements in this section, implement your platform to align with them, and plan to measure the power rails and signals mentioned here once the first boards come back from manufacturing to obviate hard-to-diagnose problems (as discussed above) in system development and deployment.

The following sub-sections describe the sequence of events that occur during a cold or warm reset including events that the platform must generate: inputs to the SoC. While general behavior is described here. For details, refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*, in Chapter 33 entitled "Resets and Voltage Sequencing" for either software or hardware events initiating a cold or warm reset.

14.1.1 Reset Sequence

A cold reset is where the system powers on from a total off state: no wall power applied. A warm reset may be triggered when the system is already powered on and able to run code. To be specific a warm reset sequence is the same as the cold reset except that the SoC SUS well, DDR4 power, and Core well power remain on during the entire sequence. The platform also provides valid reference clocks to the SoC during the entire warm reset sequence.

The platform starts up all power rails and asserts the various reset signals in the order and with the timings. Refer to Chapter 34 in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* for the signals and timings.

14.1.2 Special Note on First Board Bring-up

System designers should plan on a regime of physical measurements that include the power rail and reset signal sequences described in the sections above on their first boards from their ODM to make sure that they adhere to the order and timing specifications. Even with the best intentions during the design phase, oversights or manufacturing errors are common and either can cause a platform to malfunction.

To minimize the work of measuring all necessary signals, Intel recommends focusing on the INPUTS to the SoC since the SoC outputs should respond per specification. The following is a recommended list of waveform captures (i.e. via oscilloscope) that should be collected to verify proper behavior of the platform. Refer to the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*, in Chapter 34 entitled "Resets and Voltage Sequencing" for the specific timings.

14.2 Reset-related Use Cases

The following sections describe common reset-related scenarios that need to be handled or features that can be implemented in the platform.

14.2.1 Holding the SoC in Reset

On a board with many components, race conditions might develop when one part exits reset outside the specification needed by the SoC. The most common example is when all devices that need to be enumerated on the main PCIe bus must be out of reset and ready to be discovered by the time the enumeration algorithm in the BIOS code starts running. If such a PCIe end-point (EP) needs more time to come out of reset, a solution is to add a delay in the BIOS code or monitor a GPI indication that the device is ready.

Alternatively, a designer may wish to "hold" the SoC in reset. The board's power rails come up, the SoC goes into the S5 power state, but the reset sequence does not complete: PMU_PLTRST-N does not deassert, the cores do not start executing BIOS, etc. until some time when the PCIe end point devices are all out of reset.

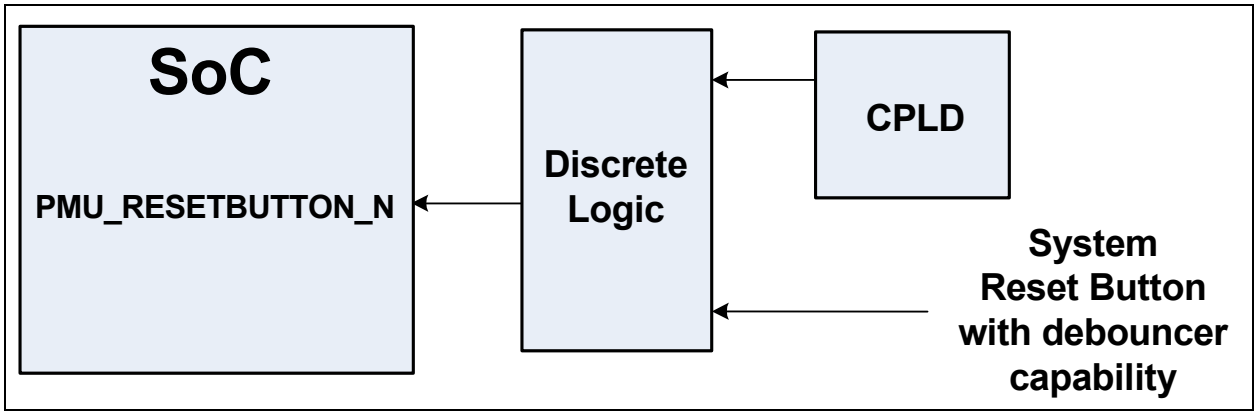
To hold the SoC in reset, the reset sequence may be paused at any point while still maintaining all order and timing requirements as described in the above sections. RSMRST_N, for example, could be held low for as long as necessary to power up the PCIe EP.

Recall that the platform must maintain the proper order and timing for all rails/signals that control reset. If there are race conditions the reset period should be extended as discussed above. The most common signal used for this function is COREPWROK. It indicates that the SoC has gone far enough in the reset sequence to allow the power rails and clocks to come up and be stable. It stops, however, before the first instruction fetch goes to the boot flash connected on the SPI interface.

14.2.2 Causing a Warm Reset via Hardware

While there are many ways to cause a warm reset via software - *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*, in Chapter 33 - the only way to initiate a warm reset in hardware is to assert the PMU_RESETBUTTON_N signal for a minimum of 16 ms (i.e. drive it to a low voltage level). Figure 14-1 shows how both a physical button or a piece of programmable logic can both be attached to the PMU_RESETBUTTON_N signal allowing for several different use cases on the same platform.

Figure 14-1. Basic PMU_RESETBUTTON_N Implementation

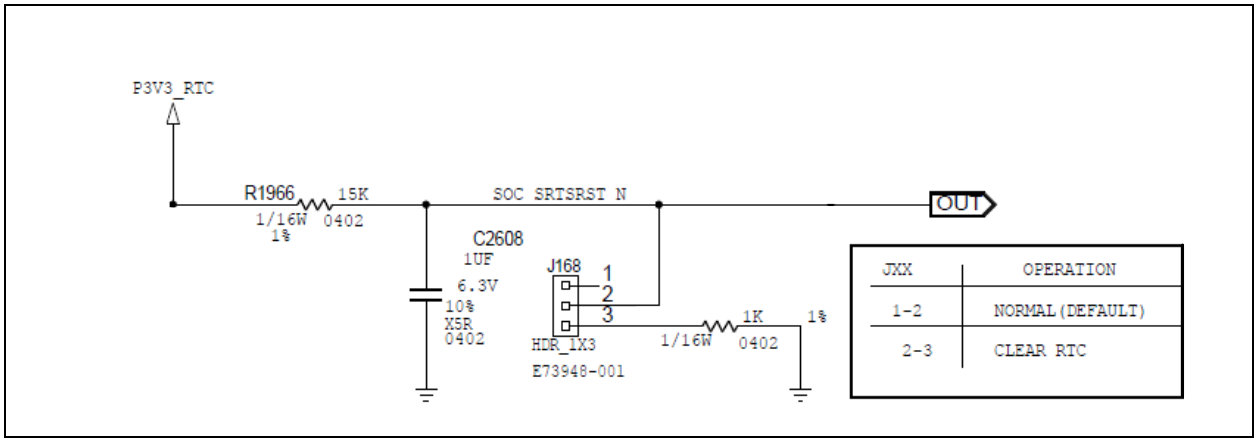


14.2.3 Clearing CMOS (Registers in the RTC Well)

For systems implementing a RTC Well battery the internal CMOS bits can be cleared by asserting the SRTCRST_N signal (logic low) for a minimum of 10 ms. When active, this signal also resets some bits in the RTC power well that are otherwise not reset by PLTRST_N, RSMRST_N, or SRTCRST_N.

Figure 14-2 shows a simple circuit that uses a jumper to pull SRTCRST_N to ground and, therefore, will clear the internal CMOS bits of the SoC if needed.

Figure 14-2. Simple Jumper based Implementation for Clearing CMOS bits-Harcuvar CRB



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15 Platform Power Distribution Guidelines

This chapter includes data on the power supply designs that have been implemented for several Intel Customer Reference Boards (CRBs). These CRBs were designed early during the Denverton Program. Not all the CRBs support all the current Denverton SKUs. The CRB power supply designs may be used as reference and should not be copied exactly for new platform designs.

For the latest SoC power supply requirements, the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4 (Document #558579)* must be referenced for the specific Denverton SKU(s) which the platform must support.

The following tools may be used to test/validate the SoC and memory power supply designs:

1. Denverton 1310 FCBGA interposer with the Gen4 VRTT - used for testing Denverton PVCCP, PVCCRAM, P1V05, and PVNN VRs.
2. DDR4 DIMM VRTT - used for testing DDR4 DIMMs VRs PVDDQ, PVPP, and PVTT rails.

15.1 SoC Power On Sequence

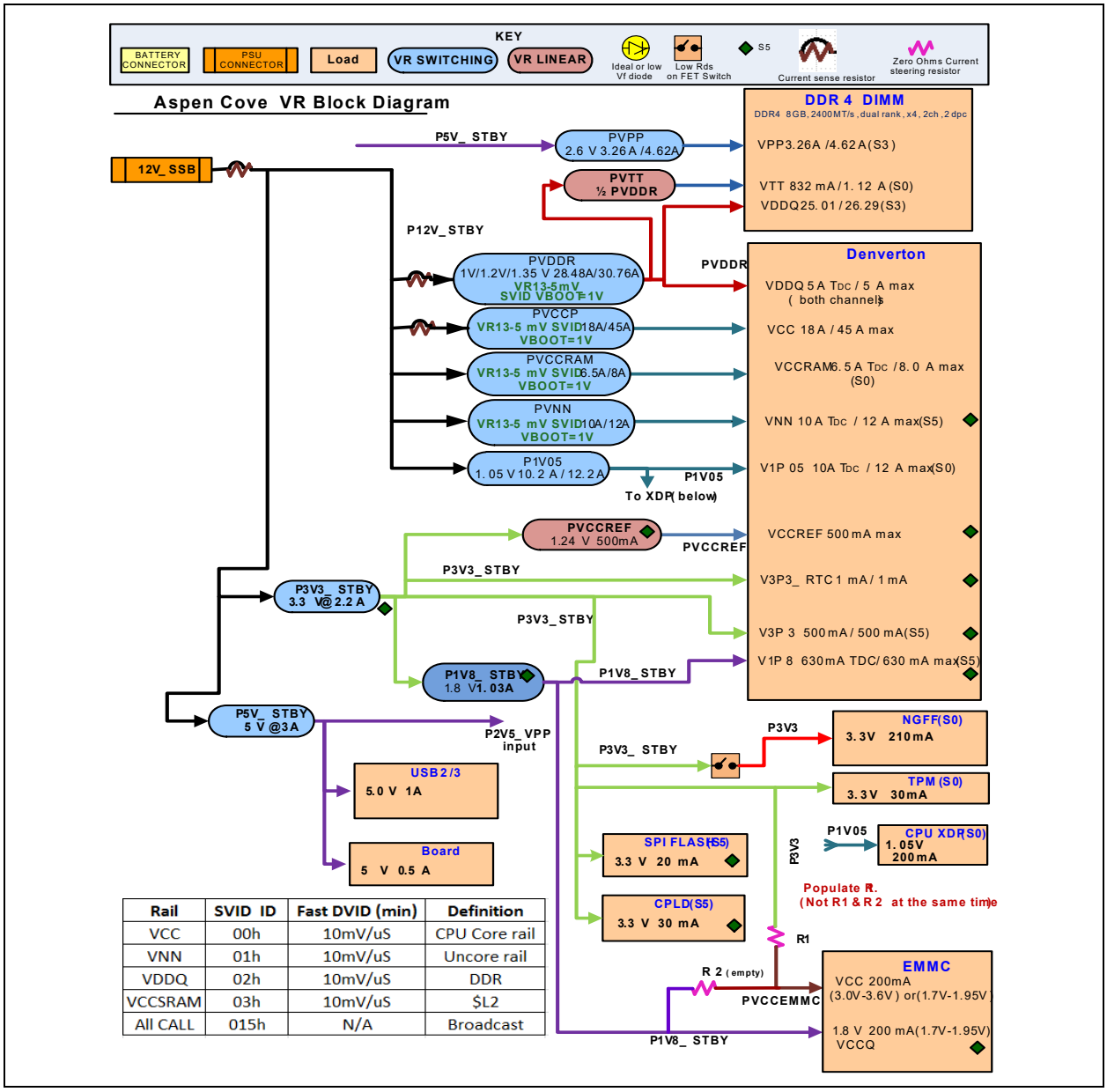
It is critical that all new platform designs meet the power supply sequencing (power-up and power-down) specifications listed in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4 (Document ID #558579).*

15.2 Customer Reference Boards Power Design Block Diagrams

The schematic for the block diagram below are included in the following document:

- Intel Atom Processor Denverton Product Family [Aspen Cove] Customer Reference Board [CRB] SODIMM PDF Schematics *(Document ID #556064)*

Figure 15-1. Aspen Cove Compute Node CRB Power Block

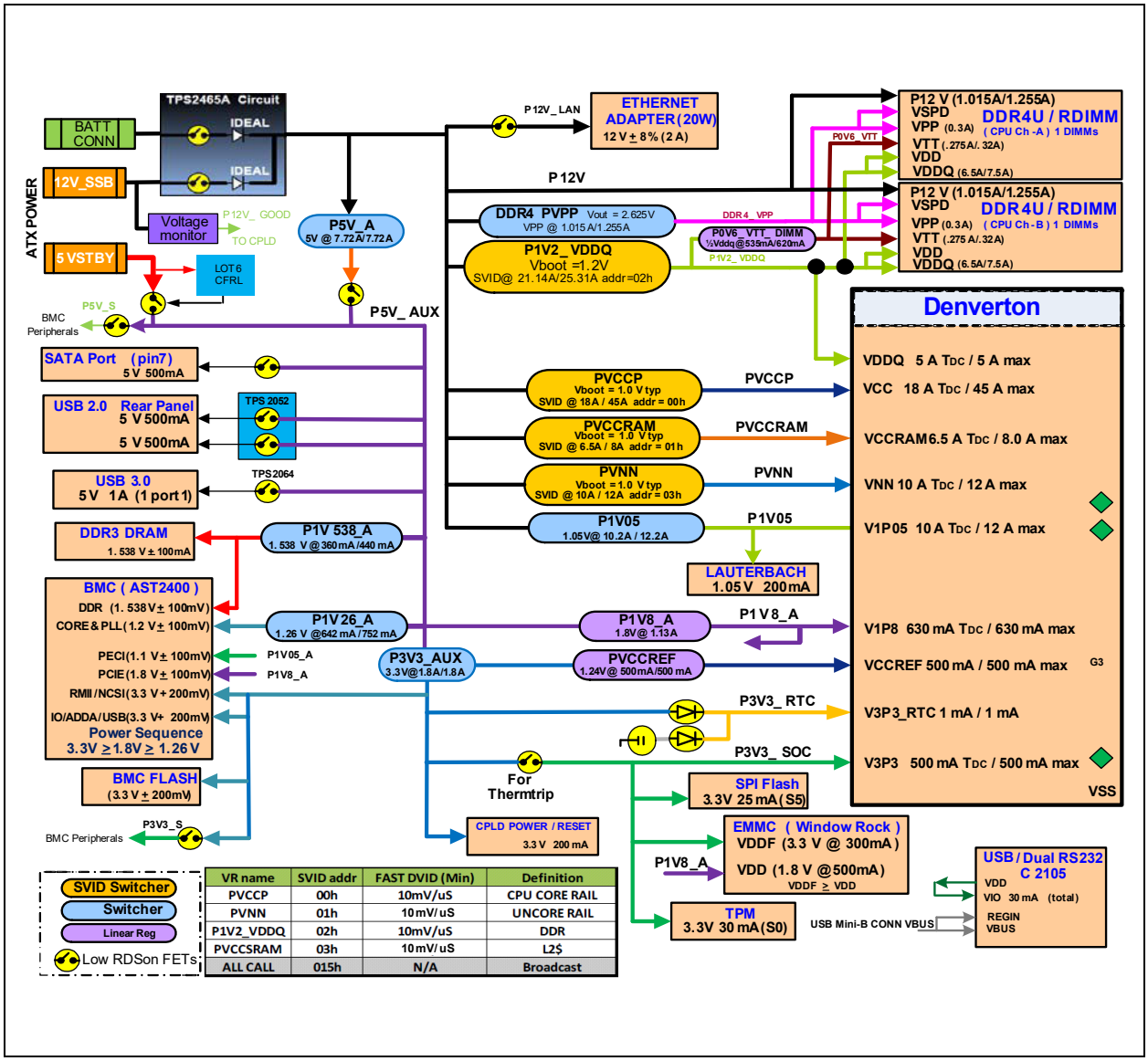


Rail	SVID ID	Fast DVID (min)	Definition
VCC	00h	10mV/uS	CPU Core rail
VNN	01h	10mV/uS	Uncore rail
VDDQ	02h	10mV/uS	DDR
VCCSRAM	03h	10mV/uS	$L2
All CALL	015h	N/A	Broadcast

The schematic for the block diagram below are included in the following document:

- Intel Atom Processor Denverton Product Family [Cormorant Lake] Customer Reference Board [CRB] PDF Schematics *(Document # 565190)*

Figure 15-2. Cormorant Lake Storage Board Power Block

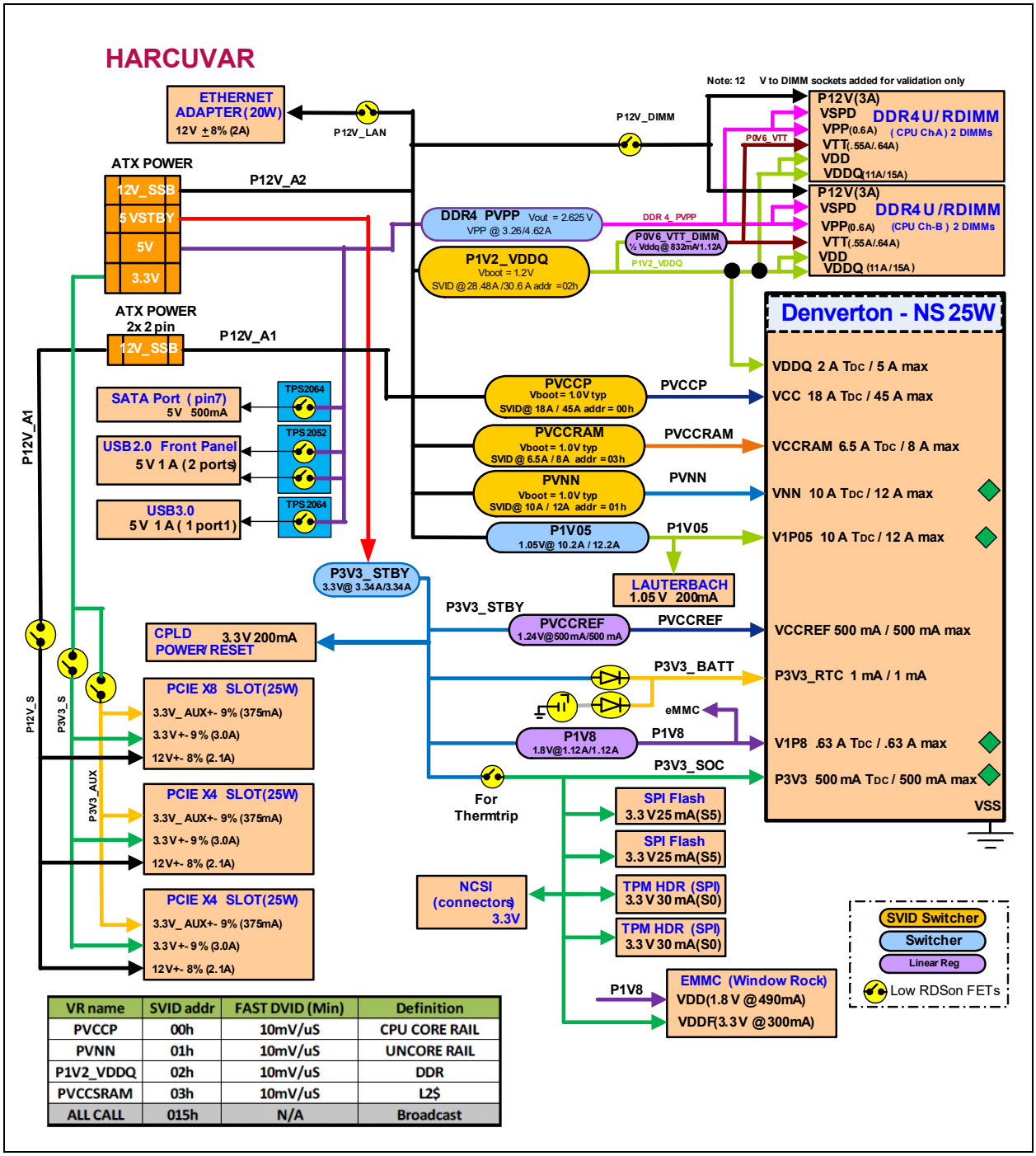


VR name	SVID addr	FAST DVID (Min)	Definition
PVCCP	00h	10mV/uS	CPU CORE RAIL
PVNN	01h	10mV/uS	UNCORE RAIL
P1V2_VDDQ	02h	10mV/uS	DDR
PVCCSRAM	03h	10mV/uS	L2$
ALL CALL	015h	N/A	Broadcast

The schematic for the block diagram below are included in the following document:

- Intel Atom Processor Denverton Product Family [Harcuvar] Customer Reference Board [CRB] PDF Schematics *(Document #556067)*

Figure 15-3. Harcuvar Communications CRB Power Block

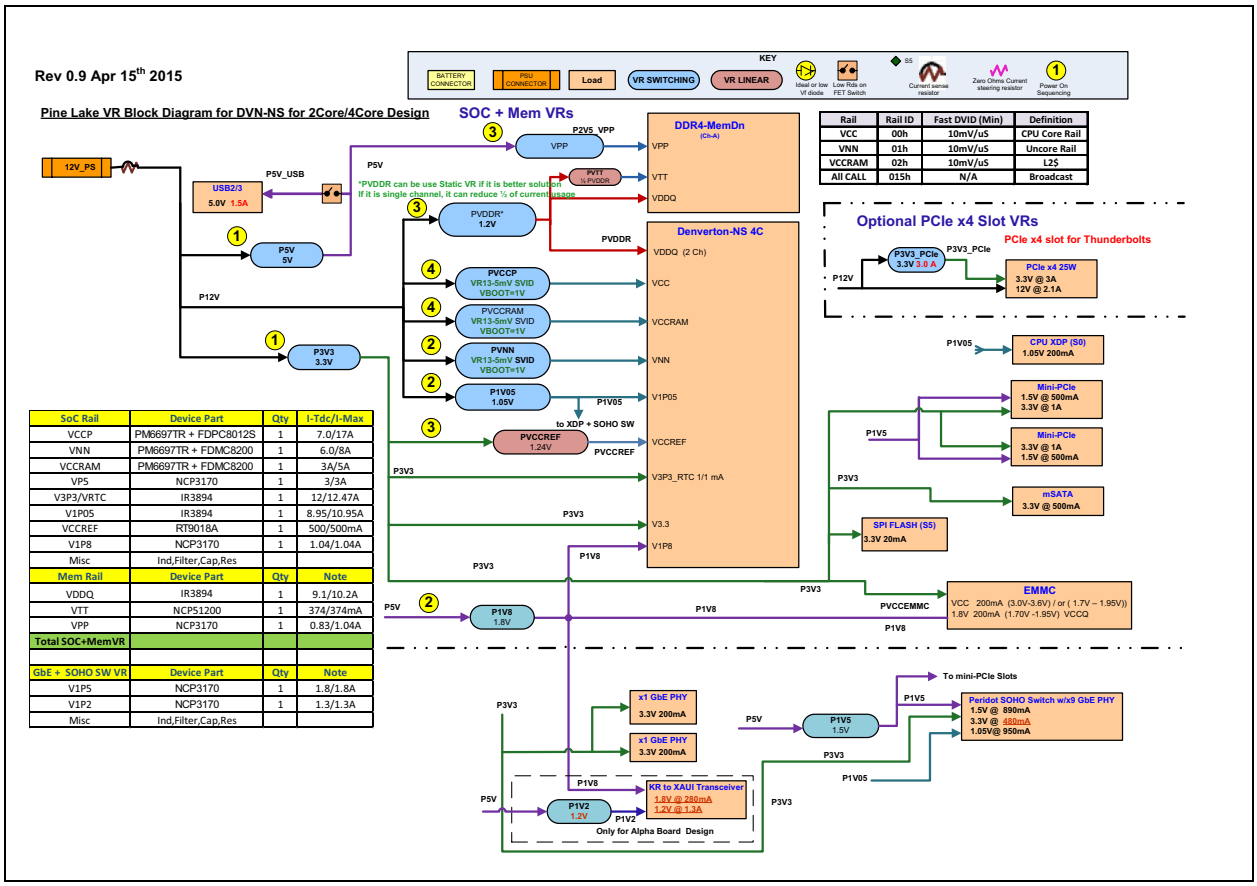


VR name	SVID addr	FAST DVID (Min)	Definition
PVCCP	00h	10mV/uS	CPU CORE RAIL
PVNN	01h	10mV/uS	UNCORE RAIL
P1V2_VDDQ	02h	10mV/uS	DDR
PVCCSRAM	03h	10mV/uS	L2$
ALL CALL	015h	N/A	Broadcast

The schematic for the block diagram below are included in the following document:

- Intel Atom Processor Denverton Product Family Pine Lake PLCC-B Proof of Design Platform for BOM Cost Optimization Design Collateral Beta 1 Release *(Document #568258)*

Figure 15-4. Pine Lake Communications CRB Power Block



Rail	Rail ID	Fast DVID (Min)	Definition
VCC	00h	10mV/uS	CPU Core Rail
VNN	01h	10mV/uS	Uncore Rail
VCCRAM	02h	10mV/uS	L2$
All CALL	015h	N/A	Broadcast

SoC Rail	Device Part	Qty	I-Tdc/I-Max
VCCP	PM6697TR + FDPC8012S	1	7.0/17A
VNN	PM6697TR + FDMC8200	1	6.0/8A
VCCRAM	PM6697TR + FDMC8200	1	3A/5A
VP5	NCP3170	1	3/3A
V3P3/VRTC	IR3894	1	12/12.47A
V1P05	IR3894	1	8.95/10.95A
VCCREF	RT9018A	1	500/500mA
V1P8	NCP3170	1	1.04/1.04A
Misc	Ind,Filter,Cap,Res		
Mem Rail	**Device Part**	**Qty**	**Note**
VDDQ	IR3894	1	9.1/10.2A
VTT	NCP51200	1	374/374mA
VPP	NCP3170	1	0.83/1.04A
Total SOC+MemVR			
GbE + SOHO SW VR	**Device Part**	**Qty**	**Note**
V1P5	NCP3170	1	1.8/1.8A
V1P2	NCP3170	1	1.3/1.3A
Misc	Ind,Filter,Cap,Res		

15.3 CRB DC-DC Converter Designs

The data in the following tables represents the specifications to which the CRBs were originally designed at the onset of the Denverton Program.

Not all CRBs may support all the latest SoC SKUs. The values in the tables below are not necessarily the current SoC specifications.

The power supply specifications for each SoC SKU is documented in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* (Document #558579). For new platform designs, please refer to the EDS for the current SoC SKU(s) specifications.

For the table below, the following definitions apply:

- DC VR Error
  This is the difference between the requested constant load VR output and the measured output averaged over time (tens of ms).
- DC Tolerance
  This is the three sigma of "DC VR Error", over the range of load and over the lifetime.
- VR Ripple
  This is the variation in the output voltage of a regulator due to the switching/sampling characteristics of the regulator. This ripple can be most easily measured by looking at the supply output under a constant load, across the range of loads. The ripple freq will be at the bandwidth of the regulator.
- Ripple Guide
  This is not an SoC specification. This represents a measurement that was taken at the output of the CRB VRs. It is a general guide for the typical ripple measured at the output pins of the CRB VRs.
- AC Tolerance
  The response to transients (I_{STEP} with DI/DT) generated by the SOC or other platform components (e.g., feed-through from the VR input supply, which may have other loads).
- Total Tolerance = DC Tolerance + VR Ripple + AC Tolerance
- Total Tolerance With Load Line = (IxRll) + DC Tolerance + VR Ripple + AC Tolerance = (IxRll) + Total Tolerance
  Where Rll is the Load Line Resistance.

The measurement points for the SoC VR specifications are at the SoC (the load). If access at the SoC is not practical, the measurements may be taken at the input of the VR sense signals, which is nearly identical to what the SoC receives.

Table 15-1. Aspen Cove CRB DC-DC Converter Design

Power Rail	Power	V_{IN}	V_{OUT}	I_{CC} MAX	I_{CC} TDC	DC Tolerance	Ripple Guide	AC Tolerance	Total Tolerance	I_{CC} Step	DI/DT	SVID Addr	SVID FAST Slew
PVCCP	SoC	12V	SVID V_{BOOT} = 1V LL= 2.3 mΩ -0.52V - 1.24V SVID $1.15V_{NOM}$	45A	18A	± 6mV	± 4mV	Load Line Dependent	Load Line ±50mV	35A	510A/µs	00h	10mV/µs
PVCCRAM	SoC	12V	SVID V_{BOOT} = 1V 0.75V - 1.2V $1.15V_{NOM}$	8A	6.5A	± 0.50%	± 8mV	± 6.5%	± 7%	3A	10A/µs	03h	10mV/µs
PVNN	SoC	12V	SVID V_{BOOT} = 1V 0.65V - 1.24V	12A	10A	± 0.50%	± 3mV	± 5.5%	± 6%	5A	80A/µs	01h	10mV/µs
PVDDQ [1]	DIMM/SoC	12V	SVID V_{BOOT} = 1V or 1.2V V_{NOM} = 1.20V (1.21V)/ 1.35V/1V	30.76A	28.48A	± 8mV	± 4mV	+ 41mV/ - 30mV	+ 49mV/- 38mV (1.259V - 1.172V) @ Gold Finger + 50mV/- 50mV (1.260V - 1.160V)	20.03A (3.48A - 23.51A)	15.87A/µs	02h	10mV/µs
PVTT	4 DIMM	VDDQ	1/2 VDDQ	1.12A	832mA	± 28mV	NA	+ 14mV/ - 8mV	+ 42mV/- 36mV (0.647V - 0.569V) @ Gold Finger + 51mV/- 45mV (0.656V - 0.560V)	1.452A Sink 734mA Source 718mA	4.06A/µs	NA	NA
PVPP	4 DIMM	5V	2.6V	4.62A	3.26A	± 1.1%	± 7mV	+ 112mV/ - 143mV	+ 150mV/- 181mV (2.750V - 2.419V) @ Gold Finger + 150mV/- 190mV (2.750V - 2.410V)	4.08A (0.15A - 4.23A)	14.62A/µs	NA	NA
P1V8_STBY	SoC/Board	3.3V	1.8V	1.03A	1.03A	± 2.1%	± 4mV	± 1.9%	± 4%	0.1A	0.1A/µs	NA	NA
P1V05	SoC	12V	1.05V	12.2A	10.2A	± 0.6%	± 3mV	± 19mV	± 25 mV	5A	20A/µs	NA	NA
PVCCREF	SoC	3.3V	1.24V	500mA	500mA	± 2.1%	NA	± 1.9%	± 4%	20mA	0.1A/µs	NA	NA
P3V3_STBY	Board	12V	3.3V	2.2A	2.2A	± 2%	± 11mV	± 3%	± 5%	0.5A	1A/µs	NA	NA
P5V_STBY	Board	12V	5V	3.0A	3.0A	± 1.5%	± 1%	± 3.5%	± 5%	0.5A	1A/µs	NA	NA

Notes:
1. **PVDDQ** - (4 DIMM) [DDR4 8GB, 2400MT/s, dual rank, x4, 2 ch, 2 dpc].

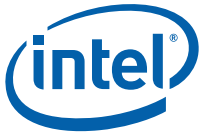


Table 15-2. Cormorant Lake CRB DC-DC Converter Design

Power Rail	Power	V_{IN}	V_{OUT}	I_{CC} MAX	I_{CC} TDC	DC Tolerance	Ripple Guide	AC Tolerance	Total Tolerance	I_{CC} Step	DI/DT	SVID Addr	SVID FAST Slew
PVCCP	SoC	12V	SVID V_{BOOT} = 1V LL= 2.3 mΩ -0.52V - 1.24V SVID $1.15V_{NOM}$	45A	18A	± 6mV	± 4mV	Load Line Dependent	Load Line ± 25mV	20A	150A/µs	00h	10mV/µs
PVCCRAM	SoC	12V	SVID V_{BOOT} = 1V 0.75V - 1.2V $1.15V_{NOM}$	8A	6.5A	± 0.50%	± 8mV	± 6.5%	± 7%	3A	10A/µs	03h	10mV/µs
PVNN	SoC	12V	SVID V_{BOOT} = 1V 0.65V - 1.24V	12A	10A	± 0.50%	± 3mV	± 5.5%	± 6%	5A	80A/µs	01h	10mV/µs
PVDDQ [1]	DIMM/SoC	12V	SVID V_{BOOT} = 1V or 1.2V V_{NOM} = 1.20V (1.21V)/ 1.35V/1V	25.31A	21.14A	± 8mV	± 4mV	+ 41mV/ - 33mV	+ 49mV/ - 41mV (1.259V - 1.169V) @ Gold Finger + 50mV/- 50mV (1.260V - 1.160V)	15A (1.7A - 16.74A)	14.74A/µs	02h	10mV/µs
PVTT	2 DIMM	VDDQ	1/2 VDDQ	620mA	535mA	± 28mV	NA	+ 15mV/ - 19mV	+ 43mV/ -4 7mV (0.648V - 0.558V) @ Gold Finger + 46mV/- 50mV (0.651V - 0.555V)	894mA Sink 479mA Source 415mA	2.3A/µs	NA	NA
PVPP	2 DIMM	5V	2.6V	1.255A	1.015A	± 1.1%	± 7mV	+ 109mV/ - 158mV	+ 138mV/- 187mV (2.738V - 2.413V) @ Gold Finger + 150mV/- 190mV (2.750V - 2.410V)	0.878A (0.137A - 1.015A)	3.68A/µs	NA	NA
P1V8_STBY	SoC/Board	5V	1.8V	1.13A	1.13A	± 2.1%	± 4mV	± 1.9%	± 4%	0.1A	0.1A/µs	NA	NA
P1V05_A	SoC	12V	1.05V	12.2A	10.2A	± 0.6%	± 3mV	± 19mV	± 25mV	5A	20A/µs	NA	NA
PVCC_REF	SoC	3.3V	1.24V	500mA	500mA	± 2.1%	NA	± 1.9%	± 4%	20mA	0.1A/µs	NA	NA
P3V3_AUX	Board	5.0V	3.3V	1.8A	1.8A	± 2%	± 11mV	± 3%	± 5%	0.5A	1A/µs	NA	NA
P5V_A	Board	12V	5V	7.72A	7.72A	± 1.5%	± 1%	± 3.5%	± 5%	0.5A	1A/µs	NA	NA
P1V538_A	Board	5V	1.538V	440mA	360mA	± 3%	± 1%	± 3%	± 6%	0.1A	0.1A/µs	NA	NA
P1V26_A	Board	5V	1.26V	752mA	642mA	± 3%	± 1%	± 3%	± 6%	0.1A	0.1A/µs	NA	NA

Notes:
1. **PVDDQ** - (2 DIMM) [DDR4 8GB, 2400MT/s, dual rank, x4, 2 ch, 1 dpc].

Table 15-3. Harcuvar CRB DC-DC Converter Design

Power Rail	Power	V_{IN}	V_{OUT}	I_{CC} MAX	I_{CC} TDC	DC Tolerance	Ripple Guide	AC Tolerance	Total Tolerance	I_{CC} Step	DI/DT	SVID Addr	SVID FAST Slew
PVCCP	SoC	12V	SVID V_{BOOT} = 1V LL= 2.3 mΩ -0.52V - 1.24V SVID $1.15V_{NOM}$	45A	18A	± 6mV	± 4mV	Load Line Dependent	Load Line ±25mV	20A	150A/µs	00h	10mV/µs
PVCCRAM	SoC	12V	SVID V_{BOOT} = 1V 0.75V - 1.2V $1.15V_{NOM}$	8A	6.5A	± 0.50%	± 8mV	± 6.5%	± 7%	3A	10A/µs	03h	10mV/µs
PVNN	SoC	12V	SVID V_{BOOT} = 1V 0.65V - 1.24V	12A	10A	± 0.50%	± 3 mV	± 5.5%	± 6%	5A	80A/µs	01h	10mV/µs
PVDDQ [1]	DIMM/SoC	12V	SVID V_{BOOT} = 1V or 1.2V V_{NOM} = 1.20V (1.21V)/ 1.35V/1V	30.6A	28.48A	± 8mV	± 4mV	+ 42mV/ - 34mV	+ 50mV/ - 42mV (1.260V - 1.168V) @ Gold Finger + 50mV/- 50mV (1.260V - 1.160V)	20.11A (3.49A - 23.6A)	17.88A/µs	02h	10mV/µs
PVTT	4 DIMM	VDDQ	1/2 VDDQ	1.12A	832mA	± 28mV	NA	+ 9mV/ - 13mV	+ 37mV/ - 41mV (0.642V - 0.564V) @ Gold Finger + 46mV/- 50mV (0.651V -0.555V)	1.452A Sink 734mA Source 718mA	4.08A/µs	NA	NA
PVPP	4 DIMM	5V	2.6V	4.62A	3.26A	± 1.1%	± 7mV	+ 113mV - 134mV	+ 142mV/- 162mV (2.742V - 2.438V) @ Gold Finger + 150mV/- 190mV (2.750V - 2.410V)	4.08A (0.15A - 4.23A)	14.62A/µs	NA	NA
P1V8_A	SoC/Board	3.3V	1.8V	1.12A	1.12A	± 2.1%	± 4mV	± 1.9%	± 4%	0.1A	0.1A/µs	NA	NA
P1V05_A	SoC	12V	1.05V	12.2A	10.2A	± 0.6%	± 3mV	± 19mV	± 25mV	5A	20A/µs	NA	NA
PVCC_REF	SoC	3.3V	1.24V	500mA	500mA	± 2.1%	NA	± 1.9%	± 4%	20mA	0.1A/µs	NA	NA
P3V3_STBY	Board	5.0V	3.3V	3.34A	3.34A	± 2%	± 11mV	± 3%	± 5%	0.5A	1A/µs	NA	NA

Notes:
1. **PVDDQ** - (4 DIMM) [DDR4 8GB, 2400MT/s, dual rank, x4, 2 ch, 2 dpc].

Table 15-4. Pine Lake CRB DC-DC Converter Design

Power Rail	Power	V_{IN}	V_{OUT}	I_{CC} MAX	I_{CC} TDC	DC Tolerance	Ripple Guide	AC Tolerance	Total Tolerance	I_{CC} Step	DI/DT
VCCP	SoC	12V	SVID V_{BOOT} = 1V LL= 2.3 mΩ -0.52V - 1.24V SVID $1.15V_{NOM}$	17A	7A	± 6mV	± 4mV	Load Line Dependent	Load Line ± 25mV	10A	120A/µs
VCCRAM	SoC	12V	SVID V_{BOOT} = 1V 0.75V - 1.2V $1.15V_{NOM}$	5A	3A	± 0.50%	± 8mV	± 6.5%	± 7%	1.5A	5A/µs
VNN	SoC	12V	SVID V_{BOOT} = 1V 0.65V - 1.24V	8A	6A	± 0.50%	± 3mV	± 5.5%	± 6%	3.5A	60A/µs
VDDQ_CPU_DDR [1]	SO-DIMM + Memory Down +SoC	12V	V_{NOM} = 1.20V	10.2A	9.1A	± 8mV	± 4mV	+ 49mV/ - 24mV	+ 57mV/- 32mV (1.257V - 1.168V) @ Gold Finger + 60mV/- 40mV (1.260V - 1.160V)	4.28A (0.63A-4.9A)	12.1A/µs
VTT_CPU_DDR	SO-DIMM+ Memory Down	VDDQ	1/2 VDDQ	374mA	374mA	± 28mV	NA	+ 7mV/ - 8mV	+ 35mV/- 36mV (0.635V - 0.564V) @ Gold Finger + 51mV/- 50mV (0.651V - 0.555V)	679mA Sink 356mA Source 323mA	0.73A/µs
VPP_CPU_DDR	SO-DIMM+ Memory Down	5V	2.6V	1.04A	0.83A	± 1.6%	± 7mV	+ 108mV/ - 137mV	+ 148mV/- 177mV (2.748V - 2.423V) @ Gold Finger + 150mV/- 190mV (2.750V - 2.410V)	0.69A (0.14A - 0.83A)	3.2A/µs
V1P80	SoC/Board	5V	1.8V	1.04A	1.04A	± 1.6%	± 1%	± 2.4%	± 4%	0.1A	0.1A/µs
V1P05	SoC	12V	1.05V	10.95A	8.95A	± 0.6%	± 3mV	± 19mV	± 25mV	5A	15A/µs
VCCREF	SoC	3.3V	1.24V	500mA	500mA	± 1.6%	NA	± 2.4%	± 4%	20mA	0.1A/µs
V3P30	Board	12V	3.3V	12.47A	12A	± 1.5%	± 11mV	± 3.5%	± 5%	0.5A	1A/µs
V5A	Board	12V	5V	3A	3A	± 2.5%	± 1%	± 2.5%	± 5%	0.5A	1A/us
V1P5	Board	5V	1.5V	1.8A	1.8A	± 2.5%	± 1%	± 2.5%	± 5%	0.3A	1A/us
V1P2	Board	5V	1.2V	1.3A	1.3A	± 2.5%	± 1%	± 2.5%	± 5%	0.3A	1A/us
V3P3A	Board	12V	3.3V	1A	1A	± 2.5%	± 1%	± 2.5%	± 5%	0.5A	1A/us
V1P5A	Board	3.3V	1.5V	0.3A	0.3A	± 2.5%	± 1%	± 2.5%	± 5%	0.1A	1A/us

Notes:

1. **VDDQ_CPU_DDR** - 1 SO-DIMM +18 Memory down Devices (DDR4 8GB, 2133, Dual Rank, x8, 2ch, 1 DIMM/ch (SO-DIMMS with ECC + Memory Down).

15.4 SoC Power Delivery

15.4.1 VCCP Voltage Regulator Output Guidelines

The VCCP using a VR13-5mV PWM controllers provides power to the SoCs input. This voltage rail is supplied by a dedicated, one-per-SoC located next to each SoC and as close as possible. The SVID address must be assigned to 00h. The converter must have its differential remote sense pairs terminated at the sense pins: AE37 SENSE_VCCCPUVIDSI0 and AE39 SENSE_VSSCPUVIDSI0 (GND reference) which will terminate to the PVCC and VSS rails on the SoC package side. These pairs should be routed differentially, refer to Section 15.4.1.1, "Remote Sense Connection" for additional details.

Note: The Harrisonville platform SVID design supports VR13-5mV specifications.

Table 15-5. PVCCP VR13-5mV (for SoC) Guidelines

Vcc parameters	Limits / description	Notes
Nominal Voltage = (function of: VID, LL & load)	VID Typ = 1.0V	PVCC_Nom = VID-Rll*ICC PVCC_Min = this is the SoC VID min. (The allowed VID min may be lower depending on variations caused by voltage transients and ripple.) PVCC_Max = VID Max+(VRs TOB) + 50mV for the 1st 25 µs of the permitted overshoot during a load release.
Denverton DC & AC voltage regulation, Load Line (Rll)=	2.3 mΩ LL (subject to change)	no offset
VBoot = 1.0	1.0V	

Notes:

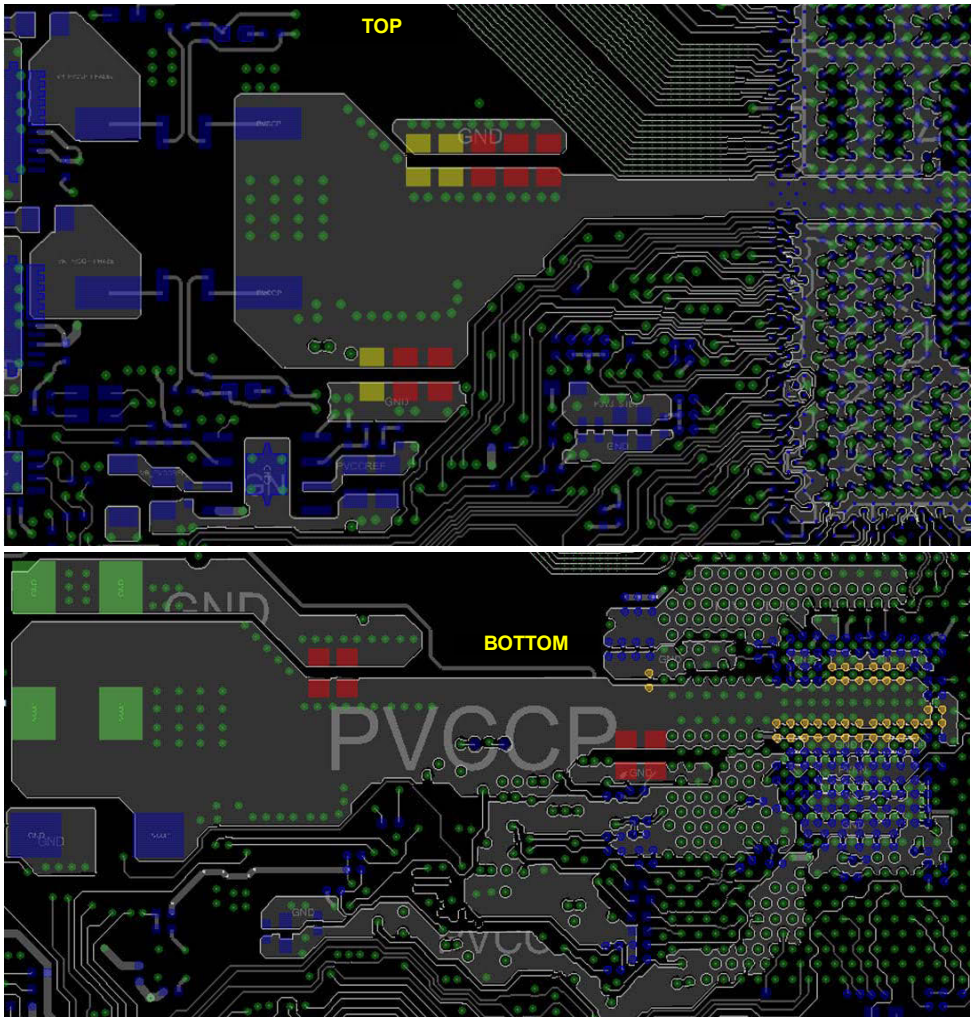
1. Refer to the latest revision of the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* for further and up to date requirements on this VR load limits.
2. The DC and Ripple TOB encompasses the AC tolerance band and must be met. Designers have flexibility in the suggested DC, Ripple, AC and Coupling Noise specifications to better fit their board constraints so long as the DC and Ripple TOB isn't exceeded in static testing and the derived AC tolerance band (function of the starting and ending current) in dynamic current testing is not exceeded.
3. Consult *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4* Dynamic Turbo Chapter for details on PL1 Tau settings and its effect on PL2 load level duration.

Table 15-6. SoC PVCCP VR13-5mV Recommended Output Caps per Interface

Cap Description	Min Quantity	Notes
470uF / 2.5V / 20% / ALUM / 3018	2	Bulk, place close to VR output inductor
47uF / 4V / 20% / X5R / 0805	9	Place as close as possible to SoC
22uF / 6.3V / 20% / X5R / 0805	3	Place as close as possible to SoC
1uF / 10V / 10% / X5R / 0402	15	Place on the bottom layer under SoC
10uF / 6.3V / 20% / X5R / 0402	5	Place on the bottom layer under SoC

Note: The above decoupling caps are minimum recommended for our VR13-5mV design used in the CRBs. But each designer should review their chosen VR topology and adjust the required caps accordingly for up to and including repeated 1 MHz step load frequency. Intel package decoupling has been selected to address frequencies above 1 MHz.

Figure 15-5. PVCCP VR Decoupling Capacitors



15.4.1.1 Remote Sense Connection

Each PVCCP and PVCCRAM rail should include a positive and negative differential remote sense input. These voltage sense lines should draw less than 100 µA of current and there should be a very small voltage drop between the remote sense connection and the VR13-5mV.

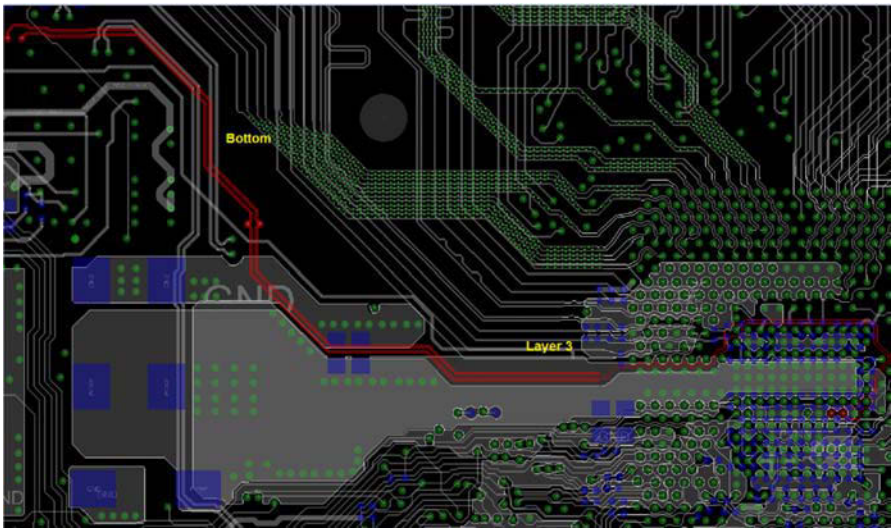
The sense lines from the VR13-5mV controller should be routed to the SoC SENSE_VCCCPUVIDSI0 (pin AE37)/ SENSE_VSSCPUVIDSI0 (pin AE39) and SENSE_VCCRAMCPU_S0 (pin AW36)/ SENSE_VSSRAMCPU_S0 (pin AW37) pin pairs.

Each sense line may be routed through a 0 Ω resistor that is located on the compute node board close to the SoC interface for both embedded VRs or VRMs. This insures that the impedances between the split remote sense routes are kept equal (or as close as possible) to minimize errors and noise pickup that can happen due to lengthy trace routes. This also simplifies the remote sense trace routing from the PWM or VRM to the summing nodes that branch to the SoC interface at the die, Figure 15-12. Designers should consult with their power delivery solution vendor to determine the appropriate resistor value. It is recommended to connect the sense lines across one of the SoC power decoupling capacitors located in the center of the SoC interface. This will provide the option to enable compute node board sensing if required and prevent open remote sense traces, when a SoC is not present. This may also be used during voltage regulator testing and debug.

Note: See Remote Sense Routing Guidelines

- Route differentially where it can be done and try to keep within a maximum of 5 mils separation.
- Traces should be at least 10 mils thick, but may be reduced when routed through the SoC interface field.
- Traces should be routed at least 20 mils away from other signals.
- Each sense line may include a 0 Ω resistor that is placed close to the SoC in order to facilitate a test point.
- For max length of traces - check with the PWM controller manufacturer.
- Avoid routing under or over areas on layers that contain switching signals. For example: VR phase nodes.
- Keep both traces close to the same length.
- Reference a solid ground plane(s) where possible.
- Avoid switching layers, if possible.

Figure 15-6. SENSE_VCCCPUVIDSIO and SENSE_VSSCPUVIDSIO Line Routing for Reference (Red Traces)



On a VRM, the positive sense line will be connected to SENSE_VCCCPUVIDSI0 and the negative sense line will be connected to SENSE_VSSCPUVIDSI0.

15.4.1.2 General Motherboard Power Delivery Design Guide

- Power Plane overlaps are typically not allowed without a ground isolation layer
  - Typically: When the distance between overlap Power Planes are 4x of the closest Ground plane separation, assume small coupling.
  - Any violation to the overlap should be analyzed and the transfer impedance of the overlapped planes should be looked into to understand the mV impact. The additional coupled noise due to overlap, should be added to the AC noise guideline and you will need to make sure the VR design is still meeting the total tolerance band guidelines with the overlap.
  - Higher voltage power planes (12V & 5V) should not be overlapped to smaller voltage power and analog power planes, when in doubt follow the analysis.
- Ground coupling for high power interfaces and for the VRs which share the same ground path needs to be studied.
  - This is the voltage created across ground planes due to high power interface switching events.
  - If no guidelines for ground coupling are provided, a transfer function study should be done. The additional coupled noise due to ground coupling should be subtracted from the provided total tolerance band guideline and the design needs to make sure it is still meeting the total tolerance band guidelines, which would include the ground coupling.

15.4.1.3 VR output enable (OUTEN) input

The VR13-5mVs OUTEN digital input enables (when HI) or disables (when LOW) the PVCC regulator output voltage.

15.4.1.4 VR_Ready Output

When PWRGD_VCCP (VR13-5mV VR_Ready) digital output indicates that the VCCP start-up sequence is good and the output voltage has moved to the programmed VID value. This signal will be used for start-up sequencing for other voltage regulators, clocks, and SoC reset. This signal is not a representation of the accuracy of the DC output to its VID value.

VR_Ready is driven by an Open-Collector / Open-Drain transistor, capable of sinking 1-4 mA in the ON-state. Typically, a 10.0 kΩ 1% pull-up resistor is required on the baseboard to the P3V3_STBY voltage rail.

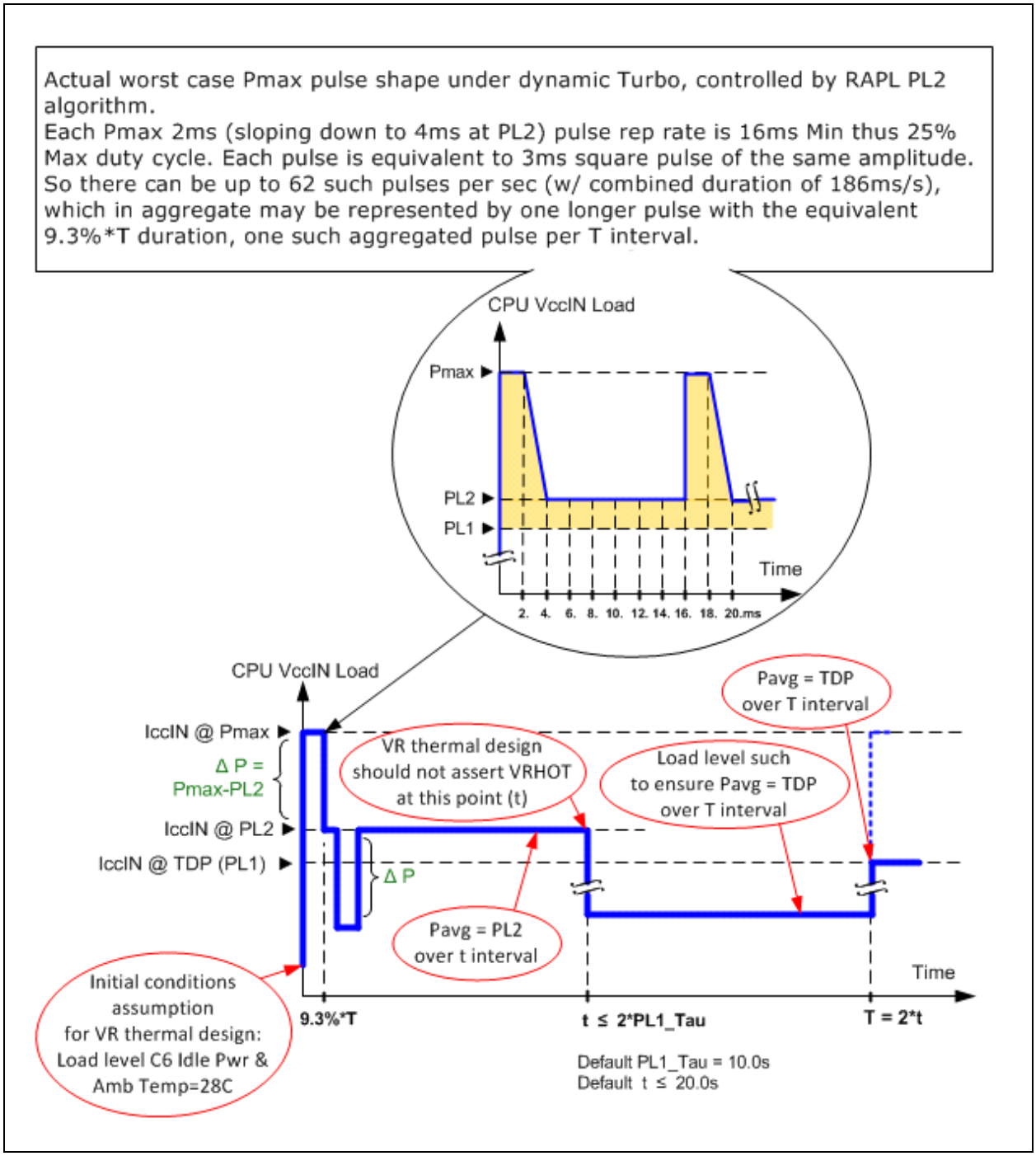
15.4.1.5 SVID BUS Protocol

The VR13-5mV PWM controller must adhere to the VR13-5mV Protocol Bus. Bus protocol details can be found in the Serial VID (SVID) Protocol Specification, Rev 1.7.

15.4.1.6 PVCCP Dynamic Load Characteristic

The following graph is a simplified representation of SoC PVCCP dynamic power (with Turbo enabled) worst case envelope for PVCCP VR design & testing purposes. For more details see the Dynamic Turbo chapter in *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*.

Figure 15-7. SoC PVCCP VR13-5mV Dynamic Load Envelope as a Function of Time



Key points:

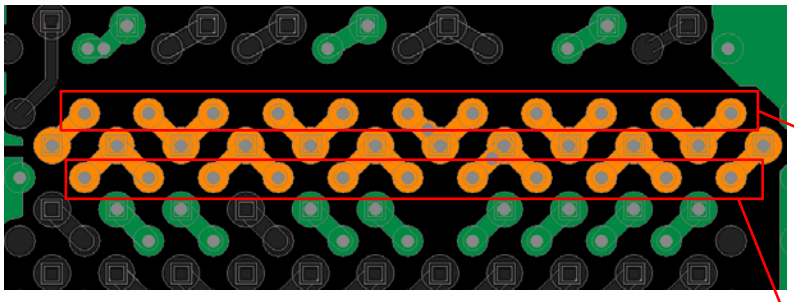
- PL2 level and PL1_Tau (which affects PL2 duration) are both programmable through BIOS.
- PL2 level is programmable up to: PL2=1.2*PL1*(1+Y) and that max value is the default & the recommended setting.
- PL1_Tau range is 0.25s - 40.0s, with default setting = 10.0s, and it is the recommended setting.
- PL2 duration t interval (dynamic Turbo max duration above PL1 interval) may opportunistically last (based on the available SoC thermal headroom below its Tj_{MAX}) until SoC or VR (=VRHOT asserted causes PROCHOT to assert) thermally throttle down to TDP. But the t interval is the max allowed PL2 duration based on the preset PL1_Tau.
- The SoC, using its RAPL algorithm, will regulate its Average Power to: PL2 level over t interval and to PL1 (=TDP) over intervals > T.
- The 9.3%*T interval represents the combined P_{MAX} pulse excursions above PL2 due to Dynamic Turbo (total 186ms pulse duration max per sec), which is balanced by a similar load drop in order to average out to PL2 level at t interval.
- VR electrical design must be able to handle the P_{MAX} for those short periods with low duty cycle and VR thermal design should be robust enough to handle PL2 level for t interval w/o asserting VRHOT.
- The actual duration of the above-PL1-power interval will depend on: PL1_Tau setting, initial power level, the cooling solution for each SoC SKU and the SoC activity factor.

15.4.1.7 DDR Isolation Requirements for P1V05, the P1V2, and Ground

To avoid noise coupling between circuit blocks within the DDR interface it is recommended to follow the power pin isolations described below. This recommendation affects 20 pins on P1V05 rail, 2 pins on the P1V2 rail, and 9 ground pins.

Figure 15-8. P1V05 Isolation-Group 1 and Group 2

Keep Group 1 isolated from Group 2 on the top layer of the board.
Group 1 is the main P1V05 DDR rail (VCCADDR_1P05) while Group 2 is the P1V05 rail for the DDR clock (VCCACKDDR1P05).



Group1	Group2
AA26	AA27
AC26	AC27
AE26	AE27
AG26	AG27
AJ26	AJ27
AM26	AM27
AP26	AP27
AT26	AT27
AU26	AU27
AW26	AW27

Figure 15-9. P1V2 Isolation-Pin Specific

AU24 and AR24 are the P1V2 power pins for the DDR clock (VCCKDDR_VDDQ). They should be isolated from the main P1V2 rail and connected at the farthest layer from the main rail

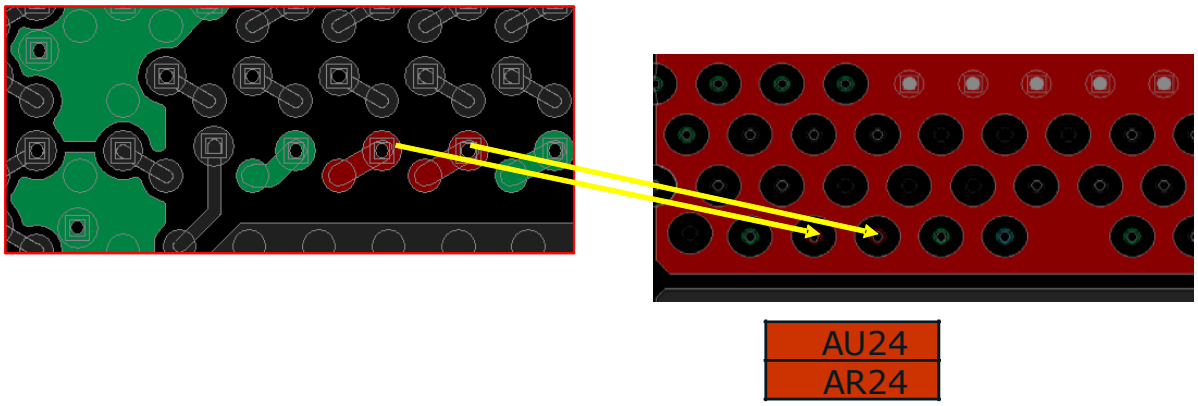
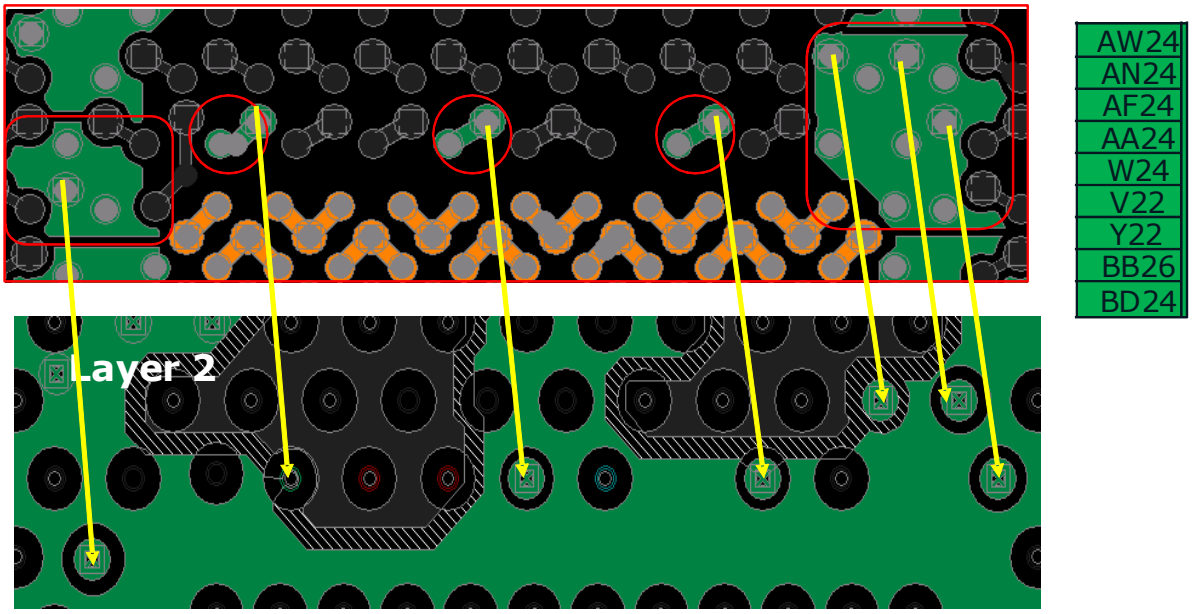


Figure 15-10. Ground Isolation

Isolation is recommended for the ground pins listed below from any top layer GND plane to avoid potential GND noise coupling on the clock rails. Vias connecting these pins should be tied to the GND net on the farthest layer from the top GND layer.



15.4.1.8 VR13-5mV - Power Planes

Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. SoC power should never be distributed by traces alone. This island from the source of power to the load should not have any breaks to minimize inductance in the plane unless specifically described in this document for noise isolation. It should also completely surround all of the pins of the source and all of the pins of the load.

The SoC requires a minimum of 2 ounces of copper per PVCCP rail to deliver power and a minimum of 1 ounce of copper to deliver ground. If available, the board designer should consider using more than 2 ounces of copper for the power rails and 1 ounce of copper for the ground. To maintain a balanced remote sense feedback, the total copper weight used for power and ground should be equal. The 8-layer Intel® Atom™ Processor C3000 Product Family CRBs use two separate power planes to deliver power to the SoC. The CRB uses two ground planes which are shared among VRs. To share the ground planes the voltage regulators must be placed such that the current to one VR does not flow in the same path. This requirement is layout-dependent. If the current paths cross, additional analysis must be done as more than two ounces of copper will likely be needed to satisfy power delivery requirements.

See the CRB 8-layer stackup description for additional details in this document.

To avoid designing more than 1 ounce of copper into the ground planes layout the VRDs (or VRMs) to each VR so there is no possibility of crossing current paths.

Place decoupling caps on the top layer for the VR power plane where possible. The bottom layer can be used if this is not practical.

15.4.2 PVCCRAM VR Sense Routing And Decoupling Recommendations

On a VRM, the positive sense line will be connected to SENSE_VCCRAMCPU_S0 and the negative sense line will be connected to SENSE_VSSRAMCPU_S0.

Figure 15-11. SENSE_VCCRAMCPU_S0 and SENSE_VSSRAMCPU_S0 Line Routing for Reference (Red Traces)

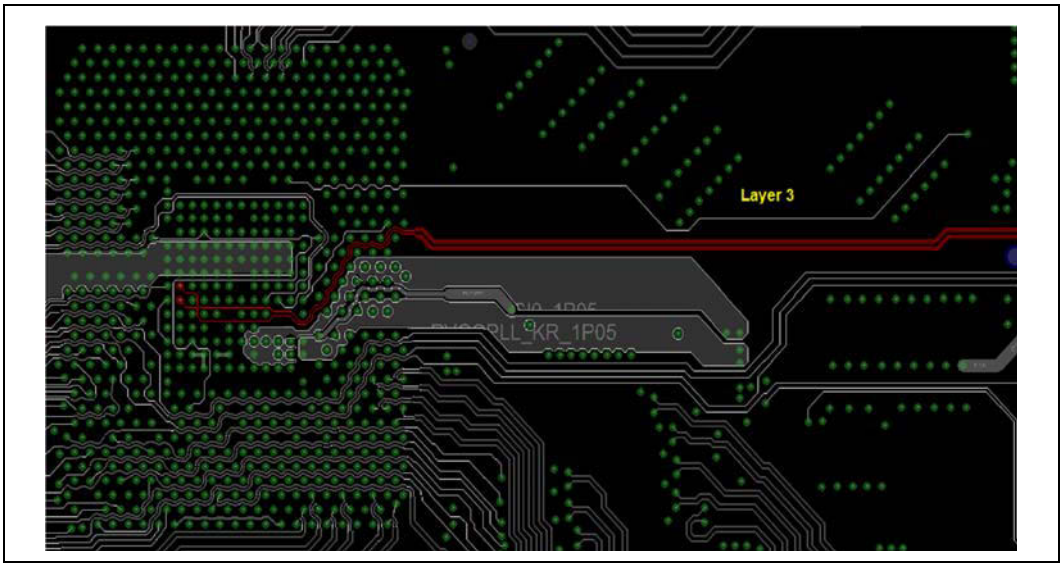
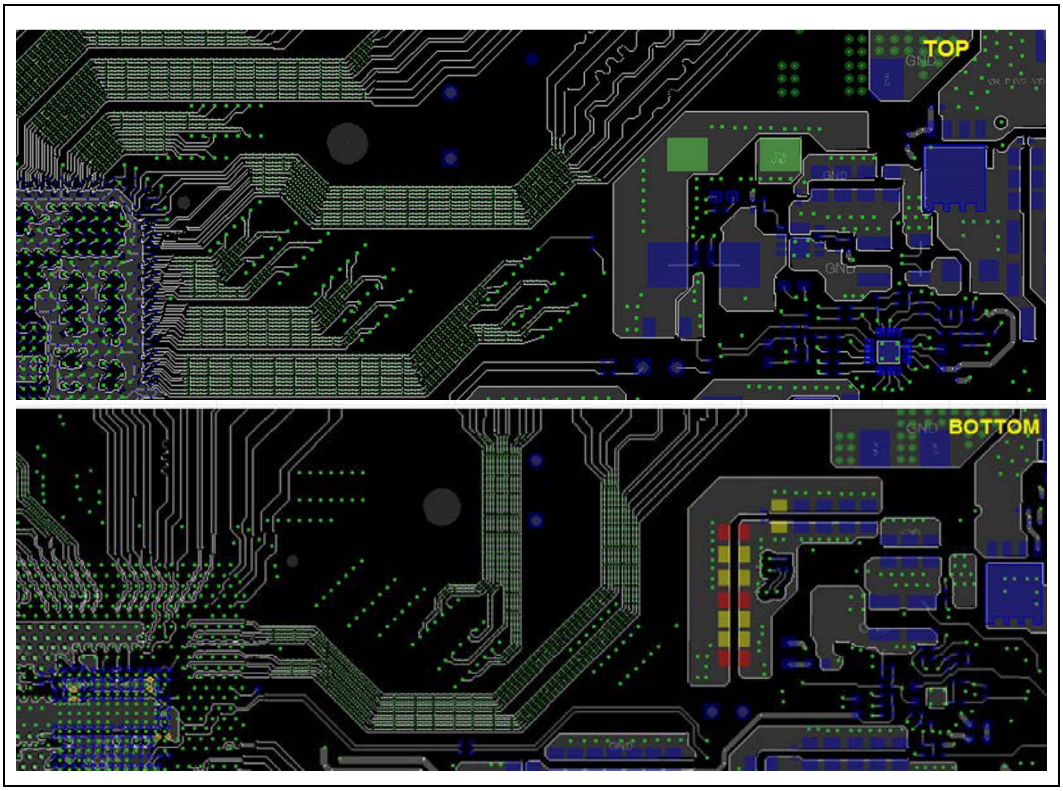


Table 15-7. PVCCRAM VR Bulk/Decoupling Caps based on Aspen Cove

Cap Value	Min Quantity per VR	Notes
470uF / 2.5V / 20% / ALUM / 3018	1	Bulk, place close to VR output inductor (green pads)
47uF / 4V / 20% / X5R / 0805	3	Place close to VR output inductor (red pads)
22uF / 6.3V / 20% / X5R / 0805	5	Place close to VR output inductor (yellow pads)
2.2uF / 6.3V / 20% / X5R / 0402	2	Place on the bottom layer under the SoC (ocher pads)
1uF / 4V / 20% / X5R / 0201	1	Place on the bottom layer under the SoC (ocher pads)

Figure 15-12. PVCCRAM Decoupling Capacitors



15.4.3 PVNN VR Decoupling Recommendations

Table 15-8. PVNN VR Bulk/Decoupling Caps based on CRB

Cap Value	Min Quantity per VR	Notes
470uF / 2.5V / 20% / ALUM / 3018	1	Bulk, place close to VR output inductor (green pads)
47uF / 4V / 20% / X5R / 0805	3	Place close to VR output inductor (red pads)
22uF / 6.3V / 20% / X5R / 0805	6	Place close to VR output inductor (yellow pads)
10uF / 6.3V / 20% / X5R / 0402	7	Place on bottom layer under the SoC (ocher pads)
1uF / 10V /10% / X5R / 0201	7	Place on bottom layer under the SoC (ocher pads)

Figure 15-13. PVNN Decoupling Capacitors

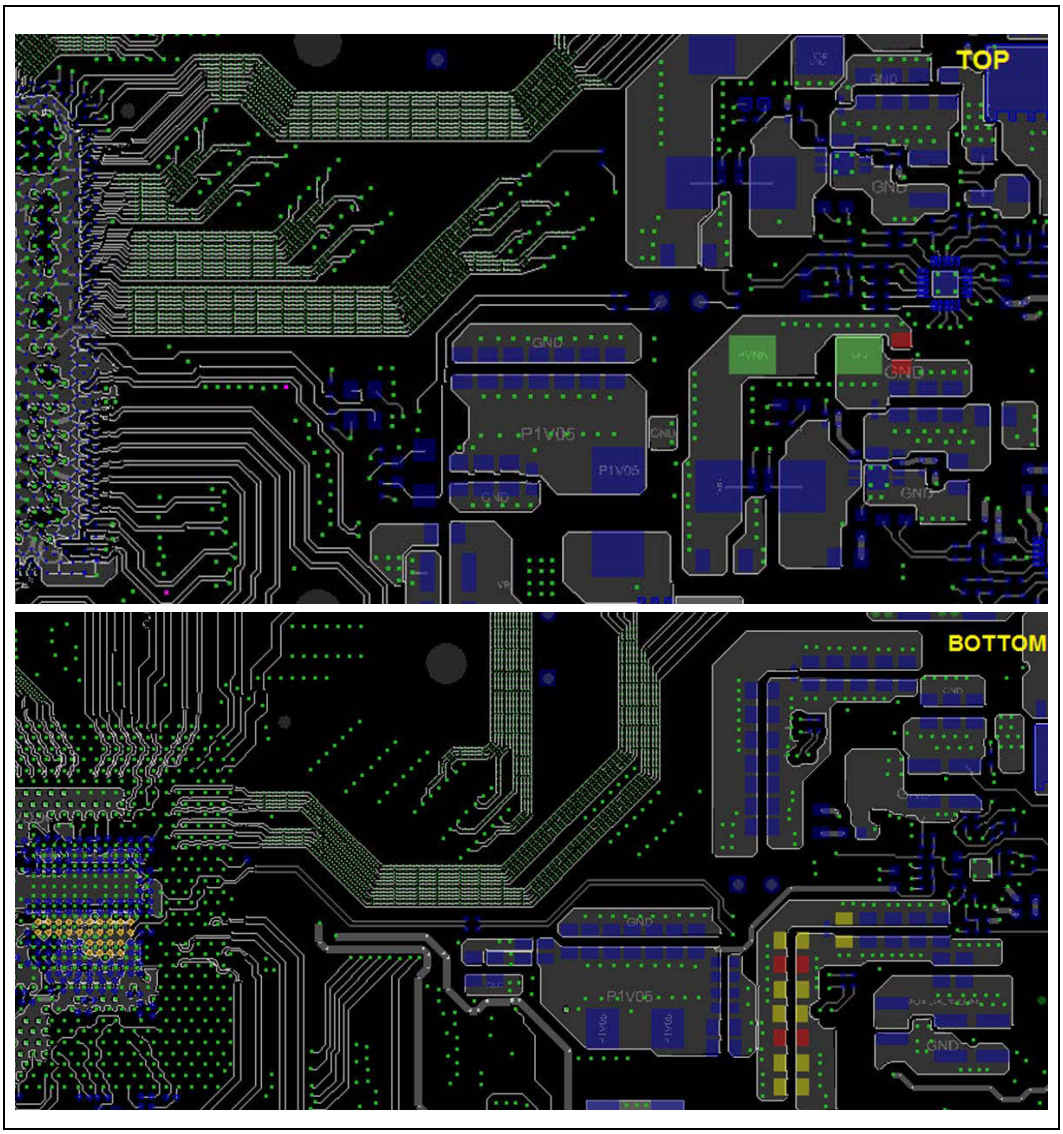
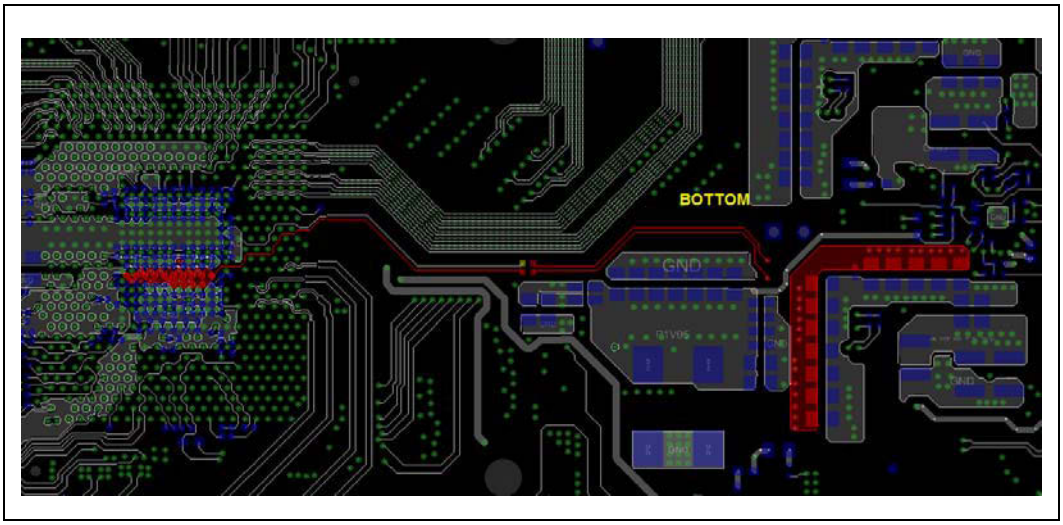


Figure 15-14. PVNN VR VSense - Sense across one of the SOC decoupling caps very close to the SOC.



Note: The sense point should be placed in the SoC area.

15.4.4 P1V05 VR Decoupling Recommendations

Table 15-9. P1V05 VR Bulk/Decoupling Caps based on CRB

Cap Value	Min Quantity per VR	Notes
470uF / 2V / 20% / ALUM / SM	2	Bulk, place close to VR output inductor (green pads)
47uF / 4V / 20% / X6S / 0805	10	Place close to VR output inductor (red pads)
22uF / 6.3V / 20% / X5R / 0805	6	Place close to VR output inductor (yellow pads)
22uF / 6.3V / 20% / X5R / 0603	1	Place close to VR output inductor (pink pads)
10uF / 6.3V / 20% / X5R / 0603	3	Place close to VR output inductor (purple pads)
10uF / 6.3V / 20% / X5R / 0402	16	Place on bottom layer under the SoC (blue pads)
1uF / 10V / 10% / X5R / 0201	7	Place on bottom layer under the SoC (ocher pads)
1uF / 10V / 10% / X5R / 0402	7	Place on bottom layer under the SoC (ocher pads)
1uF / 4V / 20% / X6S / 0201	5	Place on bottom layer under the SoC (blue pads)

Figure 15-15. P1V05 Decoupling Capacitors

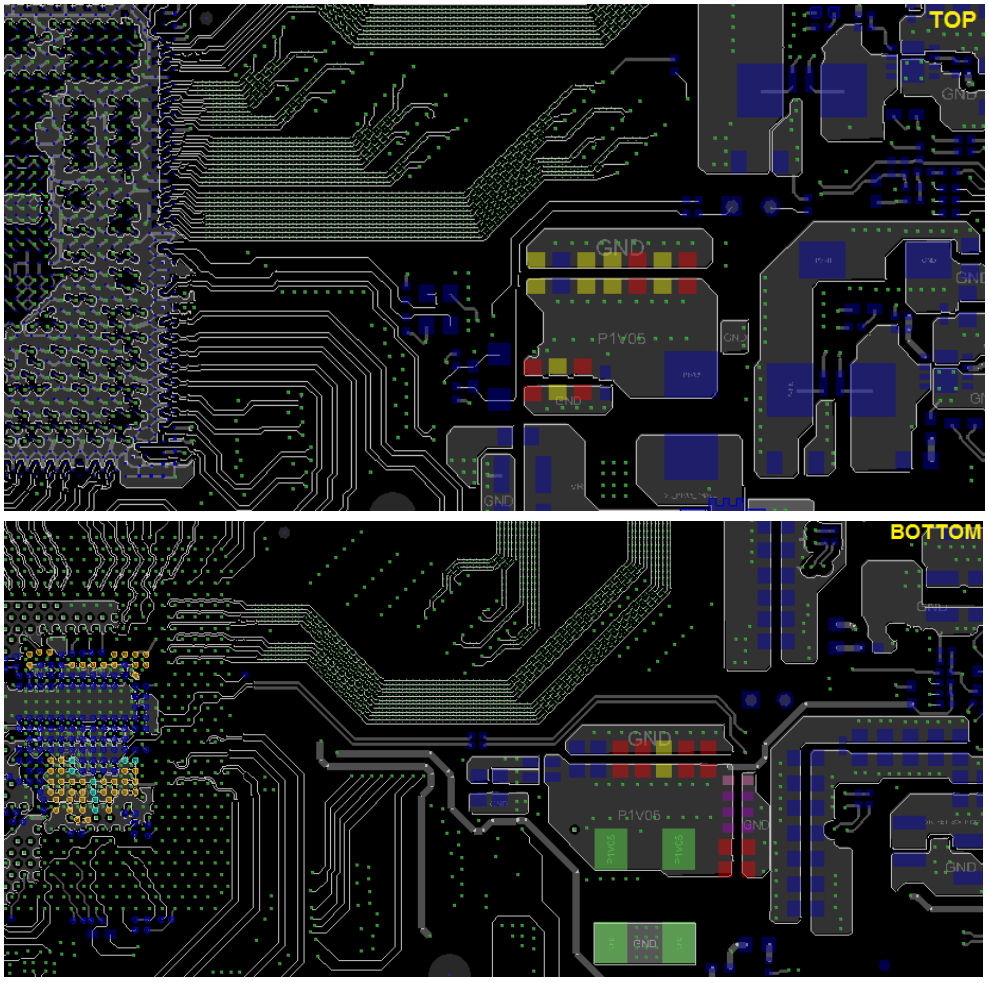
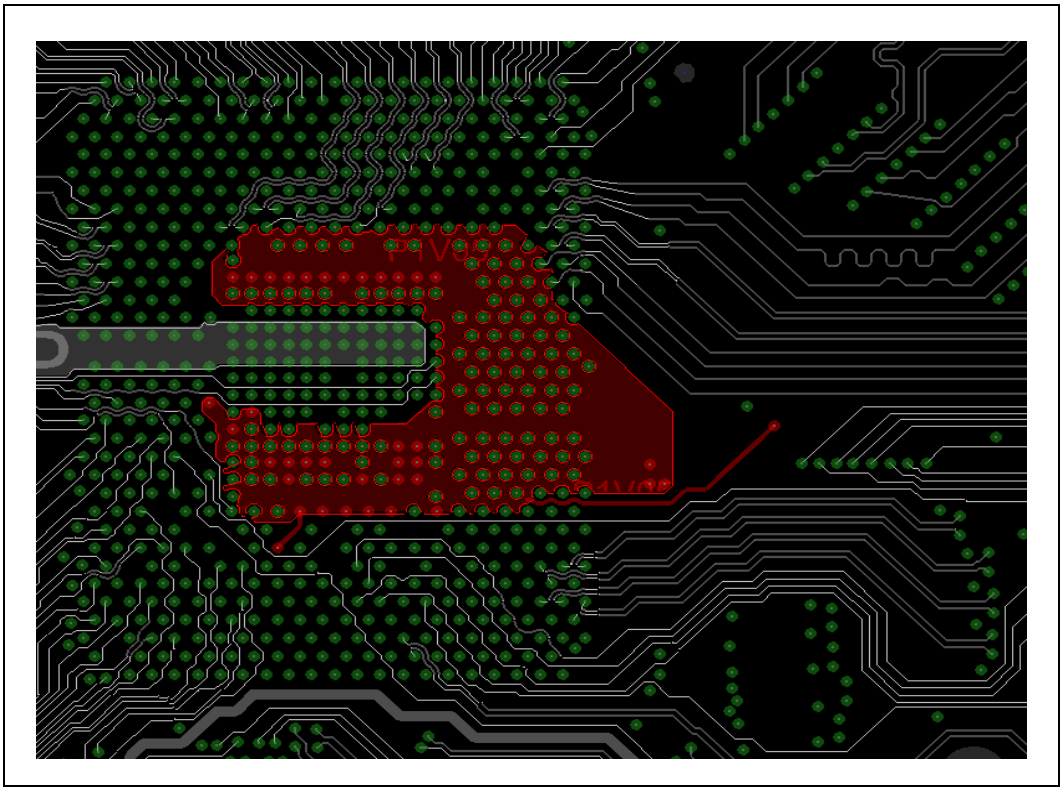


Figure 15-16. P1V05 VR VSense - VR_P1V05_FB_RR



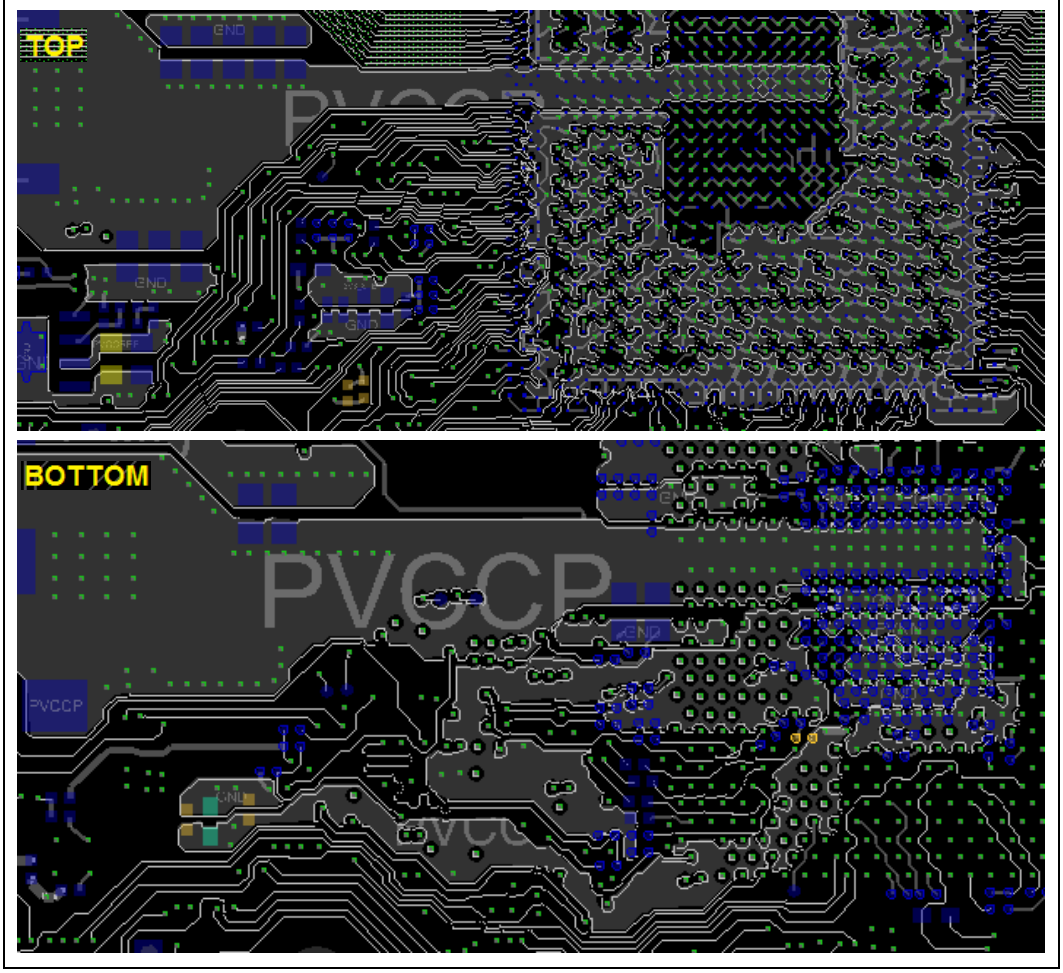
Note: The sense point should be placed in the SoC area.

15.4.5 PVCCREF VR Decoupling Recommendations

Table 15-10. PVCCREF VR Bulk/Decoupling Caps based on CRB PLACEHOLDER

Cap Value	Min Quantity per VR	Notes
22uF / 6.3V / 20% / X5R / 0805	1	Place close to VR output (yellow pads)
10uF / 6.3V / 20% / X5R / 0603	1	Place as close as possible to the SoC (blue pads)
1uF / 10V / 10% / X5R / 0402	5	Place as close as possible to the SoC (ocher pads)

Figure 15-17. PVCCREF Decoupling Capacitors



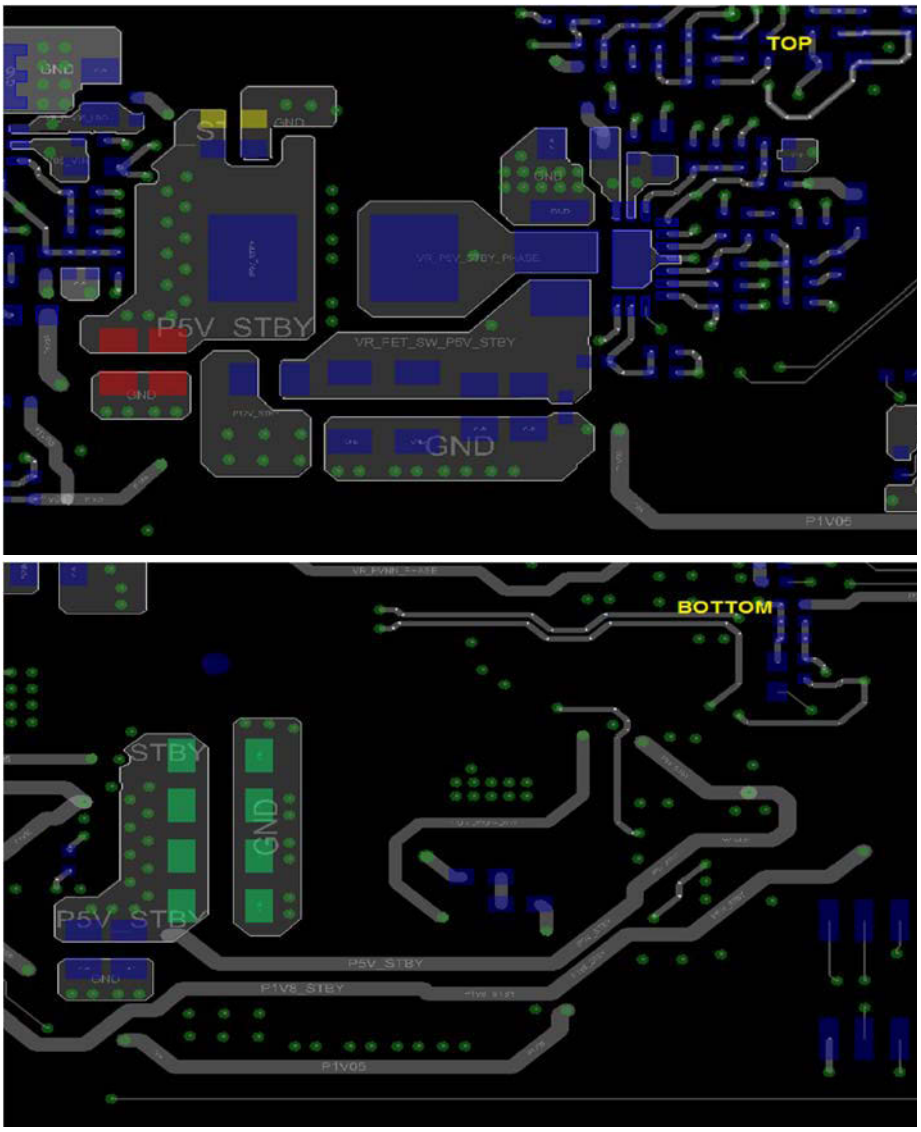
15.4.6 P5V_STBY VR Decoupling Recommendations

The P5V_STBY VR provides power to the USB 2/3 operation and other board functionality. This converter is on in S5. This voltage is supplied by a **12 V to 5.0 V_{OUT} VRD converter**, one VR per board. The VR has local sensing.

Table 15-11. P5V_STBY VR Bulk/Decoupling Caps based on CRB PLACEHOLDER

Cap Value	Min Quantity per VR	Notes
100uF / 10V / 20% / X5R / 1206	4	Bulk, place close to VR output inductor (green pads)
22uF / 10V / 20% / X5R / 0805	2	Place close to VR output inductor (red pads)
0.1uF / 25V / 10% / X7R / 0603	1	Place close to VR output inductor (yellow pads)

Figure 15-18. P5V_STBY Decoupling Capacitors



15.4.7 P3V3_STBY VR Decoupling Recommendations

The P3V3_STBY VR provides power to VCCFHVIFPSI0_3P3, VCCPADXXXSI0_3P3, VCCUSBSUS_3P3 power rails, Flash, and CPLD devices on the CRB. This P3V3_STBY VR voltage is supplied by a **12 V to 3.3V V_{OUT} VRD converter**, one VR per board. This VR has local sensing.

Table 15-12. P3V3_STBY VR Bulk/Decoupling Caps based on CRB PLACEHOLDER

Cap Value	Min Quantity per VR	Notes
47.0uF / 6.3V / 20% / X5R / 1206	2	Place close to VR output (red pads)
10uF / 6.3V / 20% / X5R / 0603	3	Place as close as possible to SoC (ocher pads)
1uF / 10V / 10% / X5R / 0402	2	Place as close as possible to SoC (blue pads)
1uF / 10V / 10% / X5R / 0402	1	Place on the bottom layer under the SoC (pink pads)
0.1uF / 16V / 10% / X7R / 0402	1	Place on the bottom layer under the SoC (yellow pads)

Figure 15-19. P3V3_STBY Decoupling Capacitors near the SoC

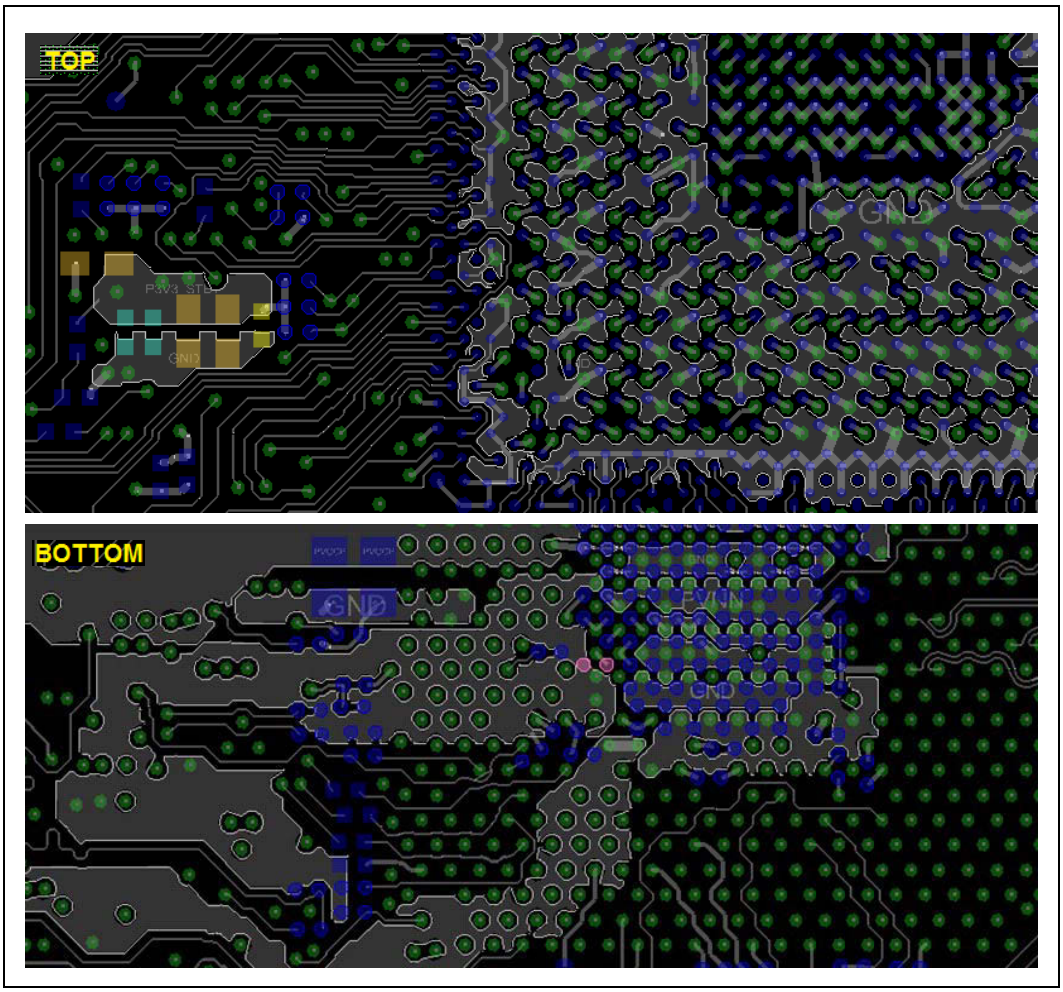
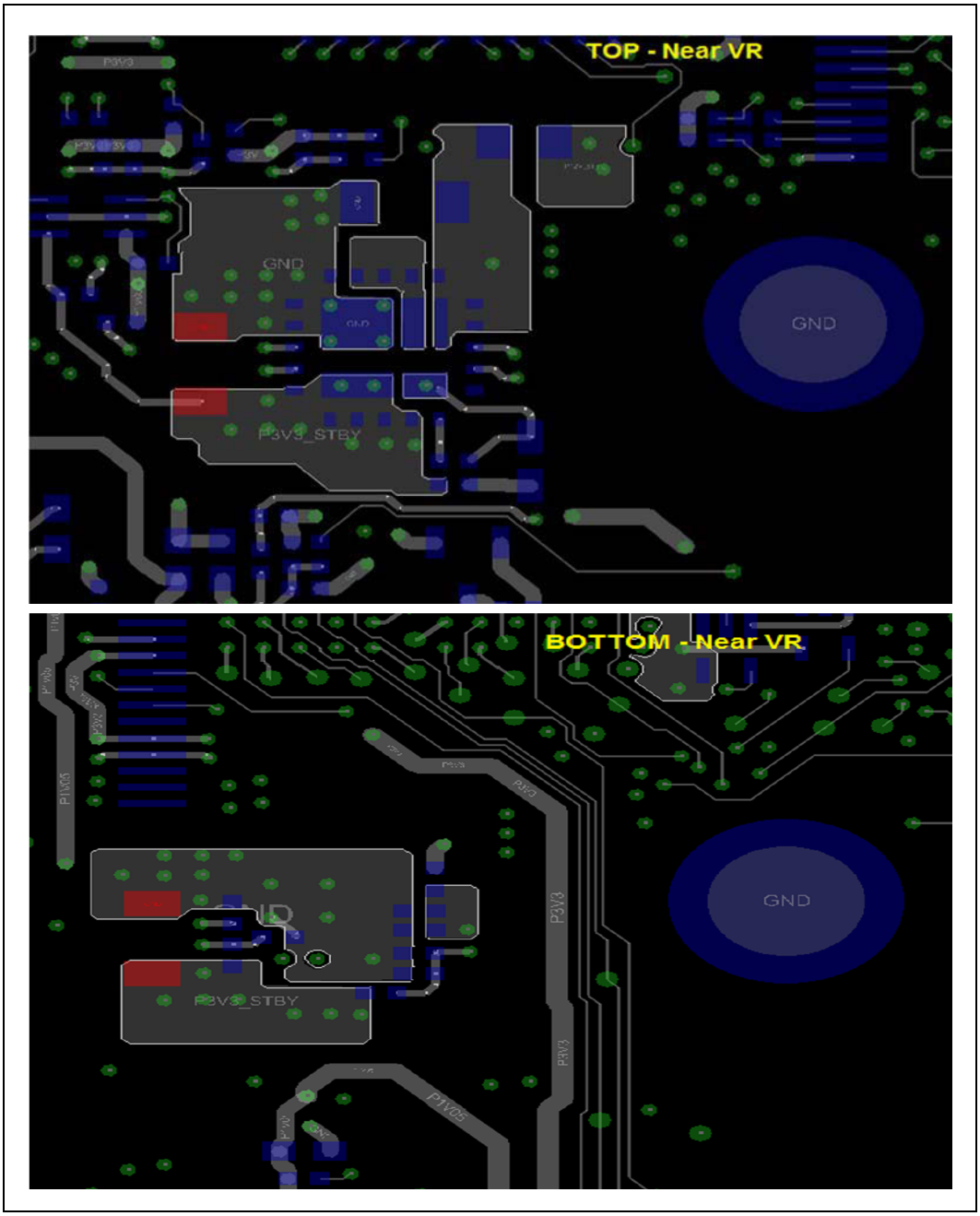


Figure 15-20. P3V3_STBY Decoupling Capacitors near the VR



15.5 SoC Voltage Regulator Output Guidelines

15.5.1 VCCP VR Sense Line and Decoupling Recommendations

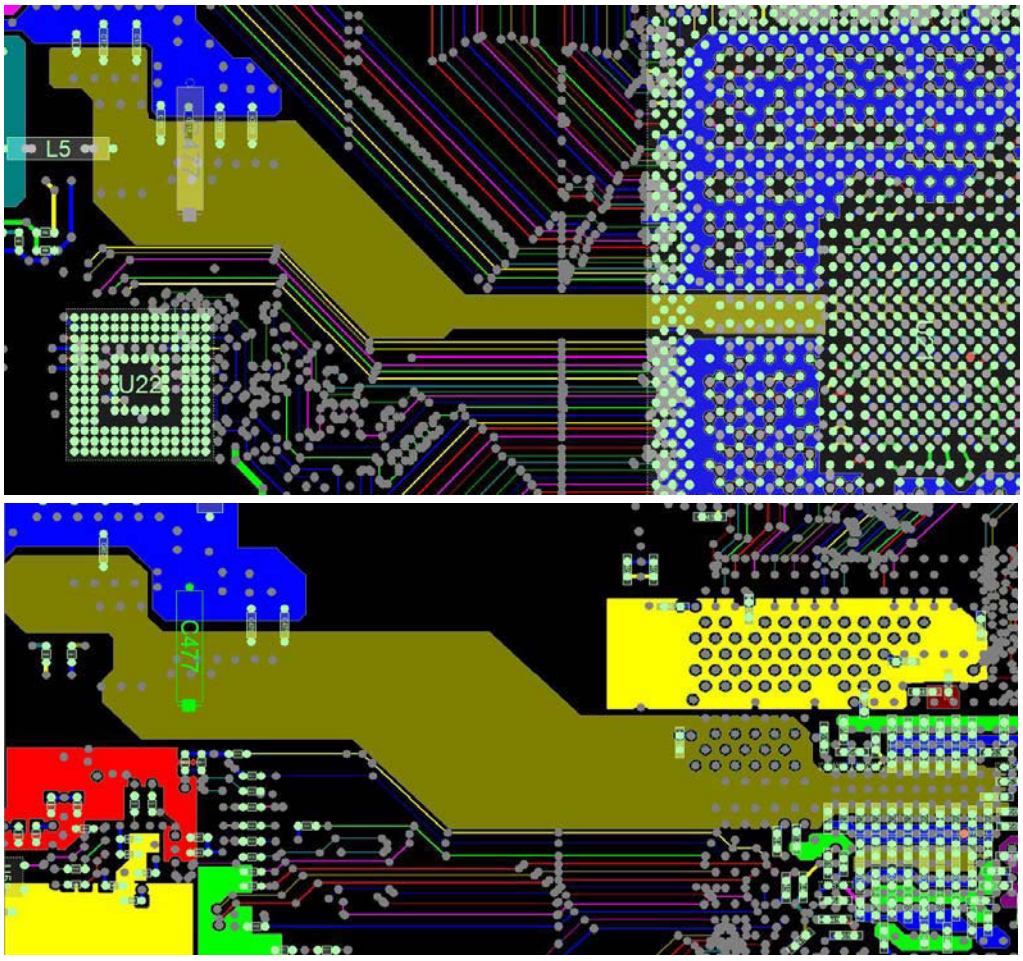
Refer to Section 15.4.1, "VCCP Voltage Regulator Output Guidelines" for details. The Pine Lake Platform specific differences are outlined below.

Table 15-13. SoC VCCP VR13-5mV Recommended Output Caps Per Interface

Cap Description	Min. Quantity	Notes
470 µF/ 2.0V / 20% / AL Polymer / 7343	1	Bulk, place close to VR output inductor.
47 µF / 6.3V / 20% / X5R / 0805	9	Place close to VR output inductor.
10 µF / 4V / 20% / X5R / 0402	20	Place on the bottom layer under the SoC.

Note: The above decoupling caps are the minimum recommended for the VR13-5 mV design used in the platform, but the designer should review their chosen VR topology and adjust the required caps accordingly for up to and including repeated 1 MHz step load frequency. Intel package decoupling has been selected to address frequencies above 1 MHz.

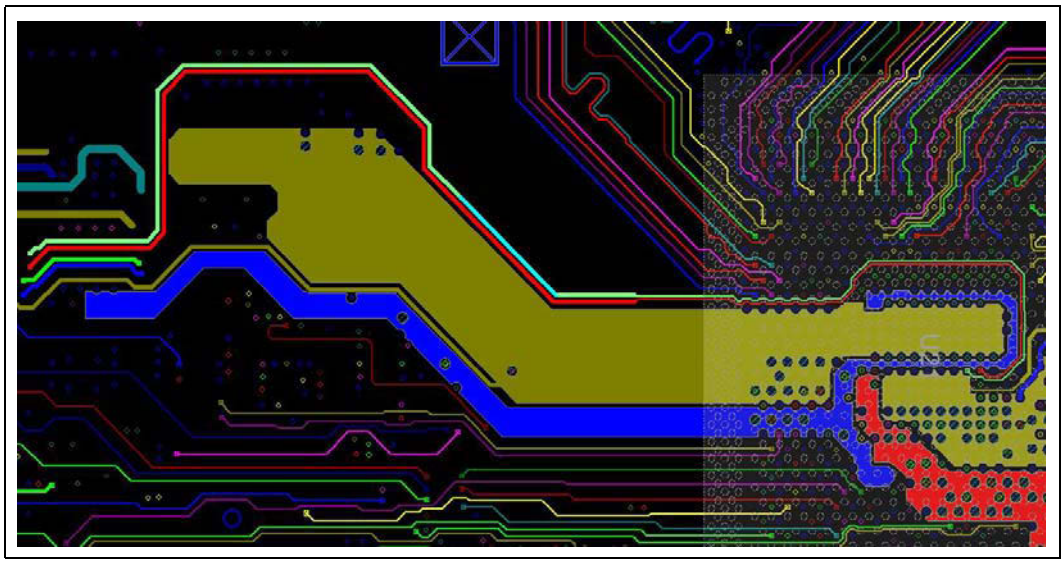
Figure 15-21. PVCCP VR Decoupling Capacitors (Top and Bottom)



15.5.1.1 Remote Sense Connection

Refer to Section 15.4.1.1, "Remote Sense Connection" for details.

Figure 15-22. VCCP_VSENSE_P and VCCP_VSENSE_N Line Routing for Reference (Green and Red Traces - Layer4)



15.5.1.2 General Motherboard Power Delivery Design Guide

Refer to Section 15.4.1.2, "General Motherboard Power Delivery Design Guide" for details.

15.5.2 VCCSRAM VR Sense Routing and Decoupling Recommendations

On a VRM, the positive sense line will be connected to SENSE_VCCRAMCPU_S0, and the negative sense line will be connected to SENSE_VSSRAMCPU_S0.

Figure 15-23. VCCSRAM_VSENSE_N and VCCSRAM_VSENSE_P Line Routing for Reference (Red and Violet Traces)

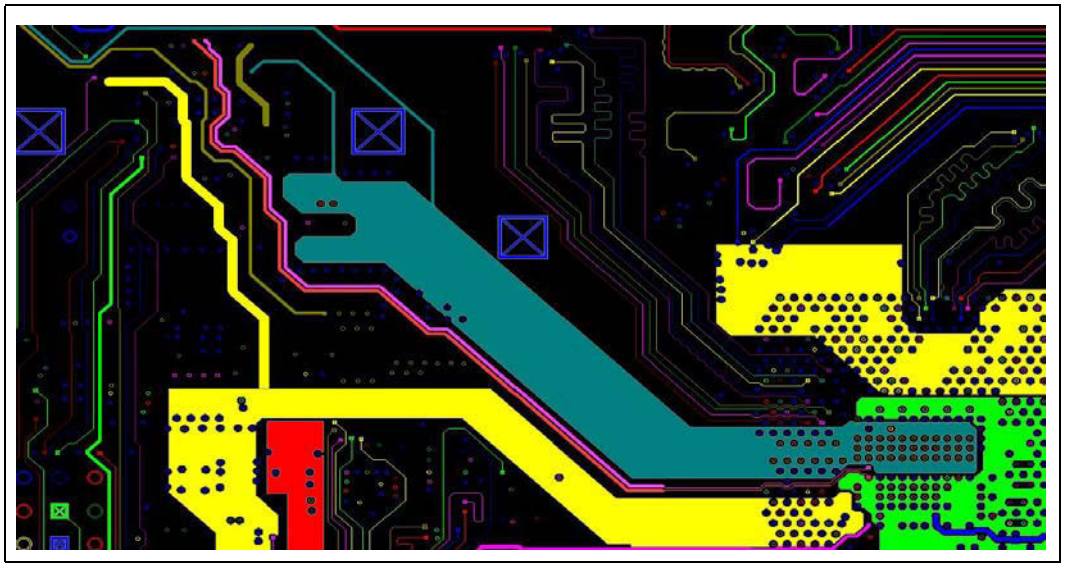
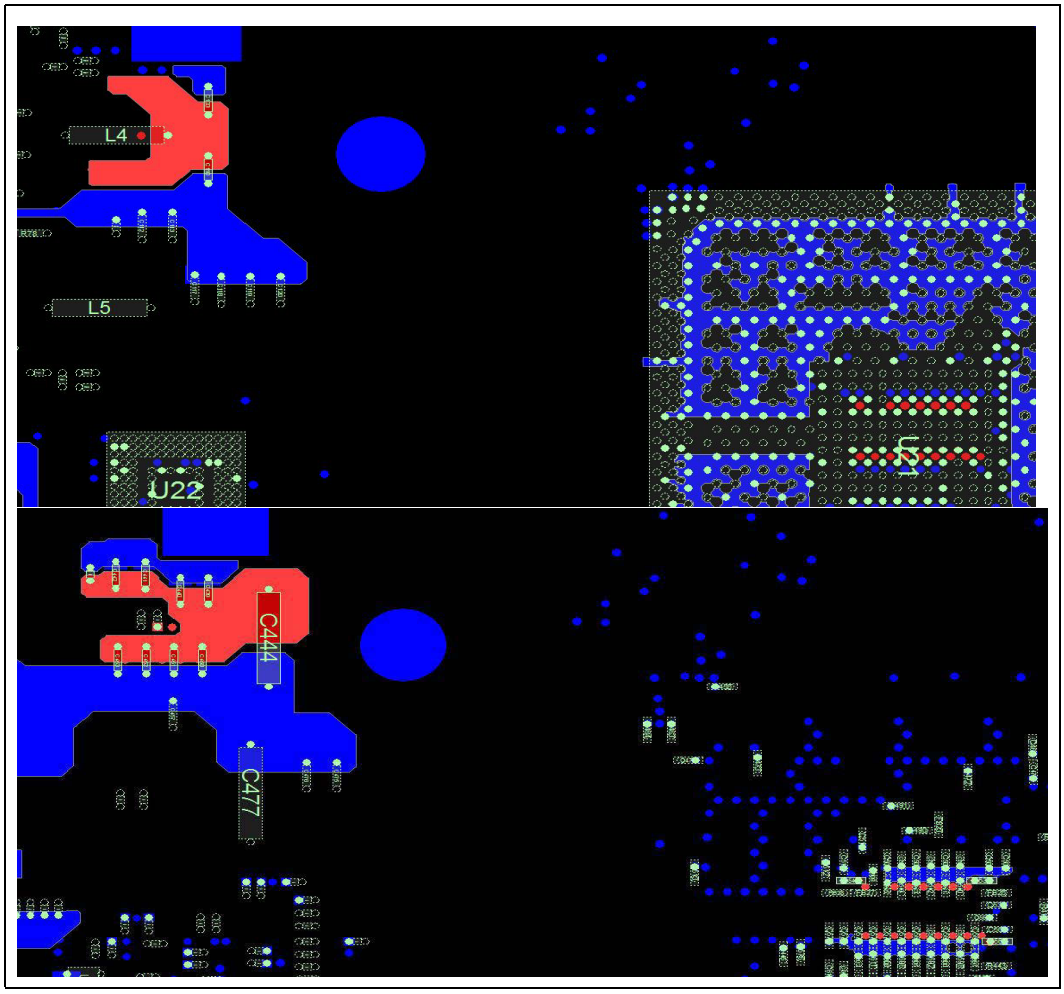


Table 15-14. VCCSRAM VR Bulk/Decoupling Caps Based on the Pine Lake Platform

Cap Value	Min. Quantity per VR	Notes
22 µF / 6.3V / 20% / X5R / 0805	5	Place close to VR output inductor.
2.2 µF / 6.3V / 20% / X5R / 0402	2	Place on the bottom layer under the SoC.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on the bottom layer under the SoC.

Figure 15-24. VCCSRAM VR Decoupling Capacitors (Top and Bottom)



15.5.3 VNN VR Sense Line and Decoupling Recommendations

Table 15-15. PVNN VR Bulk/Decoupling Caps

Cap Value	Min. Quantity per VR	Notes
470 µF / 2.0V / 20% / ALUM / 7343	1	Bulk, place close to VR output inductor.
47 µF / 6.3V / 20% / X5R / 0805	3	Place close to VR output inductor.
22 µF / 6.3V / 20% / X5R / 0805	5	Place close to VR output inductor.
22 µF / 6.3V / 20% / X5R / 0603	1	Place close to VR output inductor.
10 µF / 16V / 10% / X5R / 0805	7	Place close to VR output inductor.
1 µF / 4V / 20% / X5R / 0201	7	Place on bottom layer under the SoC.

Figure 15-25. VNN Decoupling Capacitors (Top Left - VR Bottom, Top Right - VR Top, and Bottom Image - SoC Bottom)

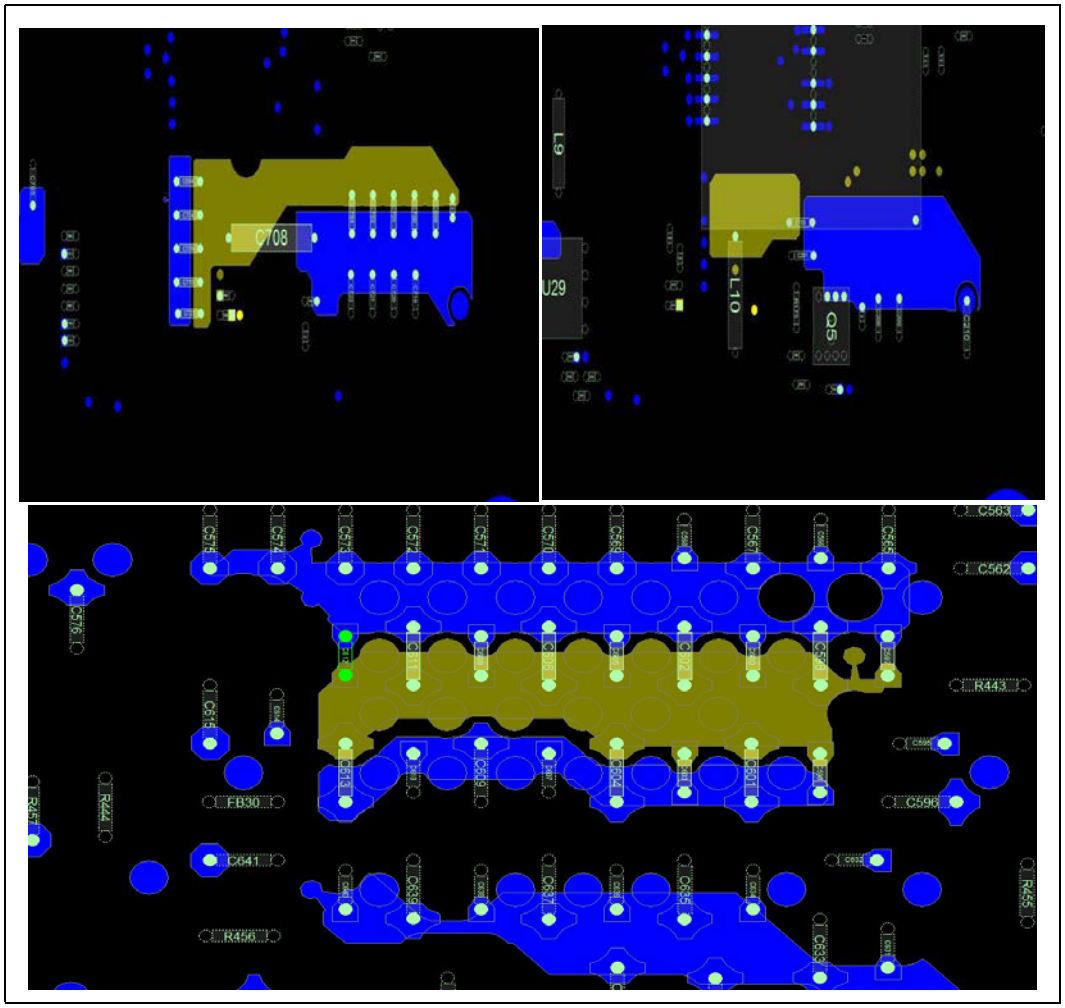
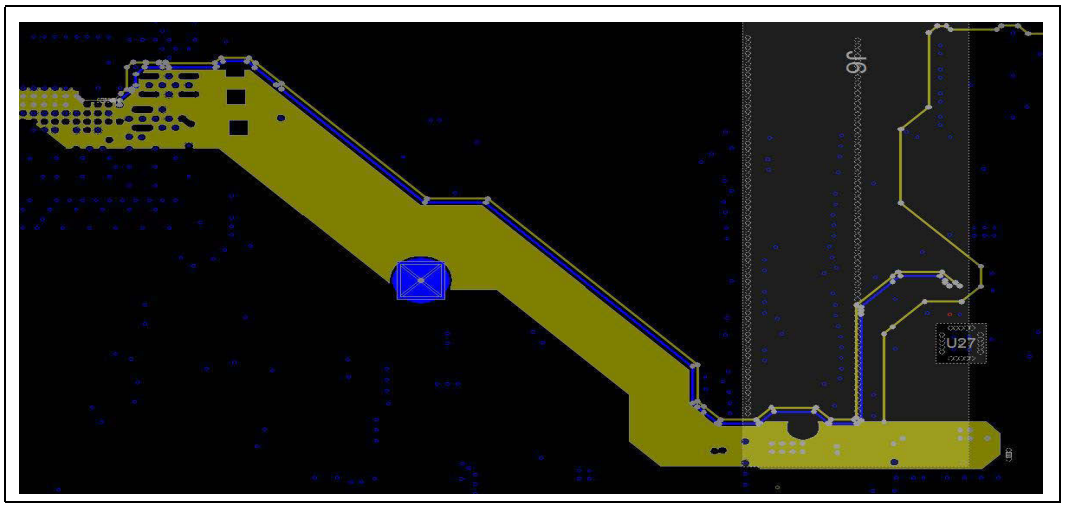


Figure 15-26. VNN VR VSense - Sense Across One of the SoC Decoupling Caps, Very Close to the SoC



Note: The sense point should be placed in the SoC area (upper left).

15.5.4 V1P05 VR VSense and Decoupling Recommendations

Table 15-16. V1P05 VR Bulk/Decoupling Caps Based on the CRB

Cap Value	Min. Quantity per VR	Notes
470 µF / 2V / 20% / ALUM / SM	2	Bulk, place close to VR output inductor.
47µF / 6.3V / 20% / X5R / 0805	6	Place close to VR output inductor.
22 µF / 6.3V / 20% / X5R / 0603	2	Place close to VR output inductor.
47 µF / 6.3V / 20% / X5R / 0603	10	Place close to VR output inductor.
10 µF / 4.0V / 20% / X5R / 0402	16	Place close to VR output inductor.
1 µF / 4V / 20% / X5R / 0201	11	Place on bottom layer under the SoC.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on bottom layer under the SoC.

Figure 15-27. V1P05 Decoupling Capacitors (VR Top, VR Bottom and SoC Bottom)

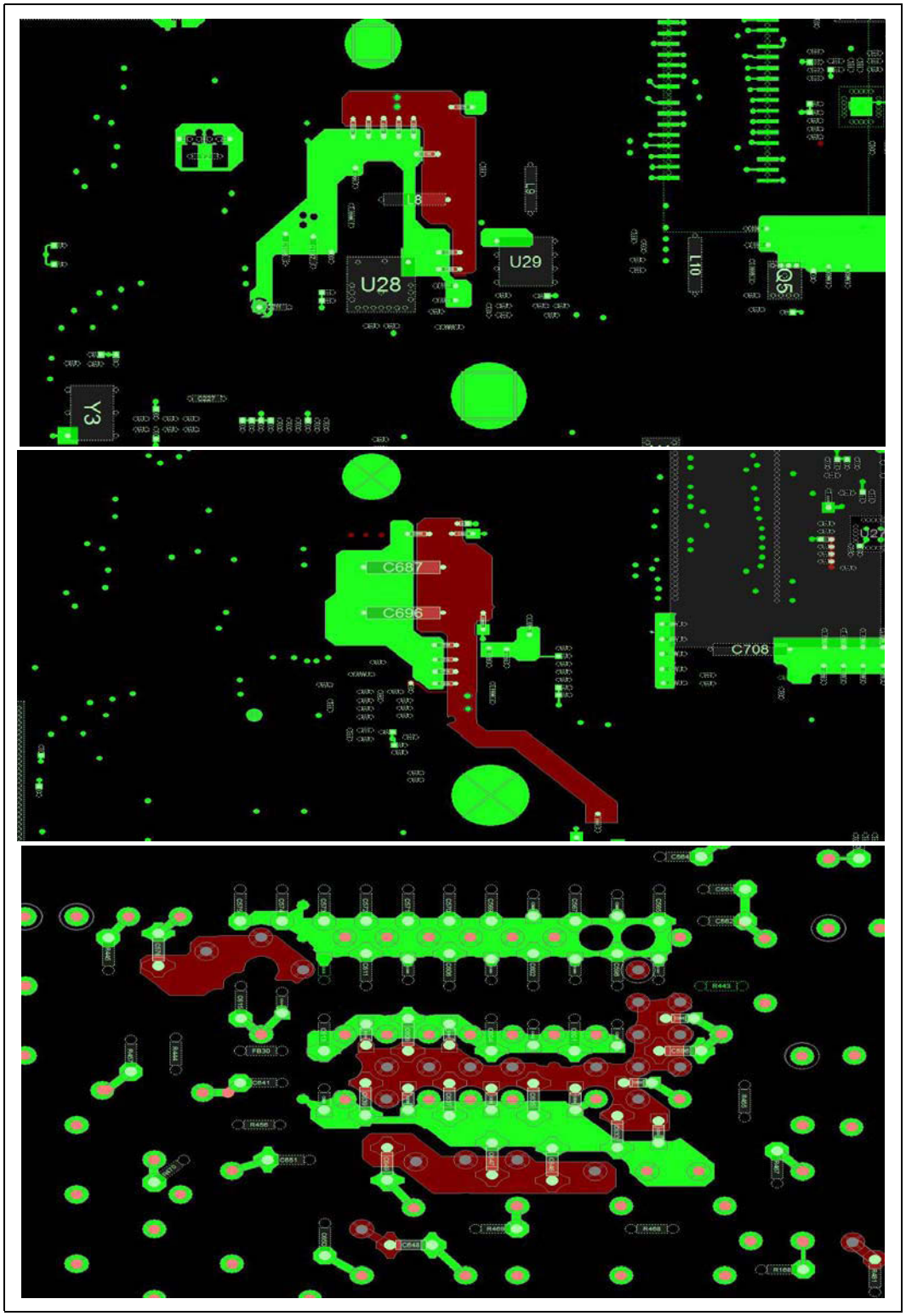
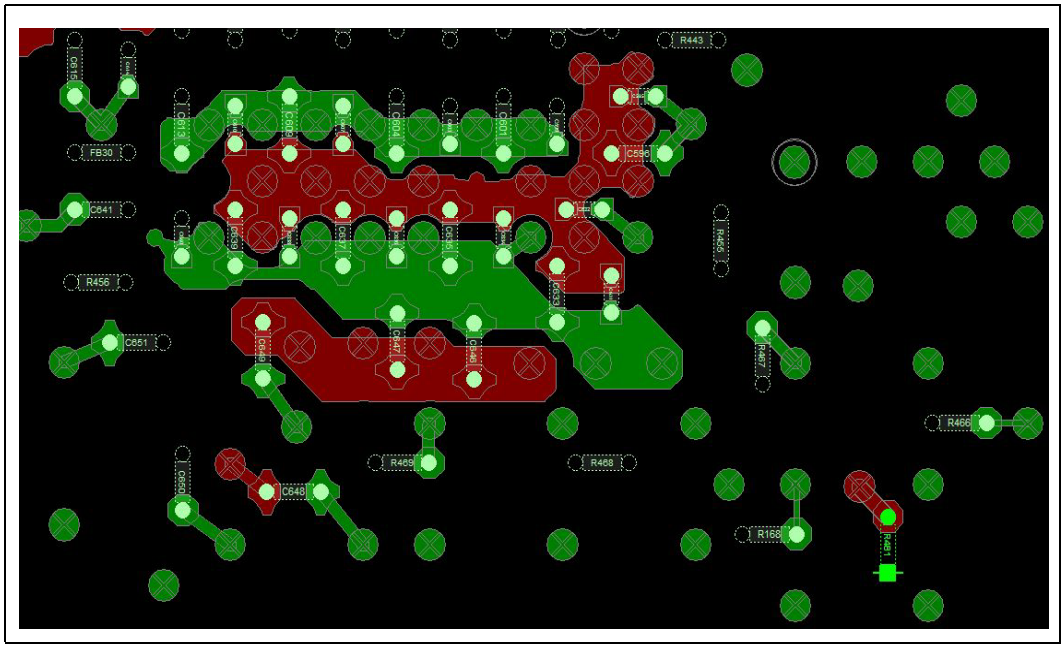


Figure 15-28. V1P05 VR VSense - Sense Across R481



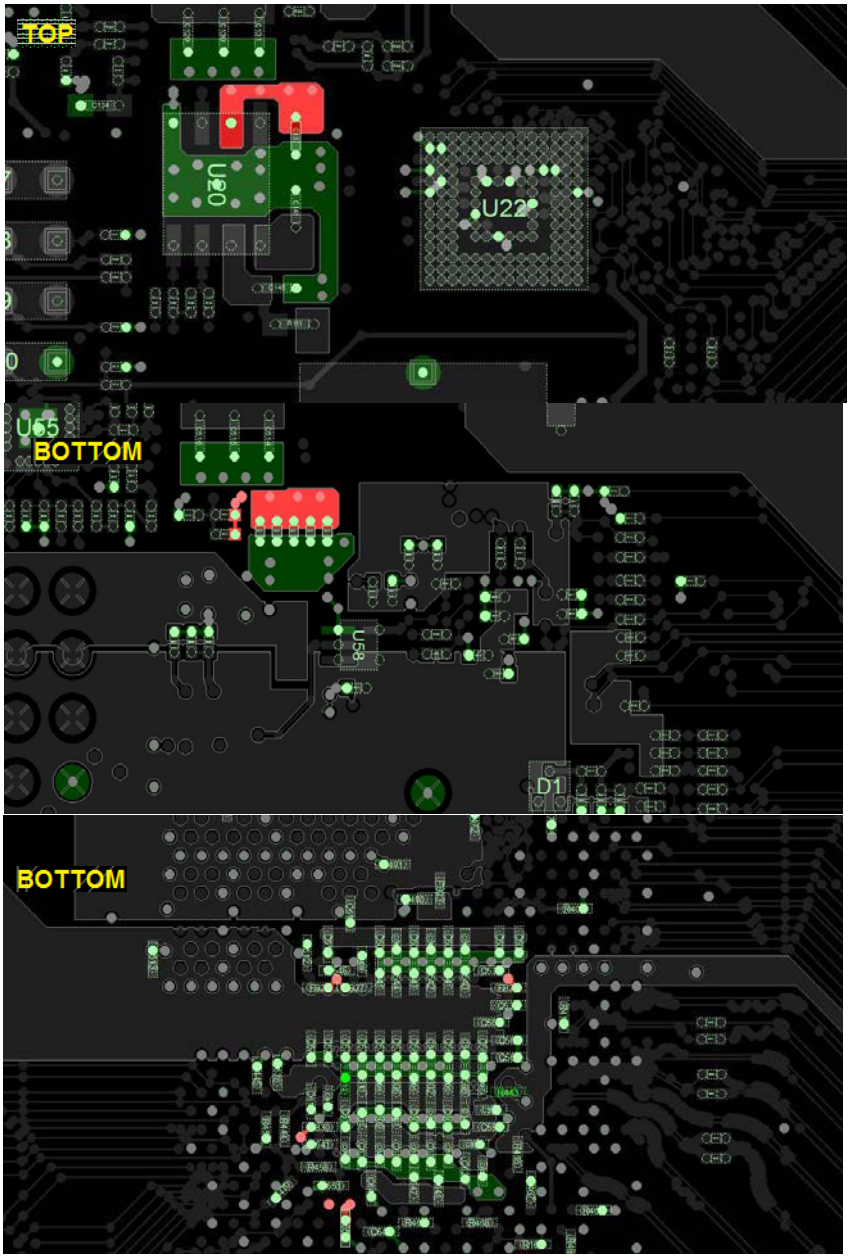
Note: Optimal placement of the V1P05 VSense.

15.5.5 VCCREF VR Decoupling Recommendations

Table 15-17. VCCREF VR Bulk/Decoupling Caps Based on the CRB

Cap Value	Min. Quantity per VR	Notes
10 µF / 6.3V / 20% / X5R / 0603	1	Place close to VR output.
10 µF / 4.0V / 20% / X5R / 0402	1	Place close to VR output.
1 µF / 6.3V / 20% / X5R / 0402	4	Place close to VR output.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on bottom layer under the SoC.

Figure 15-29. VCCREF Decoupling Capacitors

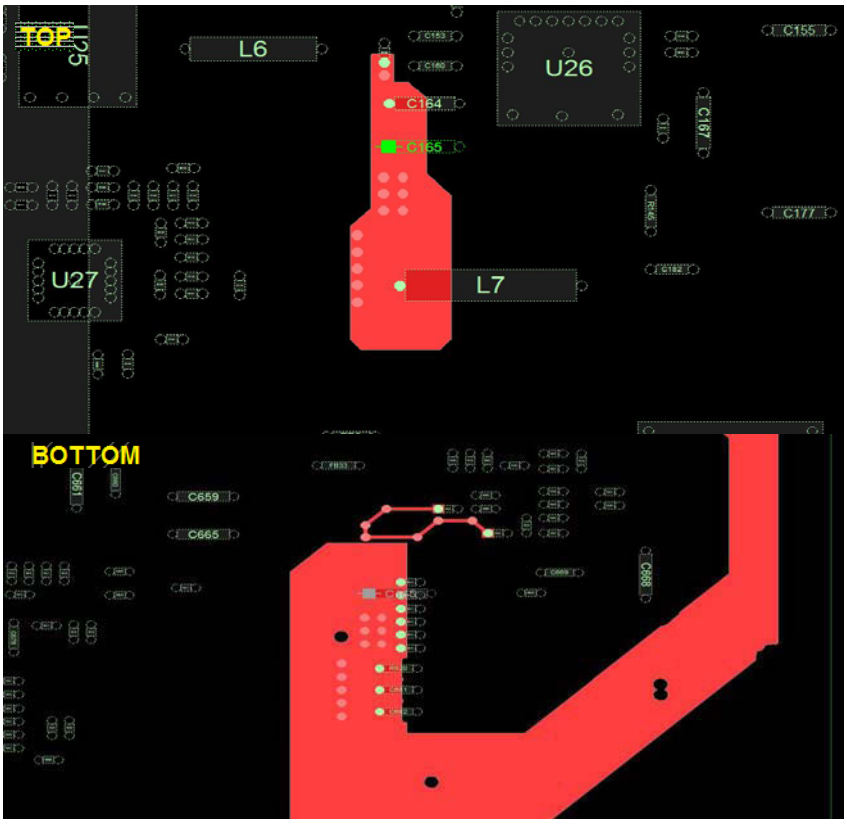


15.5.6 V3P3 VR Decoupling Recommendations

Table 15-18. V3P3 VR Bulk/Decoupling Caps

Cap Value	Min. Quantity per VR	Notes
100 µF / 6.3V / 20% / X5R / 1206	2	Place close to VR output inductor.
0.1 µF / 25V / 10% / X5R / 0402	2	Place close to VR output inductor.
10 µF / 4.0V / 20% / X5R / 0402	3	Place close to VR output inductor.
1 µF / 6.3V / 20% / X5R / 0402	2	Place close to VR output inductor.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on bottom layer under the SoC.

Figure 15-30. V3P3 Decoupling Capacitors

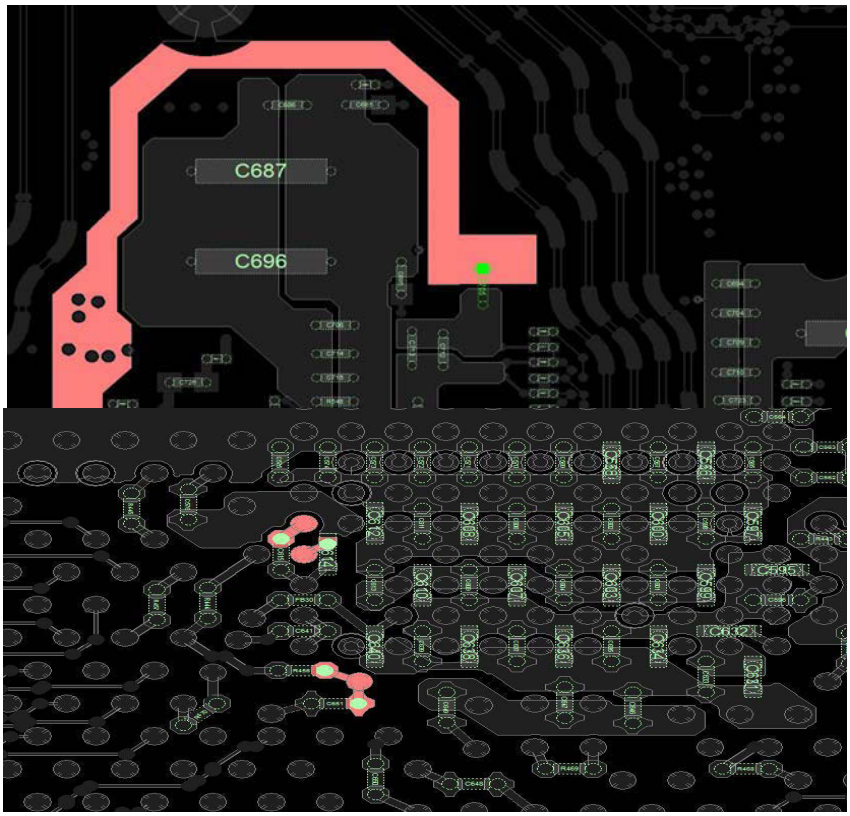


15.5.7 V1P8 VR Decoupling Recommendations

Table 15-19. V1P8 VR Bulk/Decoupling Caps

Cap Value	Min. Quantity per VR	Notes
22 µF / 6.3V / 20% / X5R / 0805	1	Place close to VR output inductor.
1 µF / 4.0V / 20% / X5R / 0201	1	Place on bottom layer under the SoC.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on bottom layer under the SoC.
1 µF / 6.3V / 20% / X5R / 0402	1	Place on bottom layer under the SoC.

Figure 15-31. V1P8 Decoupling Capacitors (Bottom VR and bottom SOC)



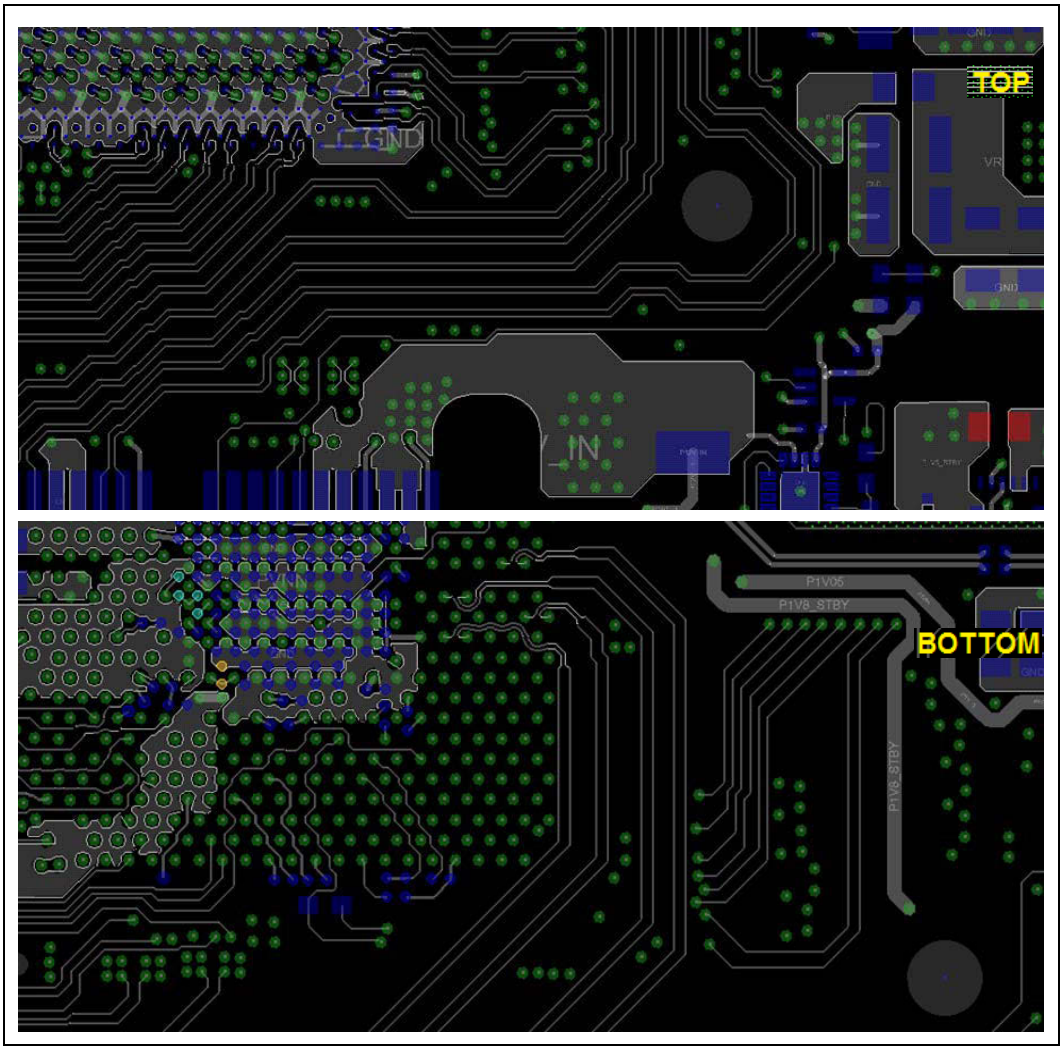
15.5.8 P1V8_STBY VR decoupling recommendations

The P1V8_STBY VR provides power to the eMMC and SATA controller on the CRB. This voltage is supplied by a **3.3V_STBY to 1.8V V_{OUT} VRD converter**, one VR per board. This VR has local sensing. Check SATA part datasheet for power pin configuration.

Table 15-20. P1V8 VR Bulk/Decoupling Caps based on CRB PLACEHOLDER

Cap Value	Min Quantity per VR	Notes
22uF / 6.3V / 20% / X5R / 0805	1	Place close to VR output (red pads)
10uF / 6.3V / 20% / X5R / 0402	1	Place on the bottom layer under the SoC (ocher pads)
1uF / 10V / 10% / X5R / 0402	1	Place on the bottom layer under the SoC (blue pads)
1uF / 4V / 20% / X6S / 0201	1	Place on the bottom layer under the SoC (blue pads)

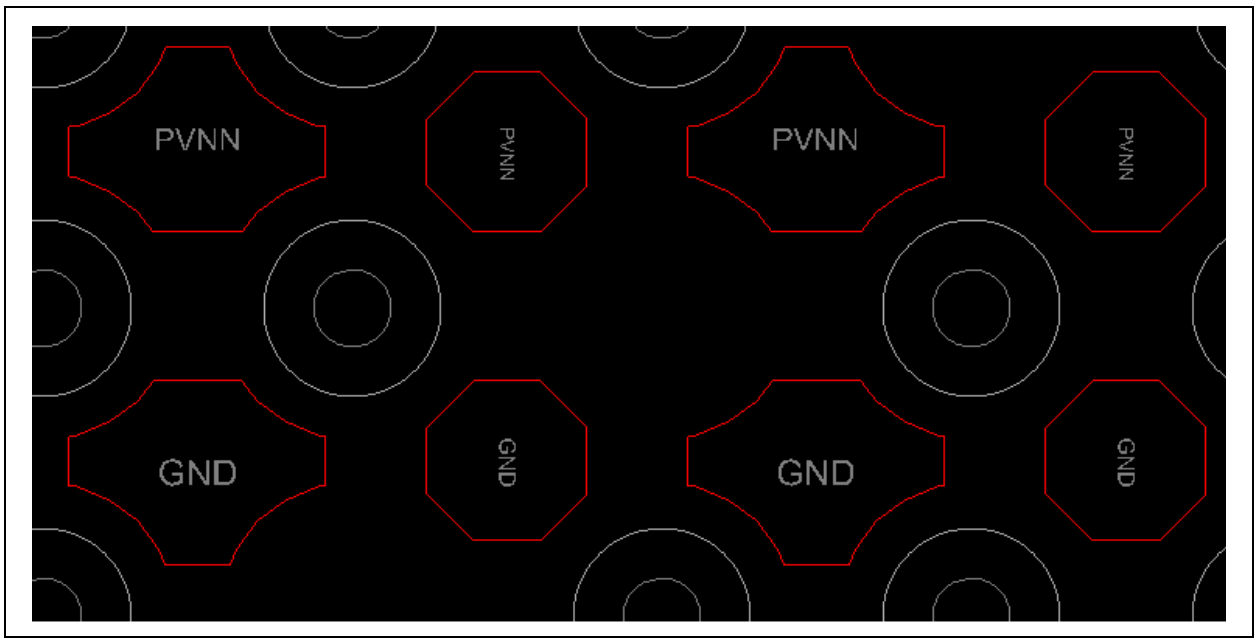
Figure 15-32. P1V8_STBY Decoupling Capacitors near the SoC



15.5.9 SoC Cavity Capacitors

The octagonal pads are too small to support typical 0402 capacitors without shorting out to the next capacitor. These pads are on the bottom level of all three Harrisonville CRBs and will be problematic for board builders.

The layout below, from Cormorant Lake, shows the bottom layer metal beneath the SoC.



There are two possible solutions.

1. Alternate the 0402 10 uF capacitors on the larger pads with 1 uF 0201 capacitors on the smaller octagonal pads. This was done on Aspen Cove. It allowed the minimum spacing of 11 mils to be met.
2. There are differences in size tolerance for 0402 capacitors. A 10 uF capacitor is larger than a 1 uF capacitor. See the snapshot of 0402 and 0201 tolerances.

TYPE	L_1 (mm)	W (mm)	T (MM)	L_2 / L_3 (mm) min.	L_2 / L_3 (mm) max.	L_4 (mm) min.
0201	0.6 ±0.03 (1) 0.6 ±0.05 (2)	0.3 ±0.03 (1) 0.3 ±0.05 (2)		0.10	0.20	0.20
0402	1.0 ±0.05 (1) 1.0 ±0.15 (2) 1.0 ±0.20 (3)	0.5 ±0.05 (1) 0.5 ±0.15 (2) 0.5 ±0.20 (3)	1 uF 10 uF	0.20	0.30	0.40
0603	1.6 ±0.10 (1) 1.6 ±0.15 (2) 1.6 ±0.20 (3)	0.8 ±0.10 (1) 0.8 ±0.15 (2) 0.8 ±0.20 (3)		0.20	0.60	0.40
0805	2.0 ±0.10 (1)	1.25 ±0.10 (1)	Refer to	0.25	0.75	0.55

For dimension see Table I

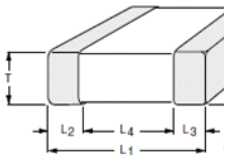
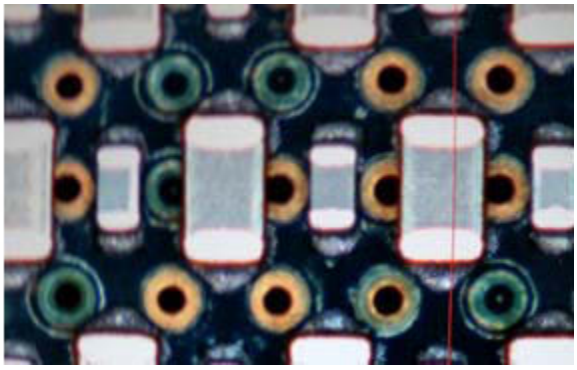


Fig. 2 Surface mount mul
ceramic capacitor

Alternating 0402, 10 uF and a 0201, 1 uF capacitors is recommended. If this is a problem, use the smaller 0402, 1 uF in place of the 0201.

A 7 mil spacing and better coverage with the solder paste mask will be achieved.



15.6 DDR4 DIMMs Power Delivery Guidelines

The Harrisonville platform CRB design.

The VDDQ VR is controlled with sVID (controlled by SoC).

Table 15-21. DDR4 DIMM Memory Power Supply Voltages per CRB

#	Power Rail	V_{IN}	V_{OUT} Nom	VR Type	VR Qty /board	Purpose
Aspen Cove CRB with DDR4						
1	VDDQ (PVDDR)	12V_stby	1.35V or 1.21V	switcher	1	DDR4 +SoC VDDR_01
2	PVTT	P1V2_VDDQ	1/2 VDDQ	source/sink linear	1	DDR4 DIMM VTT
3	PVPP	5V_stby	2.6V	switcher	1	DDR4 DIMM VPP

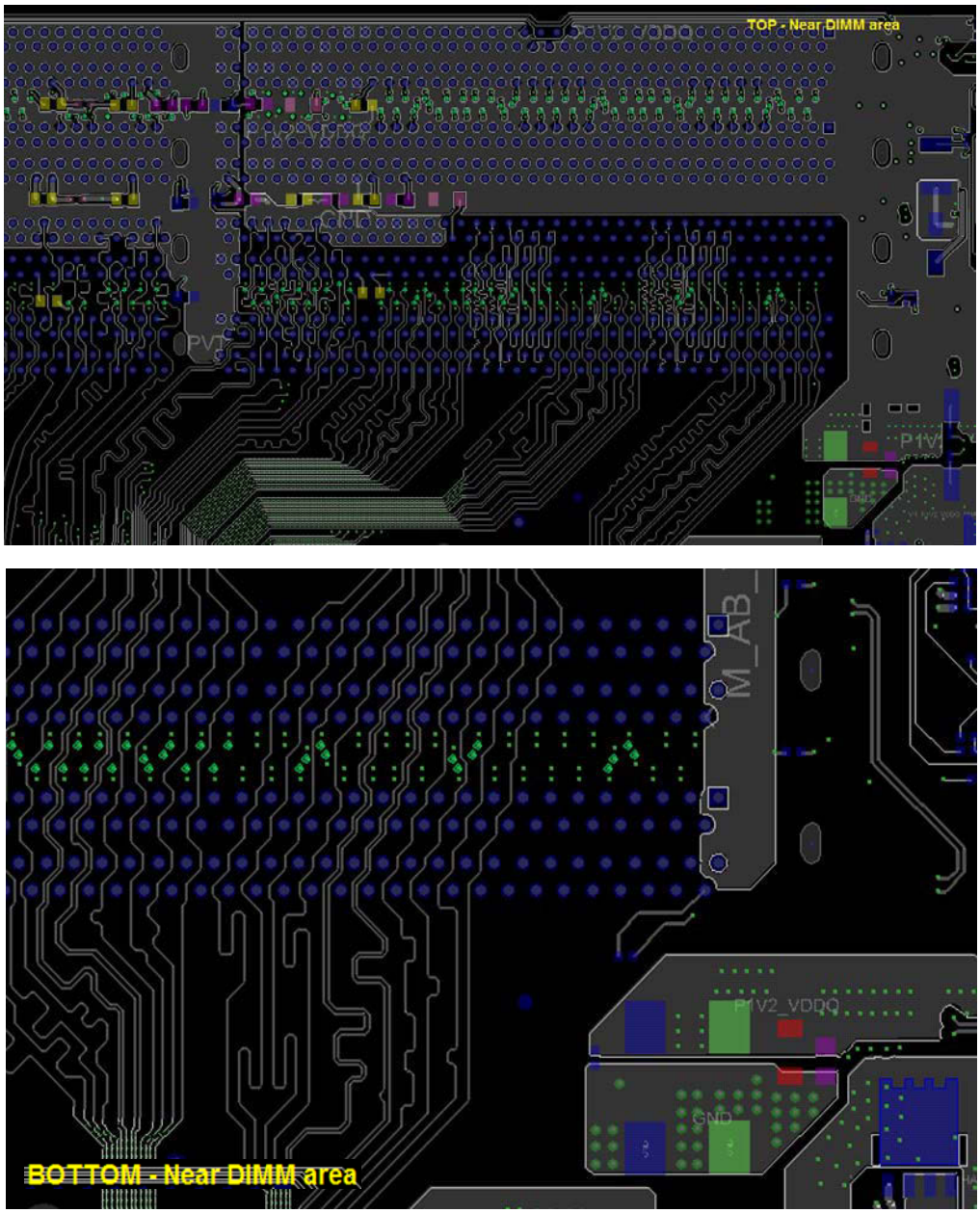
15.6.1 VDDQ (DDR4) VR Decoupling Recommendations

The Harrisonville platform VDDR supply provides power to the SoC VDDQ rail requirements. This voltage is supplied by a **12 V_STBY to 1.2 VDC out VRD13-5mV switching converter**, located in proximity to the SoC and DDR4 DIMM slots. This VR has its remote sense points terminated at a center point of the VDDQ plane, see the CRB VR placement. Each customer's VR design, layout and location of VR sense points may be more challenging, since multiple points-of-load must meet voltage regulation.

Table 15-22. PVDDQ (DDR4) VR Bulk/Decoupling Caps per CRB

Cap Value / Type	Min Quantity per VR	Notes
Beverly Cove CRB 4 DIMMs/VR		
470uF / 2.5V / 20% / ALUM / 3018	2	Bulk, place close to VR output inductor (green pads)
220uF / 4V / 20% / X5R / 1216	2	Bulk, place close to VR output inductor (red pads)
22uF / 6.3V / 20% / X5R / 0805	2	Place near DIMM area (purple pads)
47uF / 4V / 20% / X5R / 0805	9	Place near DIMM area (yellow pads)
47uF / 6.3V / 20% / X5R / 1206	2	Place near DIMM area (pink pads)
22uF / 6.3V / 20% / X5R / 0805	6	Place near DIMM area (purple pads)
22uF / 6.3V / 20% / X5R / 0603	2	Place near DIMM area (brown pads)
1uF / 10V / 10% / X5R / 0402	3	Place on bottom under SoC (ocher pads)
0.1uF / 16V / 10% / X7R / 0402	2	Place on bottom under SoC (blue pads)
2.2uF / 6.3V / 20% / X6S / 0402	2	Place on bottom under SoC (ocher pads)

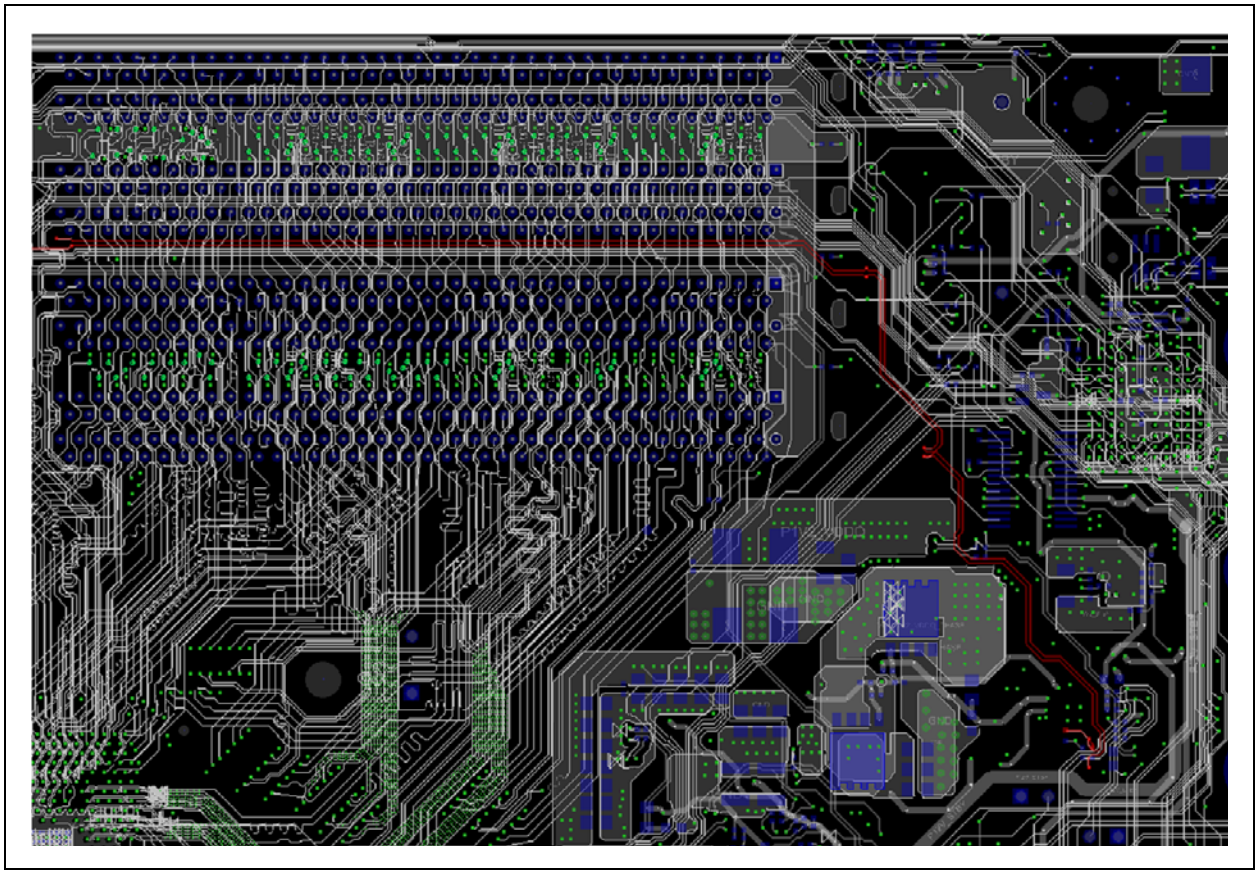
Figure 15-33. DDR4 DIMM Pin Field Capacitor Locations (VDDQ)



Additional VDDQ VR power delivery recommendations based on preliminary analysis:

1. VR sense point location should be terminated in the middle of the DIMM field for VDDQ, as depicted below.
2. Maximum VID shift should be +10 mV of nominal voltage. Not all designs will require an offset from VID.

Figure 15-34. VDDQ (DDR4) Remote Sense (Red Trace)



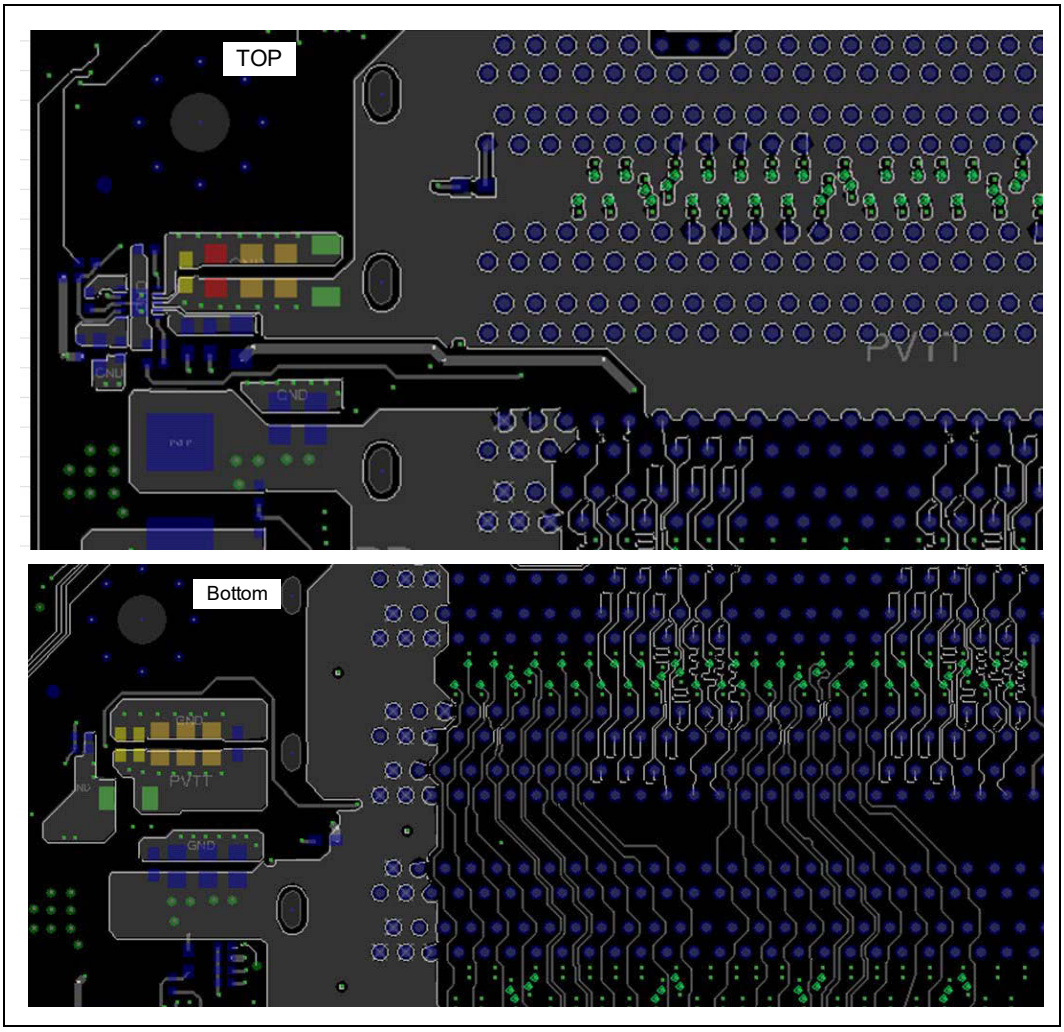
15.6.2 PVTT (DDR4) VR recommendations

The PVTT (Memory VTT or 0.5x VDDQ) VR provides linear power to VTT rails of DDR4 DIMMs.

Table 15-23. PVTT VR (DDR4) Bulk/Decoupling Caps per CRBs

Cap Value/ Type	Min Quantity per VR	Notes
Aspen Cove		
47uF / 4V / 20% / X5R / 0805	3	Place near DIMM area (blue pads)
22uF / 6.3V / 20% / X5R / 0805	1	Place close to VR output (red pads)
10uF / 6.3V / 20% / X5R / 0603	3	Place close to VR output (yellow pads)

Figure 15-35. DDR4 DIMM Pin Field Capacitor Locations (VTT)



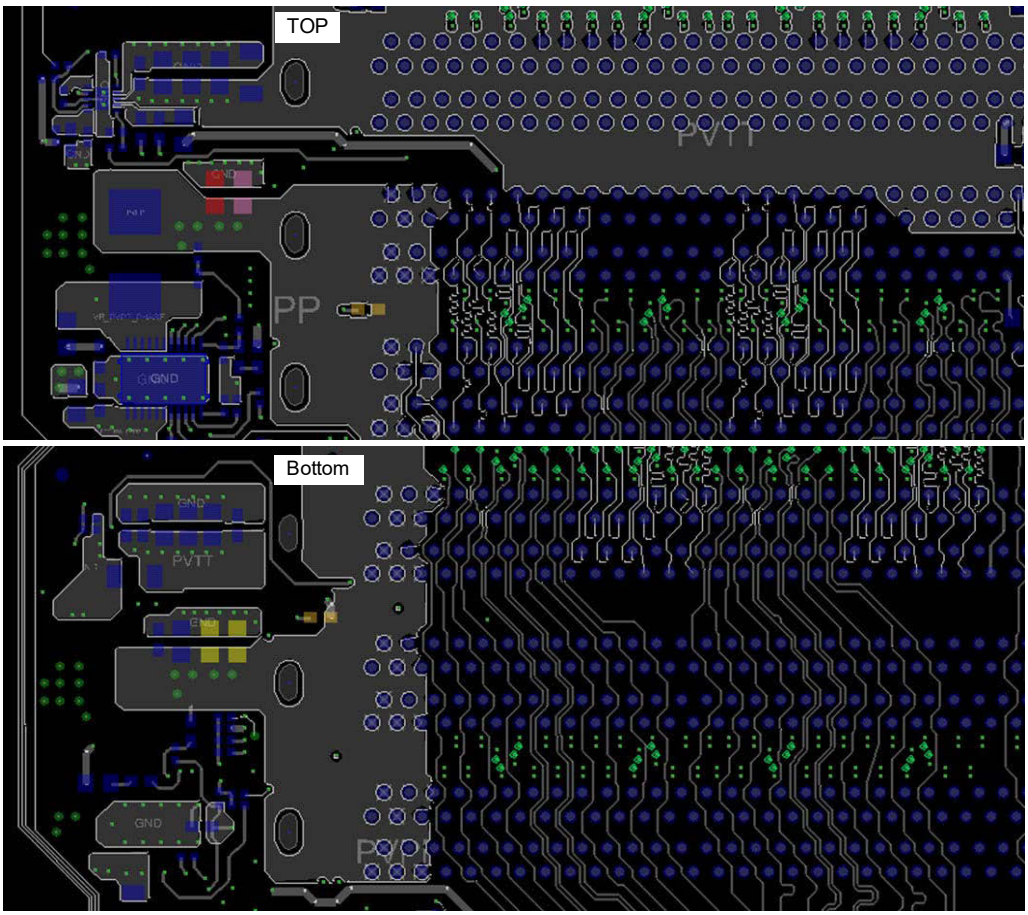
15.6.3 PVPP VR recommendations

The PVPP VR provides power to VPP rail of DDR4 DIMMs. This PVPP VR voltage is supplied by a **P5V0_STBY to 2.6 V_{OUT} VRD converter**, one VR for of the VPP rails.

Table 15-24. PVPP VR Bulk/Decoupling Caps based on CRB

Cap Value	Min Quantity per VR	Notes
Aspen Cove		
47uF / 4V / 20% / X5R / 0805	1	Place close to VR output inductor (red pads)
22uF / 6.3V / 20% / X5R / 0805	2	Place close to VR output inductor (yellow pads)
10uF / 6.3V / 10% / X5R / 0805	1	Place close to VR output inductor (pink pads)
10uF / 6.3V / 20% / X5R / 0603	1	Place close to VR inductor (blue pads)
10uF / 6.3V / 20% / X5R / 0603	3	Place near DIMM area (ocher pads)

Figure 15-36. DDR4 DIMM Pin Field Capacitor Locations (VPP)



15.7 Memory Power Delivery

Table 15-25. DDR4 Memory Power Supply Voltages

#	Power Rail	V_{IN}	V_{OUT} Nom	VR Type	VR Qty /board	Purpose
1	VDDQ_CPU_DDR	12V	1.2V	Switcher	1	DDR4 SO-DIMM + Memory Down + SoC
2	VTT_CPU_DDR	12V	1/2 VDDQ	Source/Sink Linear	1	DDR4 SO-DIMM + Memory Down
3	VPP_CPU_DDR	12V	2.6V	Switcher	1	DDR4 SO-DIMM + Memory Down

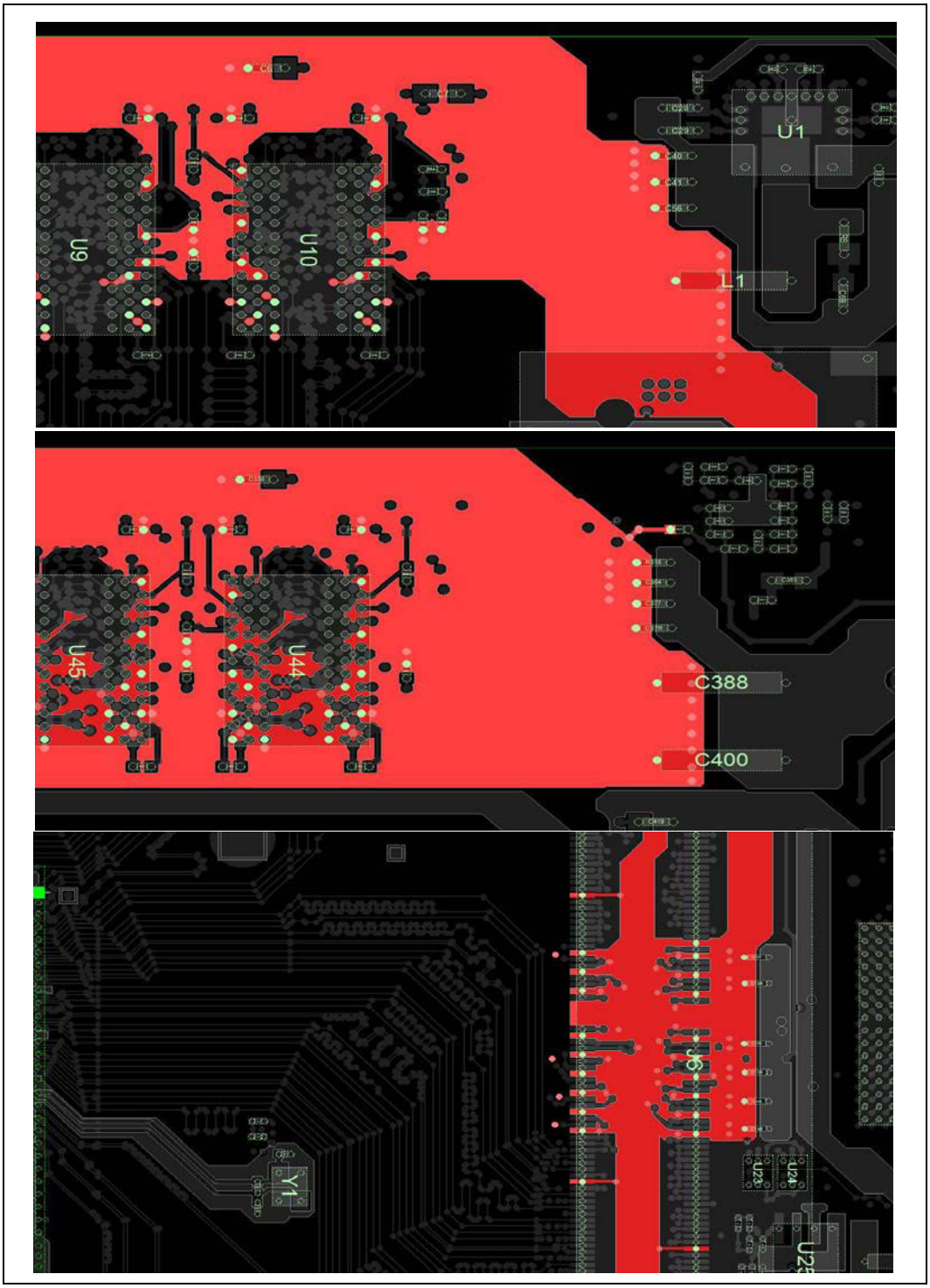
15.7.1 VDDQ (DDR4) VR Decoupling Recommendations

The Pine Lake VDDR supply provides power to the SoC VDDQ rail requirements. This voltage is supplied by a **12 V switching converter**, located in proximity to the SoC and DDR4 memory down/SO-DIMM. This VR has its remote sense points terminated at a center point of the VDDQ plane. See the CRB VR placement. Each customer's VR design, layout, and location of VR sense points may be more challenging, since multiple points-of-load must meet voltage regulation.

Table 15-26. PVDDQ (DDR4) VR Bulk/Decoupling Caps per CRB

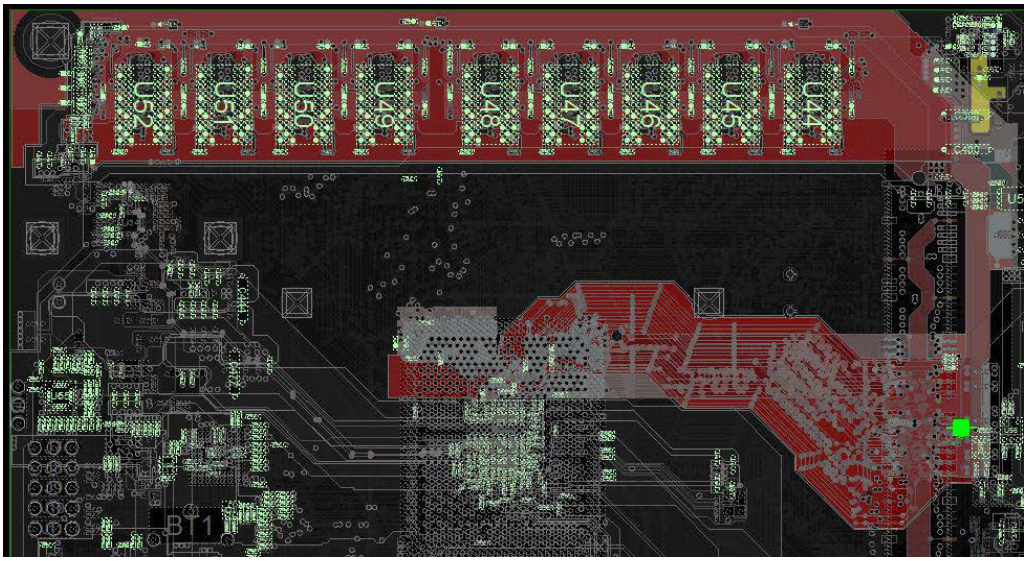
Cap Value / Type	Min Quantity per VR	Notes
470 µF/ 2.0V / 20% / AL Polymer / 7343	1	Place close to the VR output inductor.
47 µF / 6.3V / 20% / X5R / 0805	4	Place close to the VR output inductor.
2.2 µF / 6.3V / 20% / X5R / 0402	2	Place on the bottom layer under SoC.
1 µF / 6.3V / 20% / X5R / 0402	5	Place on the bottom layer under SoC.
0.1 µF / 25V / 10% / X7R / 0402	3	Place on the bottom layer under SoC.
1 µF / 6.3V / 20% / X5R / 0402	18	Place 1 close to every Memory Down chip.
0.1 µF / 25V / 10% / X7R / 0402	36	Place 2 close to every Memory Down chip.
22 µF / 6.3V / 20% / X5R / 0805	3	Place 3 close to every Memory Down chip.
47 µF / 6.3V / 20% / X5R / 0805	6	Place near to the DIMM and Memory Down.

Figure 15-37. VDDQ Memory Down Capacitor Locations (Top and Bottom Memory Down and Last SO-DIMM Top)



VR sense point location should be terminated in the middle of the SODIMM field for VDDQ, as depicted below.(green)

Figure 15-38. VDDQ_CPU_DDR sense point location



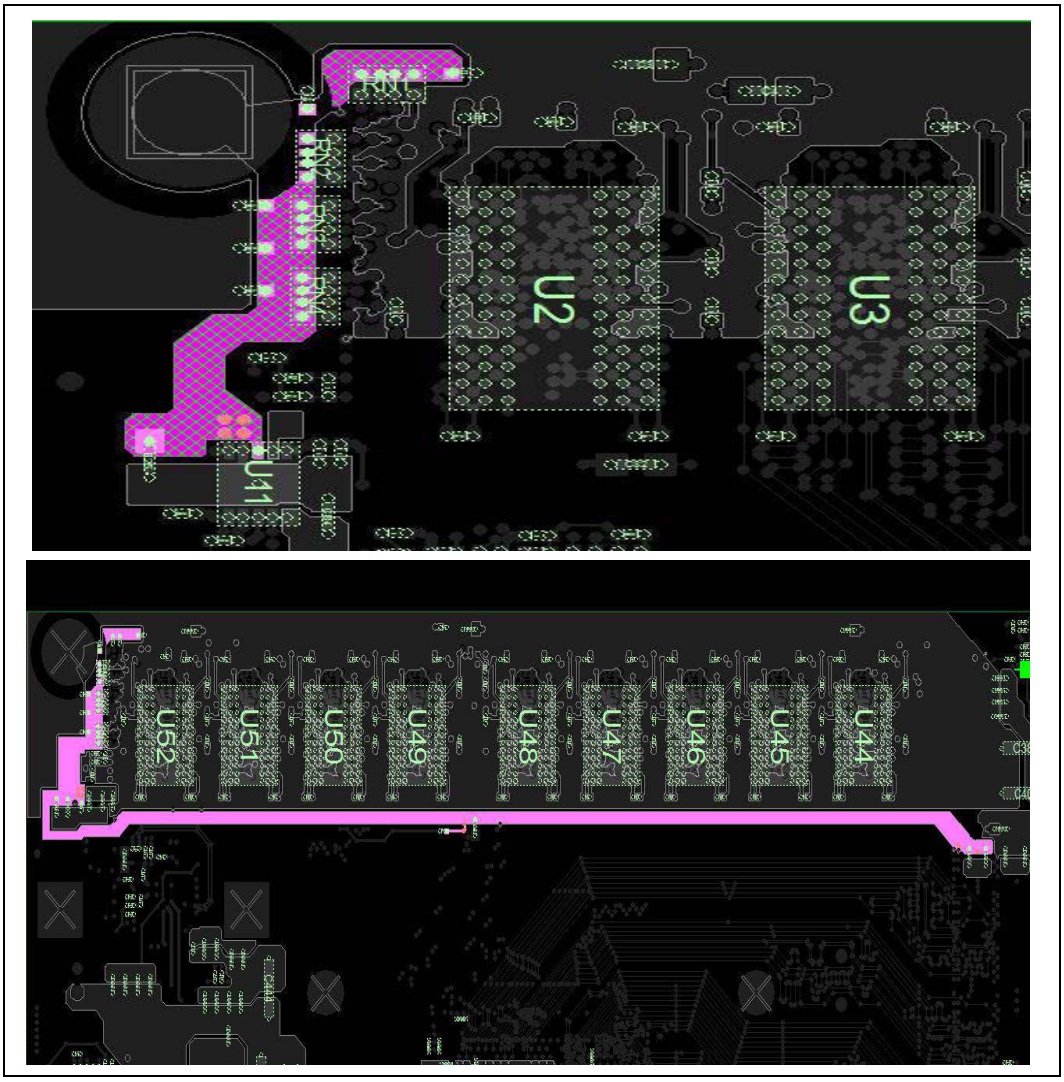
15.7.2 VTT_CPU_DDR (DDR4) VR recommendations

The VTT_CPU_DDR (memory VTT or 0.5x VDDQ) VR provides linear power to VTT rails of DDR4 SO-DIMM + memory down.

Table 15-27. VTT VR (DDR4) Bulk/Decoupling Caps per CRBs

Cap Value/Type	Min. Quantity per VR	Notes
10 µF / 6.3V / 20% / X5R / 0603	2	Place close to the VR output.
1000 pF / 50V / 10% / X7R / 0402	1	Place close to the VR output.
47 µF / 6.3V / 20% / X5R / 0805	1	Place close to the VR output.
47 µF / 6.3V / 20% / X5R / 0805	2	Place near to the DIMM and Memory Down.
0.1 µF / 25V / 10% / X7R / 0402	10	Place near to the memory down chip (between VTT and VDDQ).

Figure 15-39. VTT_CPU_DDR Decoupling Capacitor Locations (VTT)



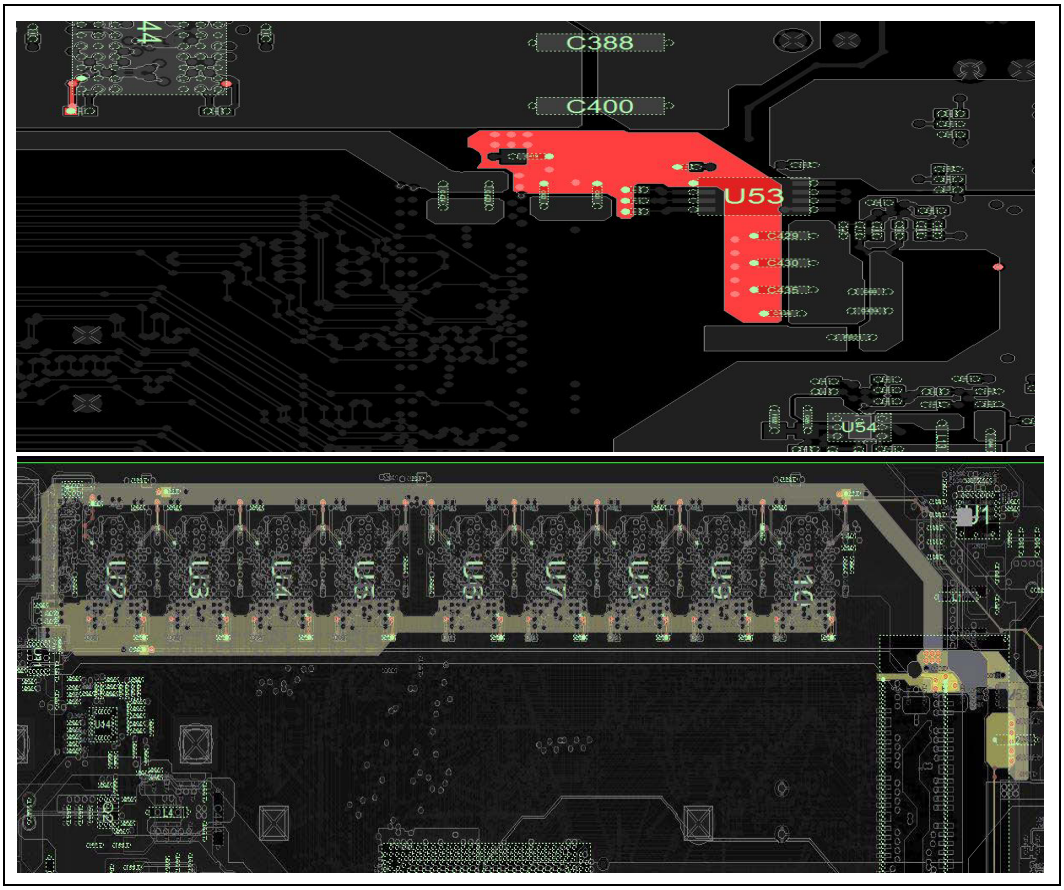
15.7.3 VPP VR Recommendations

The PVPP VR provides power to the VPP rail of the DDR4 DIMMs. This PVPP VR voltage is supplied by a **12 to 2.6 V_{OUT} VRD converter**, one VR for the VPP rails.

Table 15-28. VPP VR Bulk/Decoupling Caps based on CRB

Cap Value	Min. Quantity per VR	Notes
100 µF / 6.3V / 20% / X5R / 1206	2	Bulk, place close to the VR output inductor.
1 µF / 6.3V / 20% / X5R / 0402	18	Bulk, place close to every memory down chip.
0.1 µF / 25V / 10% / X7R / 0402	18	Bulk, place close to every memory down chip.
10 µF / 6.3V / 20% / X5R / 0603	3	Bulk, place close to every DIMM.

Figure 15-40. VPP_CPU_DDR Pin Field Capacitor Locations (VPP)



15.8 LC Filtering for Specific Applications

The table contains LC filtering information for specific applications that require different LC filtering than described in the rail sections above.

Table 15-29. LC Filtering per Specific Application

Vin	Vout	SoC pin	L (Inductor/Ferrite)	Capacitor
P1V05	PVCCPLL_KR_1P05	VCCKRLCPLL LAN0_RBIAS (through 1K resistor) LAN1_RBIAS (through 1K resistor)	INDCT, MTILAYER, 22.00nH, 1.85A, 0805, 10.00% Recommended: MPN: MLH2012F22NK (TDK CORPORATION OF AMERICA)	CAPC, X5R, 0805, 47.00UF, 4.00V, +/- 20% Recommended: MPN: GRM219R60G476ME44D (MURATA ELEC. NORTH AMERICA)
P1V05	PVCCDIGICKSI0_1P05	PVCCDIGICKSI0_1P05	INDCT, WWOUND, 5.6nH, 750.00mA, 0603, 0.2%,\ Recommended: MPN: LQW18AN5N6C00 (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0805, 47.00UF, 4.00V, +/- 20% Recommended: MPN: GRM219R60G476ME44D (MURATA ELEC. NORTH AMERICA)
P1V2_VDDQ	PVCCSFRPLLDDR	VCCDDRSFR_VDDQ	FER-BEAD, 0402, 120.0 OHM, 200.1 MA, +/- 2% Recommended: MPN: BLM15AG121SN1D (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0402, 10UF, 6.3V, +/- 20% Recommended: MPN: GRM155R60J106ME11D (MURATA ELEC. NORTH AMERICA
PVCCREF	PVCCREF_SFRXXXSIO_N	VCCREF_SFRXXXSI0_N	FER-BEAD, 0402, 120.0 OHM, 200.1 MA, +/- 2% Recommended: MPN: BLM15AG121SN1D (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0402, 1.0UF, 10V, +/- 10% Recommended: MPN: GRM155R61A105KE15D (MURATA ELEC. NORTH AMERICA
PVCCREF	PVCCREF_DTS_W	VCCREF_DTS_W	FER-BEAD, 0402, 120.0 OHM, 200.1 MA, +/- 2% Recommended: MPN: BLM15AG121SN1D (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0402, 1.0UF, 10V, +/- 10% Recommended: MPN: GRM155R61A105KE15D (MURATA ELEC. NORTH AMERICA
PVCCREF	PVCCREF_SFRXXXSIO_S	VCCREF_SFRXXXSIO_S	FER-BEAD, 0402, 120.0 OHM, 200.1 MA, +/- 2% Recommended: MPN: BLM15AG121SN1D (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0402, 1.0UF, 10V, +/- 10% Recommended: MPN: GRM155R61A105KE15D (MURATA ELEC. NORTH AMERICA
PVCCREF	PVCCREF_DTS_E	VCCREF_DTS_E	FER-BEAD, 0402, 120.0 OHM, 200.1 MA, +/- 2% Recommended: MPN: BLM15AG121SN1D (MURATA ELEC. NORTH AMERICA)	CAPC, X5R, 0402, 1.0UF, 10V, +/- 10% Recommended: MPN: GRM155R61A105KE15D (MURATA ELEC. NORTH AMERICA

15.9 Using Fast PROCHOT_N Feature of SoC for PSU Overload Protection when Momentary Global P_{MAX} is Detected

The Intel® Atom™ Processor C3000 Product Family CRBs system power supplies (a.k.a. PSUs) should be properly sized to handle the max system power consumption.

On the platform level, there is an option to employ the fast PROCHOT_N feature for reduction of the total system power P_{MAX} pulse duration down to ~100 µs, which offers the possibility to reduce the system power supply size and thus reduce cost.

With the fast PROCHOT_N enabled, the system power supply sizing can be dictated by real workloads instead of the virus condition. Fast PROCHOT_N serves as a PSU protection mechanism (from over-current shutdown) for incidental P_{MAX} spikes associated with power-virus-like applications while in Turbo mode.

With the fast PROCHOT_N enabled, the PROCHOT_N signal is asserted to indicate the system power exceeds supported application power limits. Once the PROCHOT_N signal is sent to the SoC (output mode disabled), the SoC will guarantee that:

- The power will drop below $P_{throttle}$ (~1.6x TDP as guideline) within 100 µs.
- The power will continue to drop to within 10ms except for long instructions.
- The power maintains a lower level until the PROCHOT_N signal is de-asserted. The recommendation is to hold PROCHOT_N active low for 100ms.

See Figure 15-41 and Figure 15-42 for the PROCHOT# signal connection and the SoC behavior with the PROCHOT# assertion.

Figure 15-43 illustrates the SoC behavior difference between without fast PROCHOT# enabled and with fast PROCHOT# enabled.

Figure 15-41. Fast PROCHOT# Signal Connection between Power Supplies and SoCs

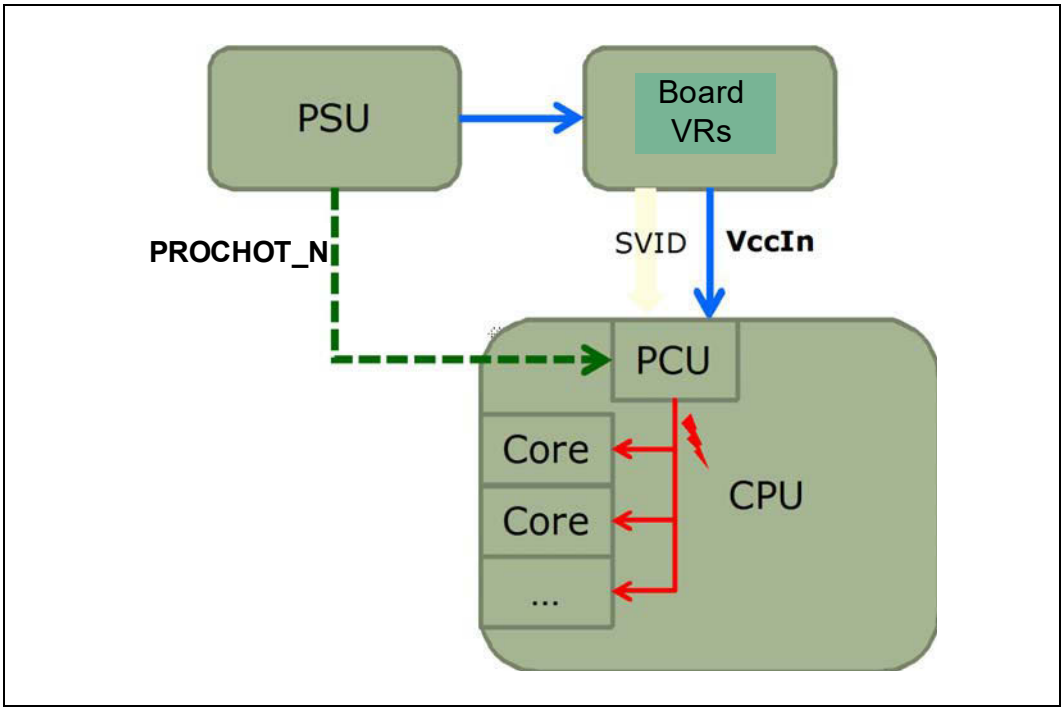
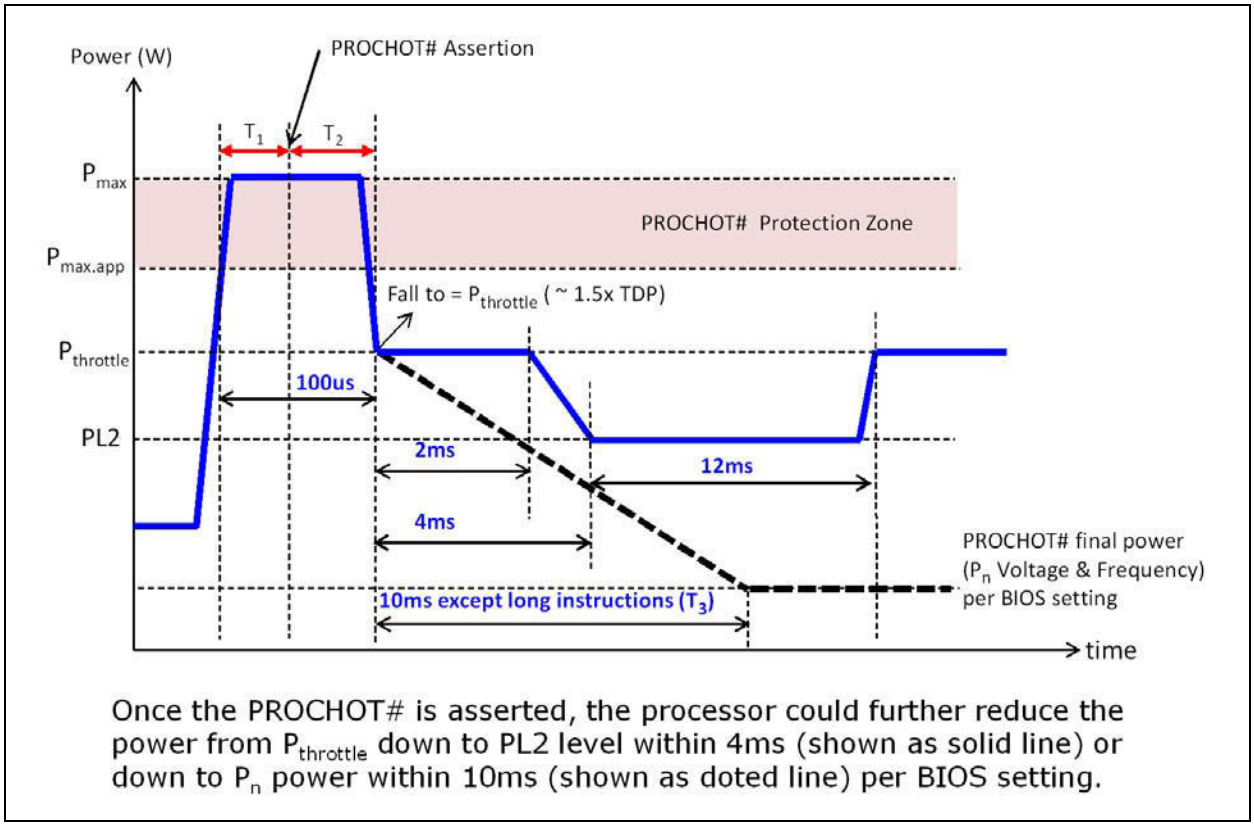


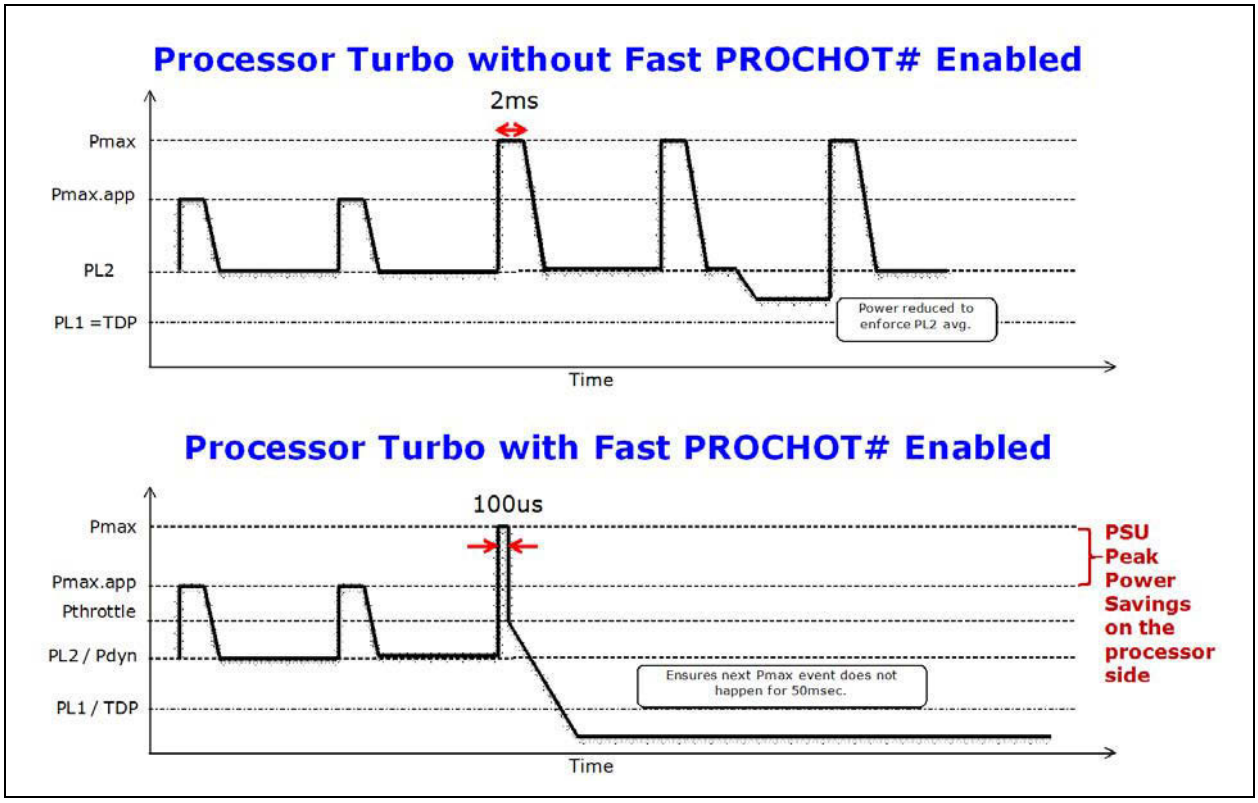
Figure 15-42. SoC Behavior with Fast PROCHOT# Enabled



Notes:

1. T_1=20µs, the time for the system power supplies or board logic to detect power excursion above $P_{MAX.APP.SYSTEM}$ and assert the PROCHOT#.
2. T_2=80µs, the time for the SoC to reduce the power down to $P_{THROTTLE}$ level.
3. T_3=10ms (min), the time for the SoC to further reduce the power down to P_N level.
4. $P_{MAX.APP}$ is the SoC power limit under normal applications against rare P_{MAX} event, and it is recommended to be set to 1.6 x TDP as a guideline.
5. $P_{THROTTLE}$ is the SoC throttle power once the PROCHOT# assertion, and it is recommended to be set to 1.5 x TDP as a guideline.

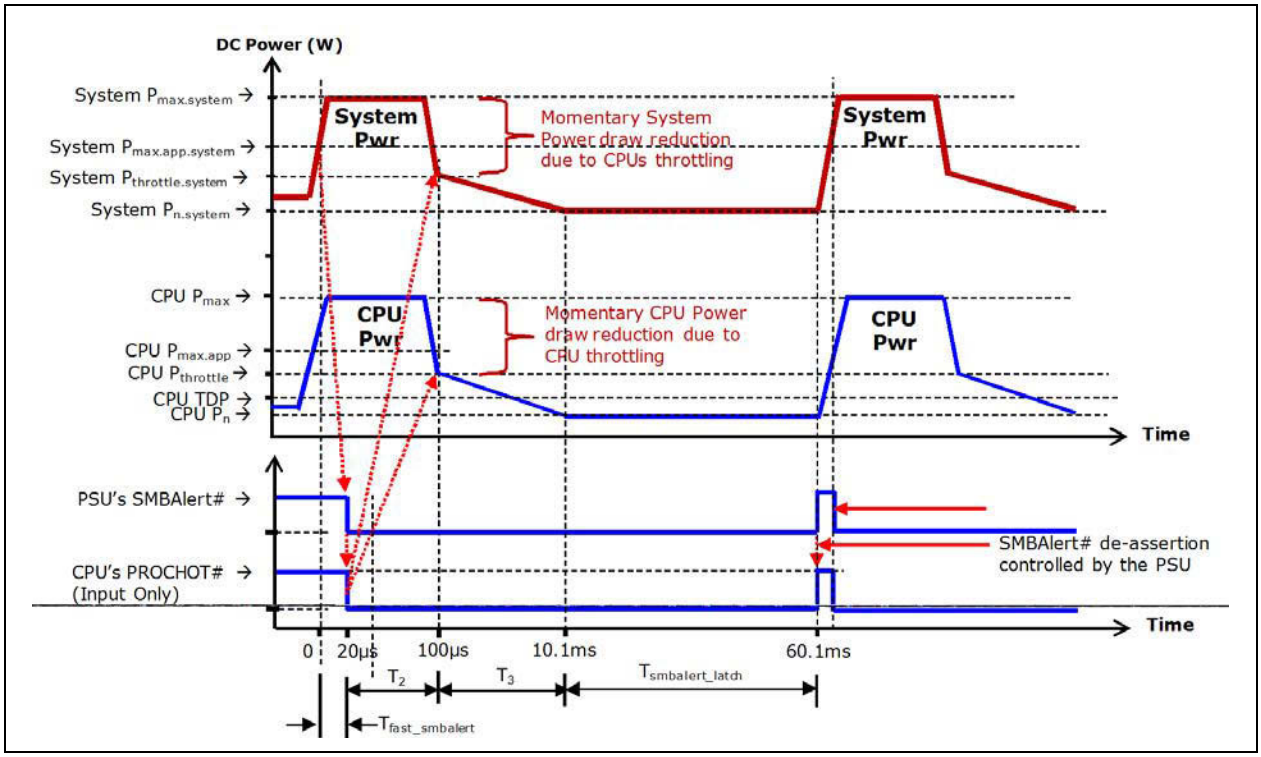
Figure 15-43. SoC Behavior Difference without and with Fast PROCHOT# Enabled



On the Platform level, once the PROCHOT# signal is asserted, the system total power would be momentarily reduced due to SoC throttling.

Figure 15-44 illustrates the SoC and system power behavior with fast PROCHOT# enabled.

Figure 15-44. System Level Behavior with Fast PROCHOT# Enabled



Notes:

1. $P_{MAX.SYSTEM}$: the system power limit corresponding to all SoCs at P_{MAX}+ other system component power.
2. $P_{MAX.APP.SYSTEM}$: the system power limit corresponding to all SoCs at $P_{MAX.APP}$+ other system component power.
3. $P_{N.SYSTEM}$: the system power limit corresponding to all SoCs at P_n+ other system component power.
4. $T_{FAST\_SMBALERT}$: the time for the PSU to detect excursion above Pmax.app and assert SMBAlert#, which is equal to T_1 in Figure 15-42.
5. $T_{SMBALERT\_LATCH}$: the time for the PSU to latch and hold SMBAlert to active low after SMBAlert assertion, 100ms is recommended as a guideline.

To implement the fast PROCHOT# feature, it requires that the platform is equipped with a fast output current sense circuit, which is capable of:

- Detecting the system power excursion above $P_{MAX.APP.SYSTEM}$.
- Then assert all SoC PROCHOT# signals to low within ~20 µs.

There are two options of the implementation of a fast output current sense circuit:

- One option is to implement it inside the system power supplies, so that the power supplies can drive the PROCHOT# signal to logic "low" within ~20 µs via the SMBAlert# signal once the power excursion above the threshold is detected. An example is shown in Figure 15-45.
- The other option is to implement it on the baseboard, so that the board logic can assert the PROCHOT# signal within ~20 µs once the power excursion over the threshold is detected. A block diagram is shown in Figure 15-46.

Figure 15-45. Power Supply Implementation to Support Fast PROCHOT# Concept

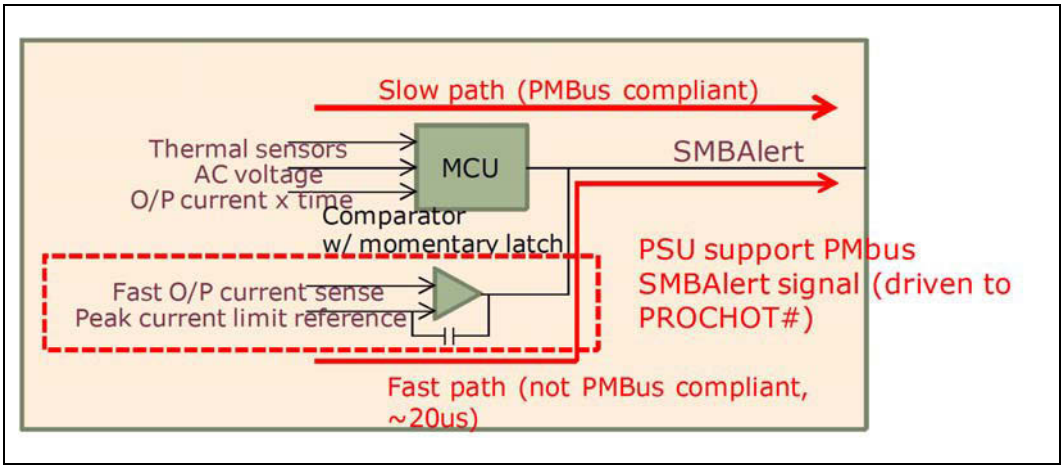
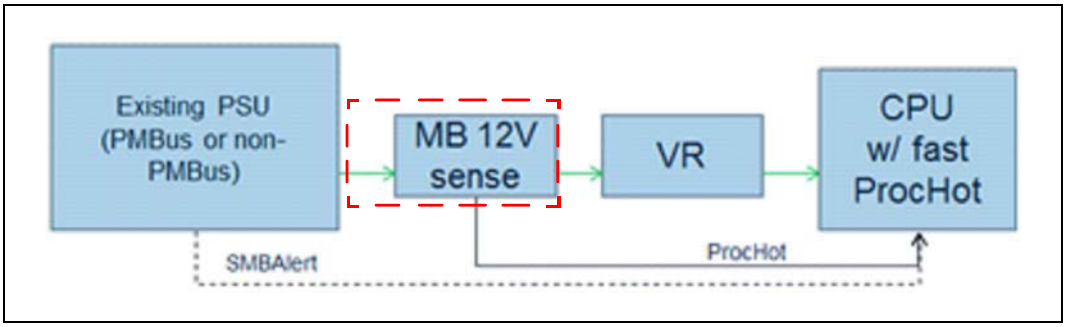
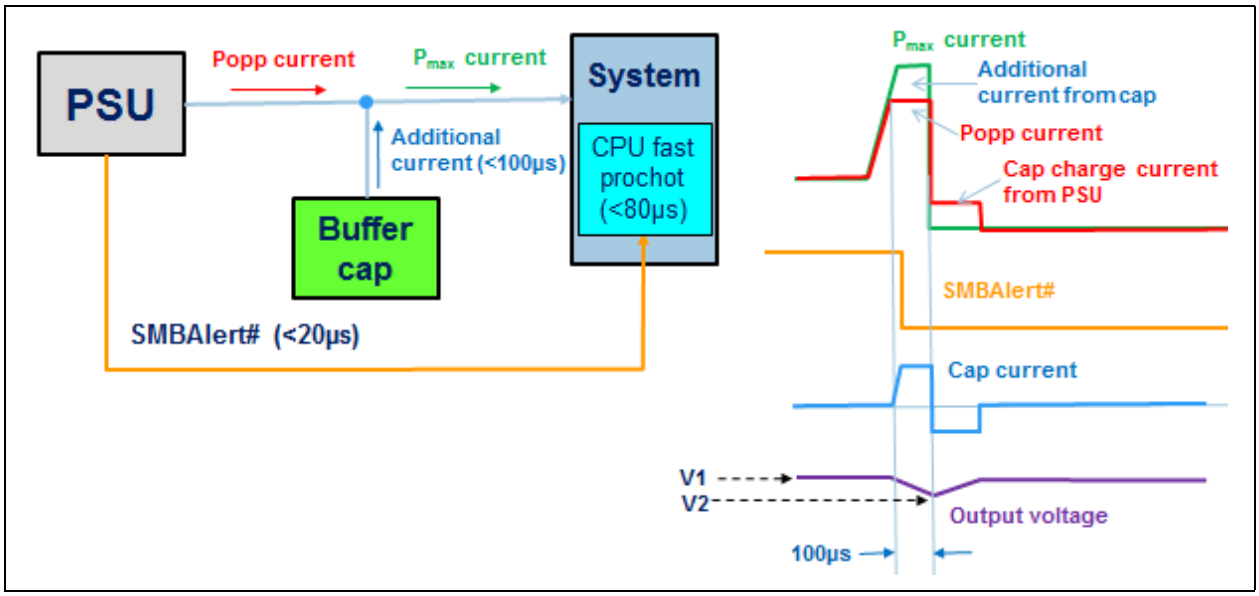


Figure 15-46. Board Logic Implementation to Support Fast PROCHOT#



Besides a fast output current sense circuit, it requires that the platform have sufficient buffer (bulk) caps to protect the system 12V rail from dropping below voltage regulation limits during max system power $P_{MAX.SYSTEM}$ levels due to SoC P_{MAX} virus condition. For the PSU implementation, the buffer caps are used to provide additional current/power(<100 µs) which results from the difference between $P_{MAX.SYSTEM}$ and PSU over power protection (OPP) level, as illustrated in Figure 15-47. The buffer caps can be placed either inside the power supplies or on the baseboard on 12V power plane, it is best to have them close to the load.

Figure 15-47. The Buffer Cap Function (PSU Implementation as an Example)



The total required Min buffer capacitance to support P_{MAX} can be calculated as follows:

$$C_{min}(\mu F) = 2 \times (P_{max} - P_{opp}) \cdot \frac{T_{max}(\mu s)}{V^2{}_1 - V^2{}_2}$$

Where:

C: Min buffer cap size assuming PSU(s) has 0µF output capacitance and 0µF on the baseboard 12V power rail.

P_{MAX}: the max system power (budget) due to SoC P_{MAX} virus condition (SoC P_{MAX}=2x TDP).

P_{OPP}: the PSU minimum OPP (over power protection) power level, and it is always set above system power budget corresponding with SoC $P_{MAX.APP}$.

Note: SoC Pmax.app=1.6x TDP; PSU SMBAlert# trip point (P_{TRIP}) must be set below P_{OPP}, but above $P_{MAX.APP}$, so the overall relationship is: $P_{MAX.APP} < P_{TRIP} < P_{OPP} < P_{MAX}$.

Example: P_{MAX}=1200W, P_{OPP}=1100W, V1 =12.0V, V2 =11.4V; T_{MAX} =120us --> C =2200uF

Reminder: The power difference between P_{MAX} and P_{OPP} is supplied by the buffer cap.

T_{MAX}: The throttle time delay after the system power exceeds the pre-defined power threshold (100 µs).

V_1 and V_2: The PSU output voltage levels at the beginning and the end of P_{MAX} time interval (T_{MAX}).

For the power supply implementation to enable the fast PROCHOT# feature, it is required that:

- The PSU shall set the over power protection (OPP) level low enough to protect the power supply continuously running in OPP mode for repeated 1msec durations at a 1% duty cycle (design guard band is included).
  - The PSU minimum OPP level should be always set above $P_{MAX.APP.SYSTEM}$ with some guard band taken into account.
  - Without any system buffer caps, the PSU should operate into the over power protection (OPP) level for a duration of no less than 1msec with stable voltage fold back, no PSU shut down and no PSU component overheating.
  - With the required system buffer caps, the PSU shall be stable operating at any resistive load point from rated power up to the OPP point: 12V output voltage at the remote sense remains within the regulation limits and all the components in the power rail meet the targeted electrical de-rating requirements.
- The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the Pmax.app level.
  - A current sense resistor right on the output side of the PSUs output capacitors shall be used to quickly sense current exceeding the $I_{THROTTLE}$ threshold.
  - Minimum OPP level should be greater then system Pmax.app to guarantee system normal operation in all supported applications.
- The PSU should support fast SMBAlert assertion:
  - $T_{FAST\_SMBALTER}$: 10µs ~ 20 µs, the time for the PSU to assert SMBAlert# signal once the output current exceeds the $I_{THROTTLE}$ threshold.
  - $T_{SMBALERT\_LATCH}$: 100ms (±50ms), can be programmed by the PSU.
- The system buffer caps should be properly sized to support the power difference between $P_{MAX.SYSTEM}$ and PSU OPP for 100 µs duration.

Intel® Atom™ Processor C3000 Product Family system designers have the option to implement the Fast PROCHOT in their AC/DC power supplies or on the board.

§ §

A 10GBASE-KR Annex 69B Informative Channel Parameters

The annex 69B informative channel parameter references for the Harrisonville platform are as follows:

- For 10GBASE-KR - IEEE 802.3 Clause 72 and Annex 69B

Harrisonville 10GBASE-KR has adopted the informative channel parameters found in the IEEE 802.3-2012 Annex69B as a normative channel specification for the KR interface on Denverton. Although these specifications specify two test points (TP1 and TP4) where TP4 includes the capacitor as part of the receiver, these channel specifications are defined from device pin to device pin. As pin-to-pin specifications they do not include either device package.

There are five channel limits specified in the frequency domain, three of which concern the insertion loss performance of the channel. The remaining two bound the return loss and ratio of insertion loss to crosstalk. As an additional reference, refer to the IEEE 802.3-2012 specification.

A.1 Insertion Loss

Insertion loss is a term, expressed in decibels, used to describe the frequency domain characteristics of a network's scattering parameters. Simply put, it describes the energy lost through a device or network. For a 2-port scattering parameter matrix, the insertion loss, or S12, is the energy measured at port 1when the input is at port 2. For a passive device, the network is expected to be reciprocal such that S21 equals S12.

If an interconnect channel only consists of a single transmission line, the insertion loss or energy lost in the channel is due mainly to the chosen PCB material, copper roughness, and skin effect losses. The frequency dependent signal attenuation is thus very smooth as shown in Figure A-1. However, practical interconnects require multiple boards, connectors, and layer transition vias that add noise to the insertion loss behavior. Because of these channel degradations, the insertion loss is specified with three limits.

The several insertion loss limits for KR are taken from the IEEE 802.3 specification using the values in Table A-1 and implemented in Equation A-1 and Equation A-2. For all the fitting equations using the least mean squares methodology, refer to the IEEE 802.3-2012 Annex 69B.

Table A-1. Insertion Loss Parameters

Parameter	10GBASE-KR	Units
F_{min}	0.05	GHz
F_{max}	15	GHz
b_1	$2x10^{-5}$	
b_2	$1.1x10^{-10}$	
b_3	$3.2x10^{-20}$	
b_4	$-1.2x10^{-30}$	
f_1	1	GHz
f_2	6	GHz
F_a	0.1	GHz
F_b	5.15625	GHz

Equation A-1. IL_{MAX}, lower

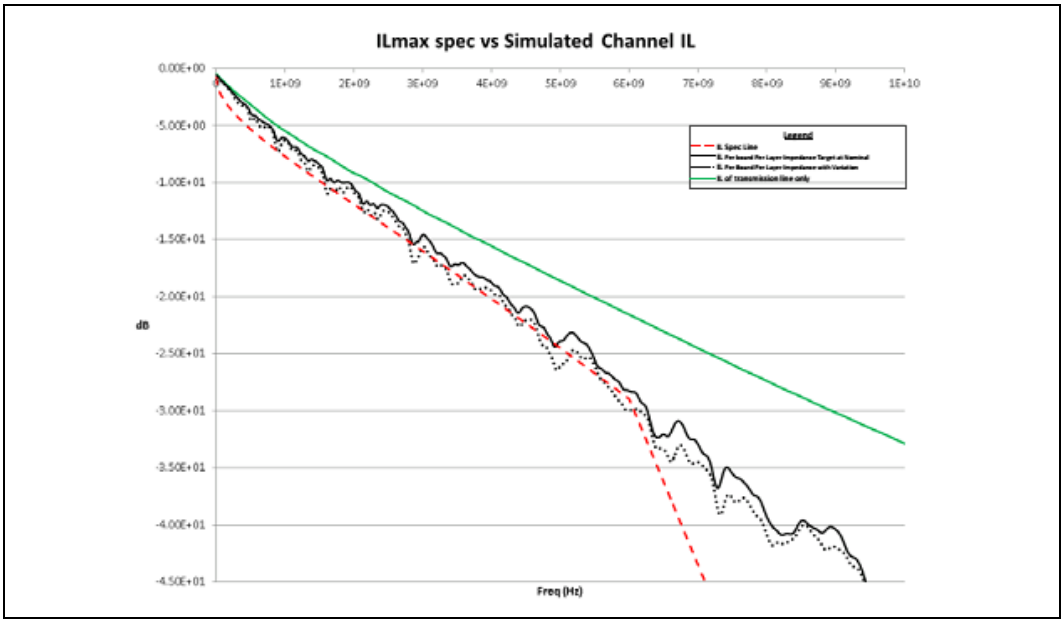
$$IL_{max}(f) = A_{max}(f) + 0.8 + 2 \times 10^{-10} f, \text{ for } f_{min} \text{ to } f_2$$

Equation A-2. IL_{MAX}, upper

$$IL_{max}(f) = A_{max}(f) + 0.8 + 2 \times 10^{-10} f_2 + 1 \times 10^{8}(f - f_2), \text{ for } f_2 \text{ to } f_{max}$$

Where A_{max} *(f)* is described in Section A.2, "Fitted Insertion Loss A(f) and Amax".

Figure A-1. Insertion Loss Plot



Plots of simulated channel insertion loss are shown in Figure A-1. There are three curves compared against the specification line. The insertion loss characteristic of a simple channel consisting only of transmission line routing is shown in green. If layer transitions, vias, and connectors are added to the channel, the same physical length of routing has the response shown by the solid black line even with the impedance targets assumed to be at nominal. If per-board, per-layer impedance variations are comprehended in simulation, the channel insertion loss characteristic, which was marginal to the specification mask is now beyond the specification line. Care must be taken to ensure all manufacturing tolerances are comprehended in the channel design.

A.2 Fitted Insertion Loss *A(f)* and A_{max}

The insertion loss response of the channel can be fitted using a least mean squares algorithm to obtain a fitted attenuation response *A(f)* as described in Annex 69B.4.2 of the IEEE specification. This fitted attenuation is bounded by the A_{MAX} specification shown in Equation A-3. It is intended to compare the performance of a channel with many interconnect components to a simple channel consisting of only a transmission line. One caveat here is that any resonance behavior from components such as connectors or vias pulls the fitted attenuation response of the channel lower. Having fewer resonance behaviors in the channel results in less fitted attenuation.

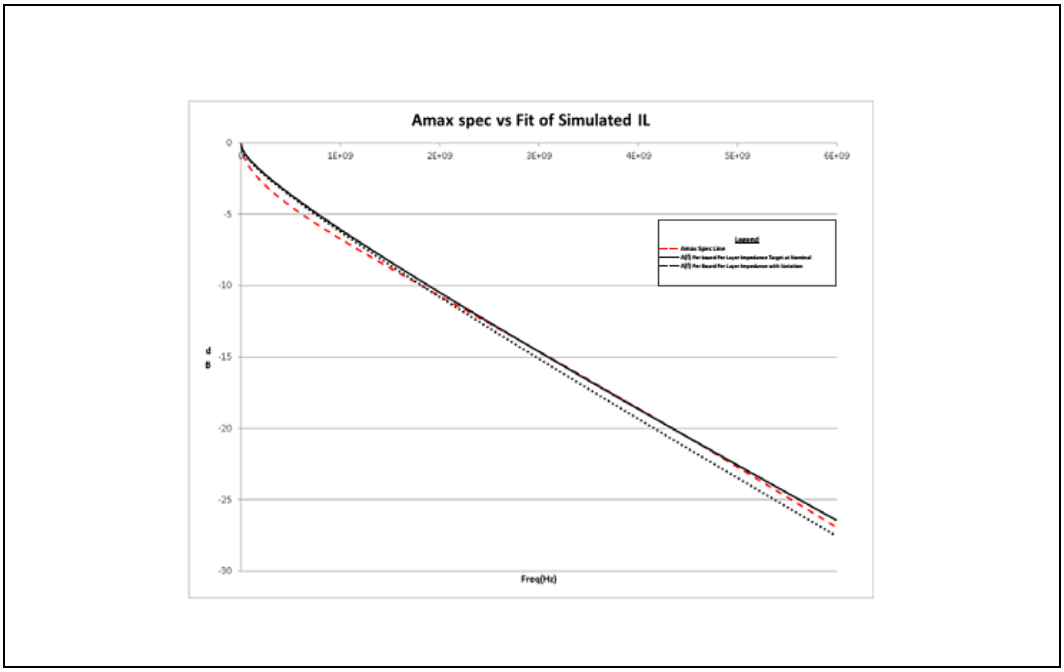
Figure A-2 shows two fitted loss curves from simulation data plotted along with A_{MAX}.

Equation A-3. A_{MAX}

$$A_{max}(f) = 20\log(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3), \text{ for } f_1 \le f \le f_2$$

where the coefficients are defined in Table A-1.

Figure A-2. Amax Loss



The plots of fitted attenuation for a simulated channel insertion loss are shown in Figure A-2. There are two curves compared against the specification line (dashed red line). Although the channel, which has all boards and layers at the nominal impedance (solid black line) is beyond the A_{MAX} specification line, adding in per-board, per-layer impedance variation increases the fitted insertion loss as shown by the dotted black line. Care must be taken to ensure the channel performance compared to the specification mask comprehends per-board and per-layer impedance variation.

A.2.1 Insertion Loss Deviation (ILD)

With the fitted attenuation obtained, the difference or deviation from this fitted response and the insertion can be examined and specified within limits. ILD and its boundaries are specified by the following equations:

Equation A-4. ILD

$$ILD = IL(f) - A(f)$$

Equation A-5. ILD_{MIN}

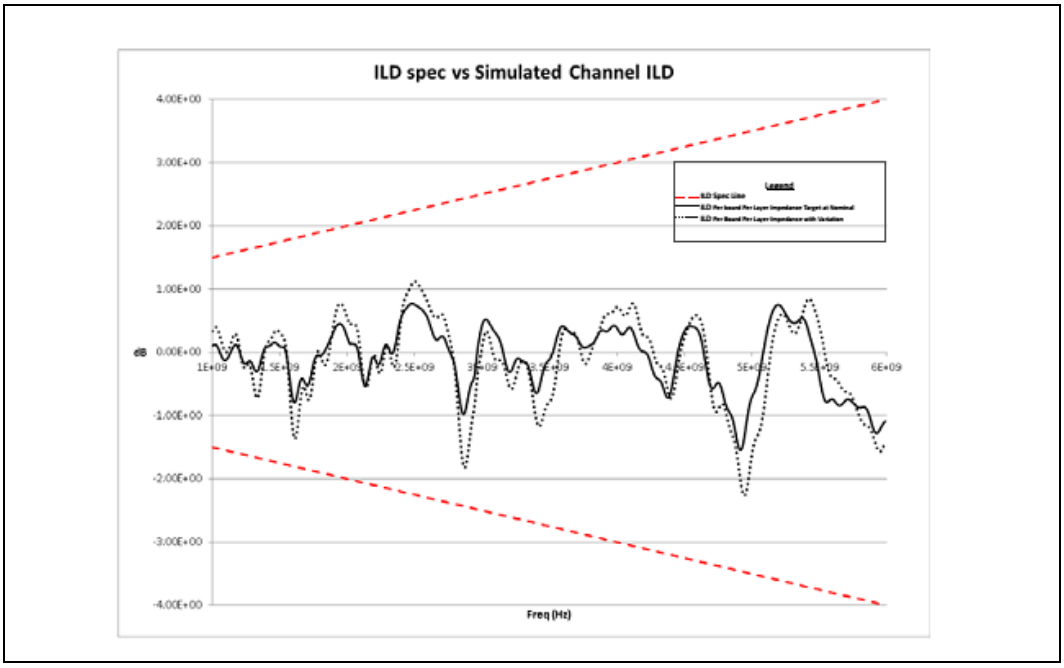
$$ILD_{min}(f) = -1.0 - 0.5 \times 10^{-9} f, \text{ for } f_1 \le f \le f_2$$

Equation A-6. ILD_{MAX}

$$ILD_{max}(f) = 1.0 + 0.5 \times 10^{-9} f, \text{ for } f_1 \le f \le f_2$$

where the fitted attenuation *A(f)* is described in Section A.2, "Fitted Insertion Loss A(f) and Amax".

Figure A-3. ILD

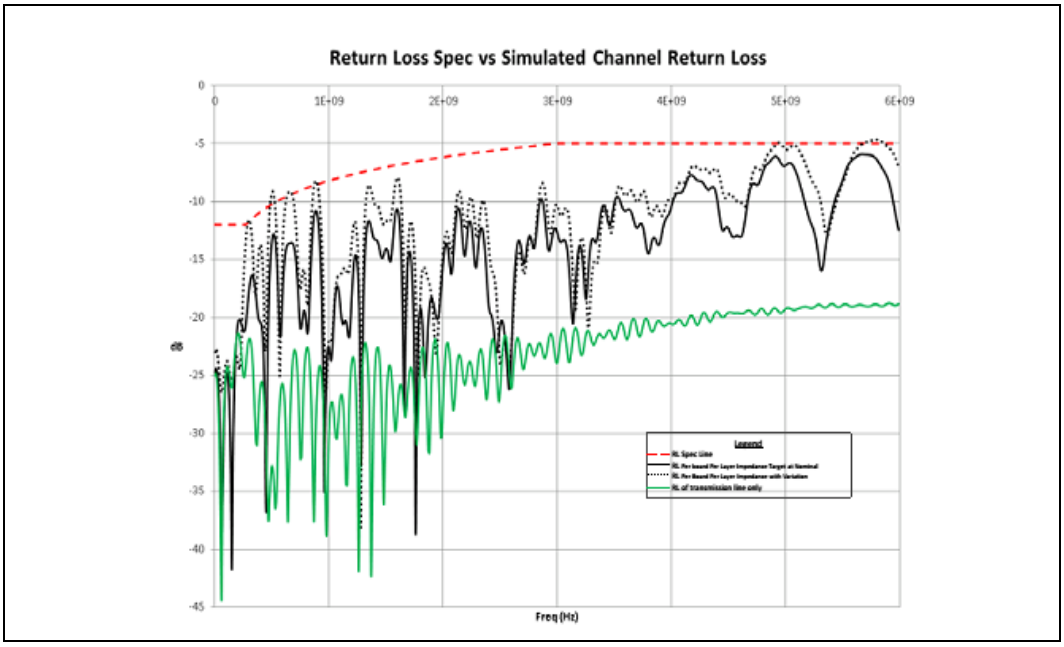


Plots of simulated channel insertion loss deviation are shown in Figure A-3. There are two curves compared against the specification line. The solid black line is the insertion loss deviation with all boards and layers assumed to be at the nominal impedance corner. If per board, per-layer impedance variations are comprehended in simulation, the channel insertion loss deviations become more exacerbated as shown by the dotted black line shown in Figure A-3. Care must be taken that all manufacturing tolerances are comprehended in the channel design.

A.2.2 Return Loss (RL)

RL is a term, expressed in decibels, used to describe a frequency domain characteristic of a network's scattering parameters. Simply put, it describes the energy measured at the input of a device or network when energy is excited at the input. For a 2-port scattering parameter matrix, the return loss or S11 is the energy measured at port 1 when the energy input is at port 1.

Figure A-4. Return Loss



Plots of simulated channel return loss are shown in Figure 6-24 There are three curves compared against the specification line. The return loss characteristic of a simple channel consisting only of transmission line routing is shown in green. The solid black line is return loss of a channel of the same physical length but with the addition of interconnect components while keeping all boards and layers at the nominal impedance corner. If per-board, per-layer impedance variations are comprehended in simulation, the channel return loss becomes more exacerbated and is beyond the specification line as shown by the dotted black line shown in Figure 6-24. Care must be taken that all manufacturing tolerances are comprehended in the channel design.

A.2.3 Insertion Loss-to-Crosstalk Ratio (ICR)

ICR is the ratio of insertion loss to the power sum crosstalk at the pin of the receive device. For equations on computing the power sum crosstalk please refer to the IEEE 802.3-2012 specification.

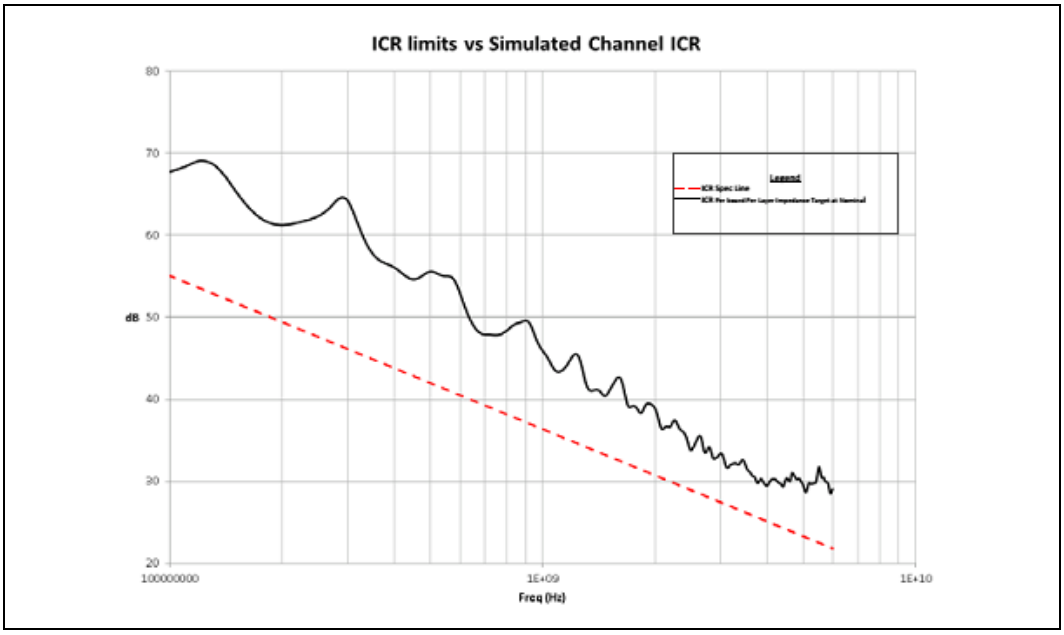
Equation A-7. ICR Limit

$$ICR_{min}(f) = 23.3 - 18.7\log_{10}\left(\frac{f}{5GHz}\right), \text{ for } F_a \text{ to } F_b$$

where F_a and F_b are defined in Table A-1.

Figure 6-24 is an example of the channel ICR plotted against the ICR specification limit.

Figure A-5. ICR Limits



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B CRB 8L Stack-Up Details

The following tables provide the CRB stack-ups shown in Chapter 2, "Platform Stack-up and General Design Considerations" plus details on trace impedances and spacings. If not otherwise stated all impedance values are ± 10%.

B.1 Stack-Up for Aspen Cove Details

Table B-1. 8-Layer Printed Circuit Board (PCB) Stack-Up Example (Aspen Cove)

Layer	Type	Material	ε_r	Thickness (mils)
		Solder Mask		1.0
L1	Signal	CU + Plating	4	1.95
	Prepreg	(IT150DA) 106 78%		2.5
L2	Plane	CU 1 oz.		1.3
	Core	IT180I		3.0
L3	Signal	CU 1 oz.	3.9	1.3
	Prepreg	(IT180I) 7628 47.5%*2		14.76
L4	Plane	CU 2 oz.		2.6
	Core	IT180I		8
L5	Plane	CU 2oz.	3.9	2.6
	Prepreg	(IT180I) 7628 47.5%*2		14.76
L6	Signal	CU 1 oz.		1.3
	Core	IT180I		3
L7	Plane	CU 1 oz.		1.3
	Prepreg	(IT150DA) 106 78%		2.5
L8	Signal	CU 0.5 oz.	3.9	1.95
		Solder Mask		1.0
Total Thickness				64.82 mils ± 10%

Table B-2. 8-Layer Printed Circuit Board (PCB) Stack-Up 40 Ohm Z_0(Aspen Cove) [Single Ended]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	40	2	6.5	40.12
	Prepreg				
L2	Plane				
	Core				
L3	Signal	40	4/2	6	39.75
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	40	5/7	6	39.75
	Core				
L7	Plane				
	Prepreg				
L8	Signal	40	7	6.5	40.12
SM					

Table B-3. 8-Layer Printed Circuit Board (PCB) Stack-Up 50 Ohm Z_0(Aspen Cove) [Single Ended]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	50	2	4.125	50.45
	Prepreg				
L2	Plane				
	Core				
L3	Signal	50	4/2	3.875	49.73
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	50	5/7	3.875	49.73
	Core				
L7	Plane				
	Prepreg				
L8	Signal	50	7	4.125	50.45
SM					

Table B-4. 8-Layer Printed Circuit Board (PCB) Stack-Up 85 Ohm Z_0(Aspen Cove) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	85	2	5.0/7.0	84.07
	Prepreg				
L2	Plane				
	Core				
L3	Signal	85	4/2	4.75/7.25	85.03
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	85	5/7	4.75/7.25	85.03
	Core				
L7	Plane				
	Prepreg				
L8	Signal	85	7	5.0/7.0	84.07
SM					

Table B-5. 8-Layer Printed Circuit Board (PCB) Stack-Up 93 Ohm Z_0(Aspen Cove) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	93	2		
	Prepreg				
L2	Plane				
	Core				
L3	Signal	93	4/2		
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	93	5/7		
	Core				
L7	Plane				
	Prepreg				
L8	Signal	93	7		
SM					

Table B-6. 8-Layer Printed Circuit Board (PCB) Stack-Up 100 Ohm Z_0(Aspen Cove) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	100	2	4.0/15.0	99.64
	Prepreg				
L2	Plane				
	Core				
L3	Signal	100	4/2	3.75/15.25	100.09
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	100	5/7	3.75/15.25	100.09
	Core				
L7	Plane				
	Prepreg				
L8	Signal	100	7	4.0/15.0	99.64
SM					

B.2 Stack-Up for Cormorant Lake Details

Table B-7. 8-Layer Printed Circuit Board (PCB) Stack-Up Example (Cormorant Lake)

Layer	Type	Material	ε_r	Thickness (mils)
		Solder Mask		1.0
L1	Signal	CU (0.5 oz.) + Plating		1.95
	Prepreg	1080h		2.8
L2	Plane	CU 1 oz.		1.3
	Core	3.0 mil (1/1) core		3.0
L3	Signal	CU 1 oz.		1.3
	Prepreg	7628 46%*2		14.5
L4	Plane	CU 2 oz.		2.6
	Core	6 mil (2/2) core		6
L5	Plane	CU 2oz.		2.6
	Prepreg	7628 46%*2		14.5
L6	Signal	CU 1 oz.		1.3
	Core	3.0 mil (1/1) core		3.0
L7	Plane	CU 1 oz.		1.3
	Prepreg	1080 65%		2.8
L8	Signal	CU 0.5 oz.+ plating		1.95
		Solder Mask		1.0
Total Thickness				62.9 mils

Table B-8. 8-Layer Printed Circuit Board (PCB) Stack-Up 40 Ohm Z_0(Cormorant Lake) [Single Ended]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	40	2	6.5	40.74
	Prepreg				
L2	Plane				
	Core				
L3	Signal	40	4/2	6	40.69
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	40	5/7	6	40.69
	Core				
L7	Plane				
	Prepreg				
L8	Signal	40	7	6.5	40.74
SM					

Table B-9. 8-Layer Printed Circuit Board (PCB) Stack-Up 50 Ohm Z_0(Cormorant Lake) [Single Ended]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	50	2	4.25	50.3
	Prepreg				
L2	Plane				
	Core				
L3	Signal	50	4/2	3.75	51.36
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	50	5/7	3.75	51.36
	Core				
L7	Plane				
	Prepreg				
L8	Signal	50	7	4.25	50.3
SM					

Table B-10. 8-Layer Printed Circuit Board (PCB) Stack-Up 85 Ohm Z_0(Cormorant Lake) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	85	2	4.0/4.0	84.36
	Prepreg				
L2	Plane				
	Core				
L3	Signal	85	4/2	4.0/4.0	83.82
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	85	5/7	4.0/4.0	83.82
	Core				
L7	Plane				
	Prepreg				
L8	Signal	85	7	4.0/4.0	84.36
SM					

Table B-11. 8-Layer Printed Circuit Board (PCB) Stack-Up 93 Ohm Z_0(Cormorant Lake) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	93	2	4.0/7.2	93.71
	Prepreg				
L2	Plane				
	Core				
L3	Signal	93	4/2	4.0/8.0	93.28
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	93	5/7	4.0/8.0	93.28
	Core				
L7	Plane				
	Prepreg				
L8	Signal	93	7	4.0/7.2	93.71
SM					

Table B-12. 8-Layer Printed Circuit Board (PCB) Stack-Up 100 Ohm Z_0(Cormorant lake) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	100	2	3.5/8.0	100.44
	Prepreg				
L2	Plane				
	Core				
L3	Signal	100	4/2	3.5/8.5	99.56
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	100	5/7	3.5/8.5	99.56
	Core				
L7	Plane				
	Prepreg				
L8	Signal	100	7	3.5/8.0	100.44
SM					

B.3 Stack-Up for Harcuvar Details

Table B-13. 8-Layer Printed Circuit Board (PCB) Stack-Up Example (Harcuvar)

Layer	Type	Material	ε_r	Thickness (mils)
		Solder Mask		0.5
L1	Signal	CU + Plating		1.9
	Prepreg	1080		2.7
L2	Plane	CU 1 oz.		1.2
	Core	3.5(1/1) Core		3.5
L3	Signal	CU 1 oz.		1.2
	Prepreg	106*2+ 8 mil dummy core+ 106*2		15.3
L4	Plane	CU 2 oz.		2.4
	Core	5mil(2/2) Core		5
L5	Plane	CU 2oz.		2.4
	Prepreg	106*2+ 8 mil dummy core+ 106*2		15.3
L6	Signal	CU 1 oz.		1.2
	Core	3.5(1/1) Core		3.5
L7	Plane	CU 1 oz.		1.2
	Prepreg	1080		2.7
L8	Signal	CU 0.5 oz.		1.9
		Solder Mask		0.5
Total Thickness				62.4 mils ± 10%

Table B-14. 8-Layer Printed Circuit Board (PCB) Stack-Up 40 Ohm Z_0(Harcuvar) [Single Ended]

Layer	Type	Trace Impedance (ohms) ± 5 ohms	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	40	2	6.4	
	Prepreg				
L2	Plane				
	Core				
L3	Signal	40	4/2	6.7	
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	40	5/7	6.7	
	Core				
L7	Plane				
	Prepreg				
L8	Signal	40	7	6.4	
SM					

Table B-15. 8-Layer Printed Circuit Board (PCB) Stack-Up 50 Ohm Z_0(Harcuvar) [Single Ended]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	50	2	4.2	
	Prepreg				
L2	Plane				
	Core				
L3	Signal	50	4/2	4.2	
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	50	5/7	4.2	
	Core				
L7	Plane				
	Prepreg				
L8	Signal	50	7	4.2	
SM					

Table B-16. 8-Layer Printed Circuit Board (PCB) Stack-Up 85 Ohm Z_0(Harcuvar) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	85	2	4.5/5.5	
	Prepreg				
L2	Plane				
	Core				
L3	Signal	85	4/2	4.0/4.7	
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	85	5/7	4.0/4.7	
	Core				
L7	Plane				
	Prepreg				
L8	Signal	85	7	4.5/5.5	
SM					

Table B-17. 8-Layer Printed Circuit Board (PCB) Stack-Up 93 Ohm Z_0(Harcuvar) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	93	2	4.0/7.2	
	Prepreg				
L2	Plane				
	Core				
L3	Signal	93	4/2	4.0/7.5	
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	93	5/7	4.0/7.5	
	Core				
L7	Plane				
	Prepreg				
L8	Signal	93	7	4.0/7.2	
SM					

Table B-18. 8-Layer Printed Circuit Board (PCB) Stack-Up 100 Ohm Z_0(Harcuvar) [Differential]

Layer	Type	Trace Impedance (ohms)	Reference Plane	Width/ Space (mils)	Simulated Z_0
SM					
L1	Signal	100	2		
	Prepreg				
L2	Plane				
	Core				
L3	Signal	100	4/2		
	Prepreg				
L4	Plane				
L5	Plane				
	Prepreg				
L6	Signal	100	5/7		
	Core				
L7	Plane				
	Prepreg				
L8	Signal	100	7		
SM					

B.4 Stack-Up for Pine Lake Details

Table B-19. 6-Layer Printed Circuit Board (PCB) Stack-Up Example (Pine Lake)

Layer		Cu Weight	Proposed Thickness (mils)	Dk, at 1 GHz	Df, at 1 GHz
	Soldermask		0.5	3.6	0.023
L1	Top	1.5 oz. finished	1.0		
	Prepreg		2.7	3.9	0.013
L2	GND	1.0 oz.	1.2		
	Core		3.5	3.9	0.014
L3	Signal	1.0 oz.	1.2		
	Prepreg		15.3	3.9	0.015
	Dummy Core		10	4	0.015
	Prepreg		15.3	3.9	0.015
L4	Signal	1.0 oz.	1.2		
	Core		3.5	3.9	0.014
L5	GND	1.0 oz.	1.2		
	Prepreg		2.7	3.9	0.013
L6	Bottom	1.5 oz. finished	1.9		
	Soldermask		0.5	3.6	0.023
	Finished Thickness (mils)		62.6		

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C SoC to LAN Common Connections

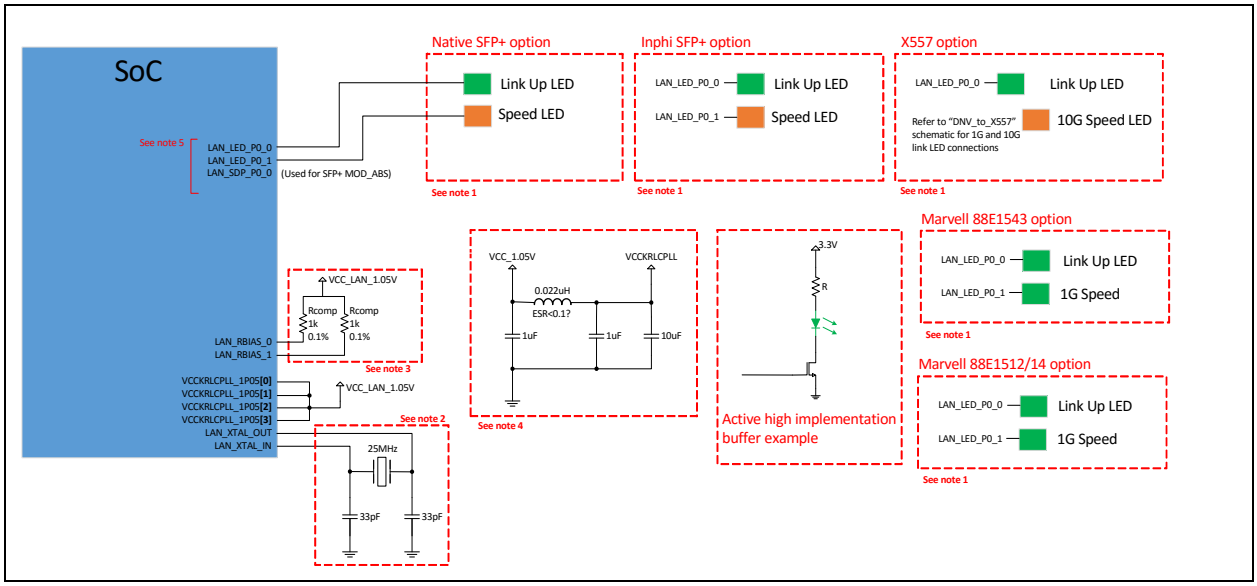
In this Appendix the SoC basic LAN connections are presented. The reference schematics show signal connects common to most LAN designs.

The following documents should be reviewed and used for any LAN design:

- Intel Ethernet Network Connection X553 [Denverton] Schematic Checklist *(#551166)*
- Intel Ethernet Connection X553 Denverton Layout Checklist *(#563945)*

C.1 SoC Power and Misc IO Connections Shared across LAN configurations

Figure C-1. SoC Basic Power and Misc IO Connections



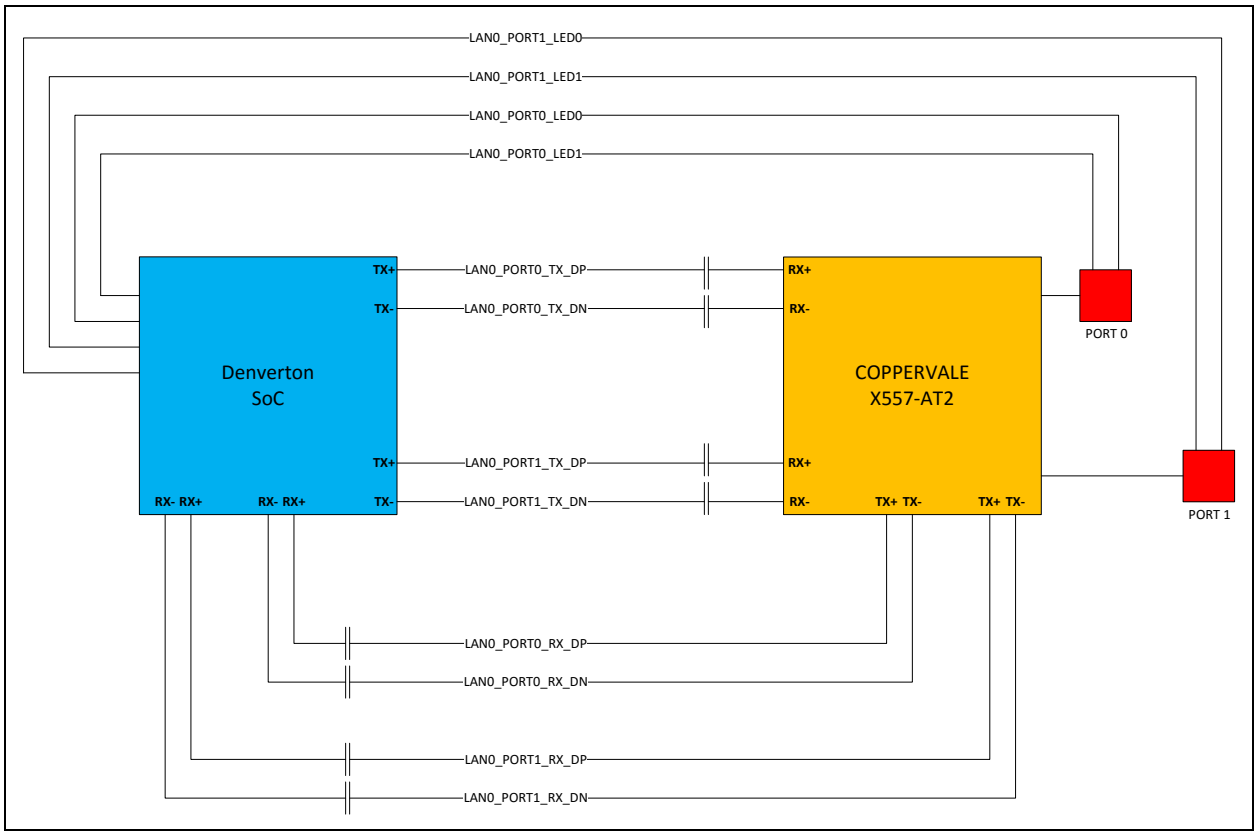
Notes:

1. Designers must implement DNV Native LEDs to draw or sink no more than 40 mA. **Default implementation of LED control pins is active low. User can change NVM to make LEDs active high**.
2. Refer to the Denverton Platform Design Guide (PDG) for specific approved crystal part numbers and routing guidelines.
3. Refer to the PDG for placement of bias resistors.
4. Refer to the PDG for VCC_LAN_1.05V filter values and recommended components. TDK Inductor PN:MLH2012F22NK is on the primary LBG reference platform.
5. Repeat connection for additional ports. LAN_SDP_P0_0 is used for SFP+ MOD_ABS signal.

C.2 SoC to X557 design reference for 10GBASE-T

The SoC to X557 design reference for 10GBASE-T application utilizes the Intel X557 PHY device.

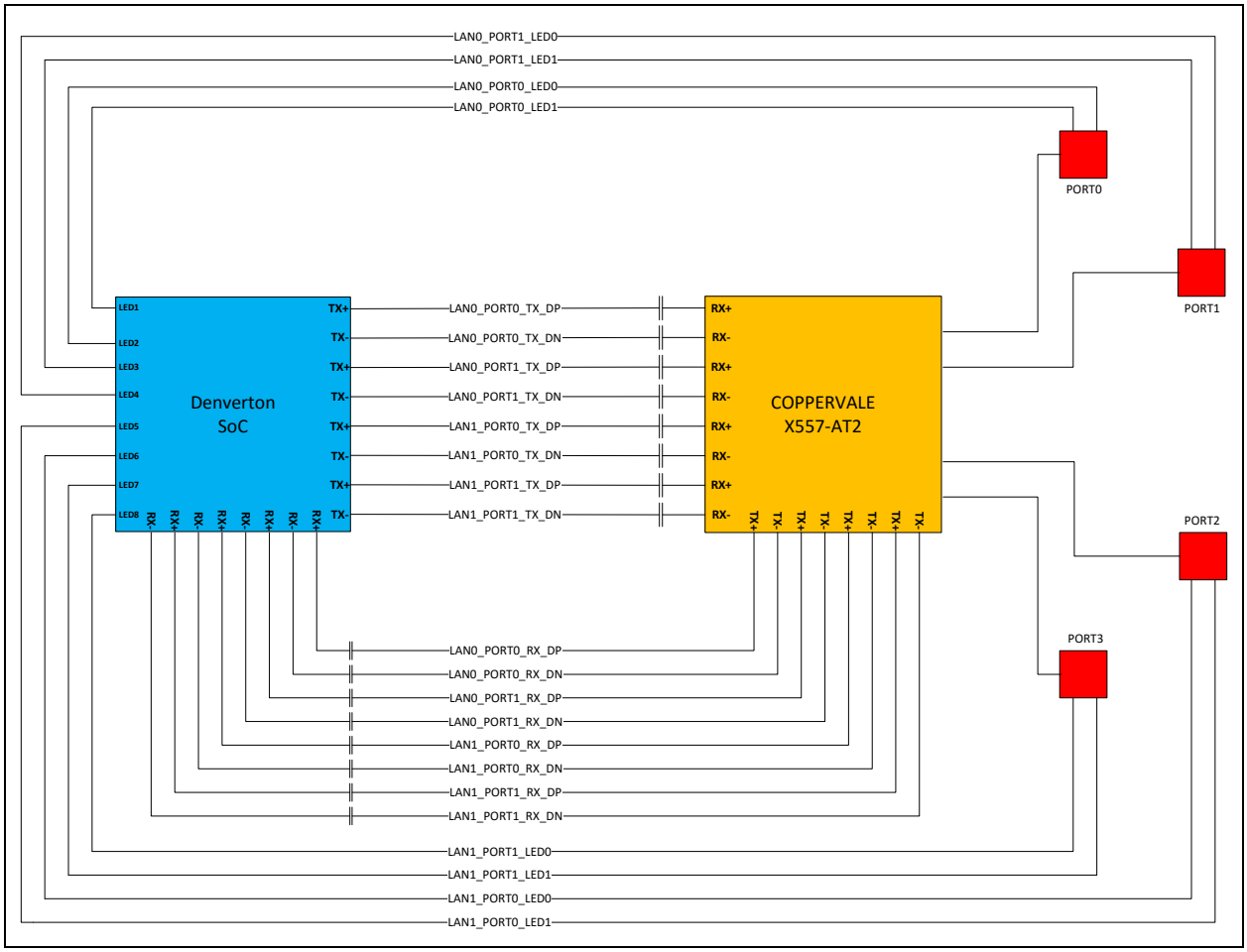
Figure C-2. SoC to X557 PHY 2 Port Schematic Diagram



Notes:

1. The signal names in the schematic match those in the Denverton EDS. If a search is done, for example, on "LAN0_PORT1_RX_DP" in the EDS, the corresponding pin number and signal description will be found.
2. A series of 0.1µF capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. Use X7R quality or better.
3. PORT0 and PORT1 use SFP+ Connectors.

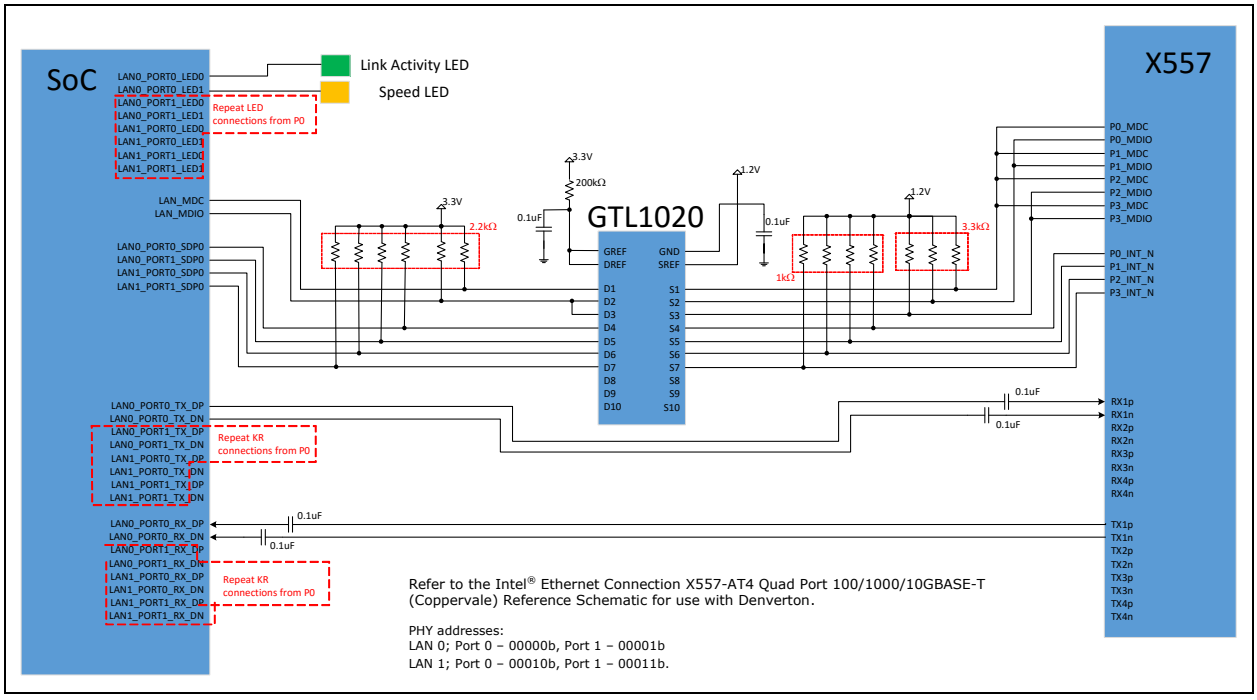
Figure C-3. SoC to X557 PHY 4 Port Schematic Diagram



Notes:

1. The signal names in the schematic match those in the Denverton EDS. If a search is done, for example, on "LAN0_PORT1_RX_DP" in the EDS, the corresponding pin number and signal description will be found.
2. A series of 0.1µF capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. Use X7R quality or better.
3. PORT0, PORT1, PORT2, and PORT3 use SFP+ Connectors.

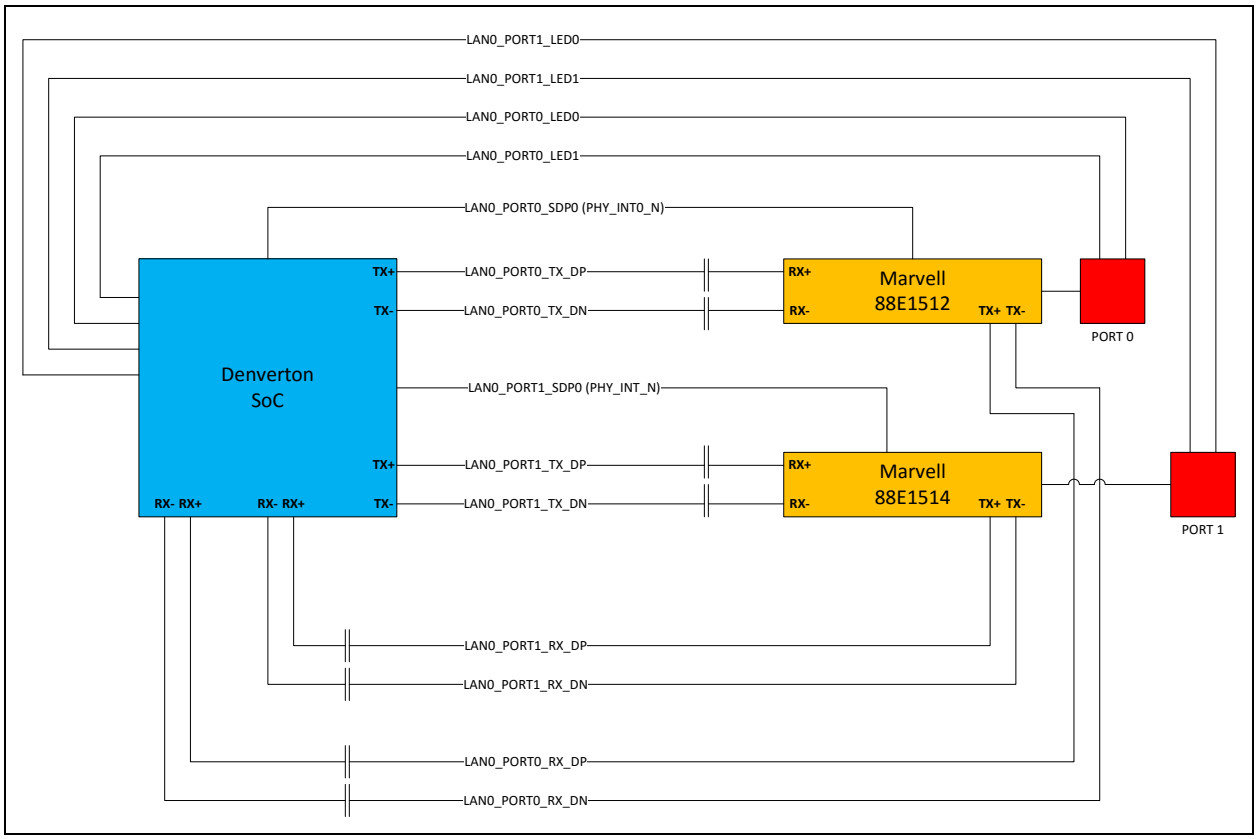
Figure C-4. SoC KR and Sideband Connections to the X557 (Coppervale)



C.3 SoC to 88E1512/88E1514

SoC to 88E1512/88E1514 uses the *Marvell 88E1512 and 88E1514 which are single channel 1GBASE-T PHYs.

Figure C-5. 1GBASE-T Block Diagram



Notes:

1. The signal names in the schematic match those in the Denverton EDS. (The only exception are the signal names in parentheses.) If a search is done, for example, on "LAN0_PORT1_RX_DP" in the EDS, the corresponding pin number and signal description will be found.
2. A series of 0.1µF capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. Use X7R quality or better.
3. The Marvell has several strapping options. Refer to the data sheet as to how to select these.
4. PORT0 and PORT1 use RJ45 Connectors.
5. LAN0 Port 0 - PHY addr = 0
   LAN0 Port 1 - PHY addr = 1
   LAN1 Port 0 - PHY addr = 2
   LAN1 Port 1 - PHY addr = 3.

Figure C-6. SGMII to Dual 1GBASE-T

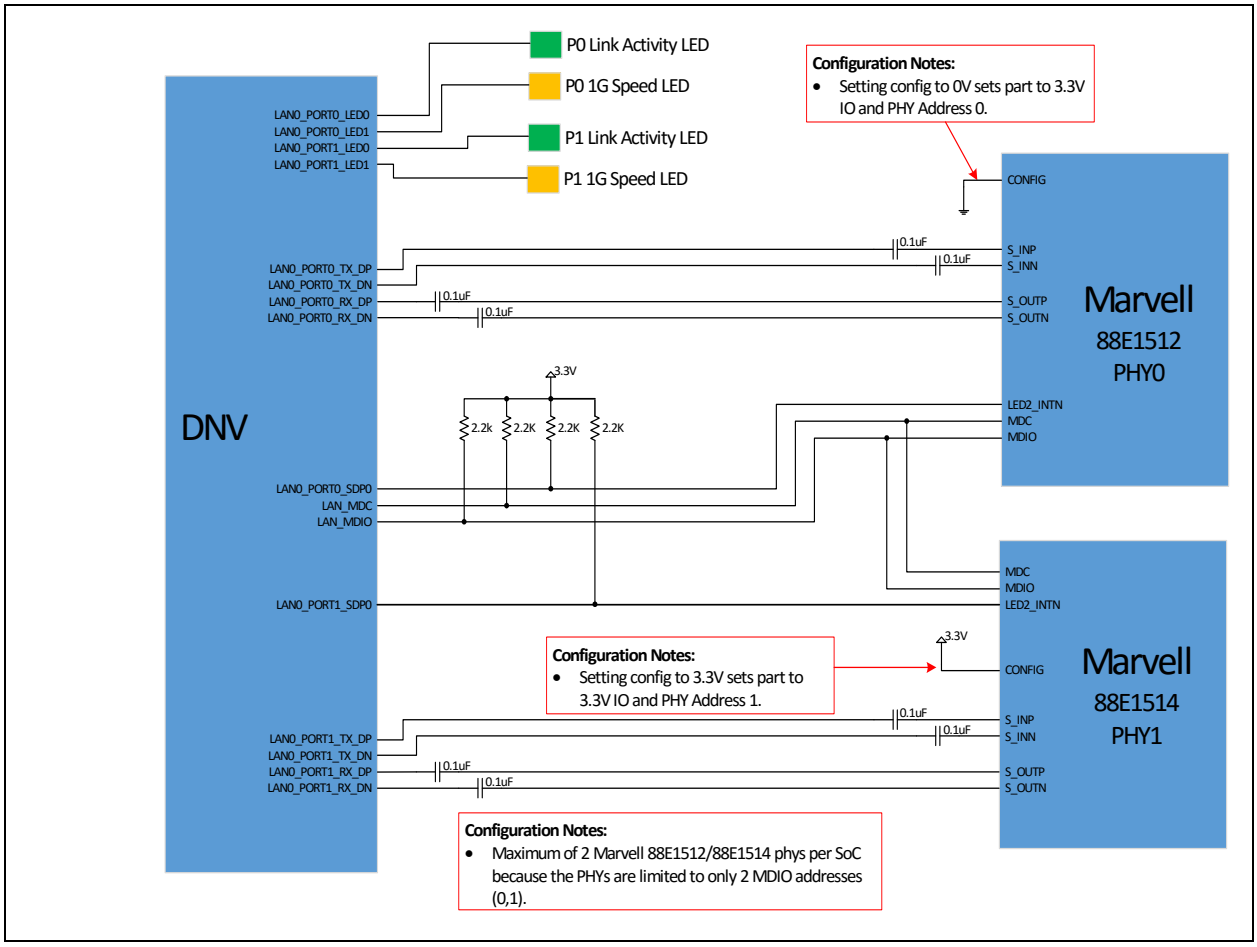
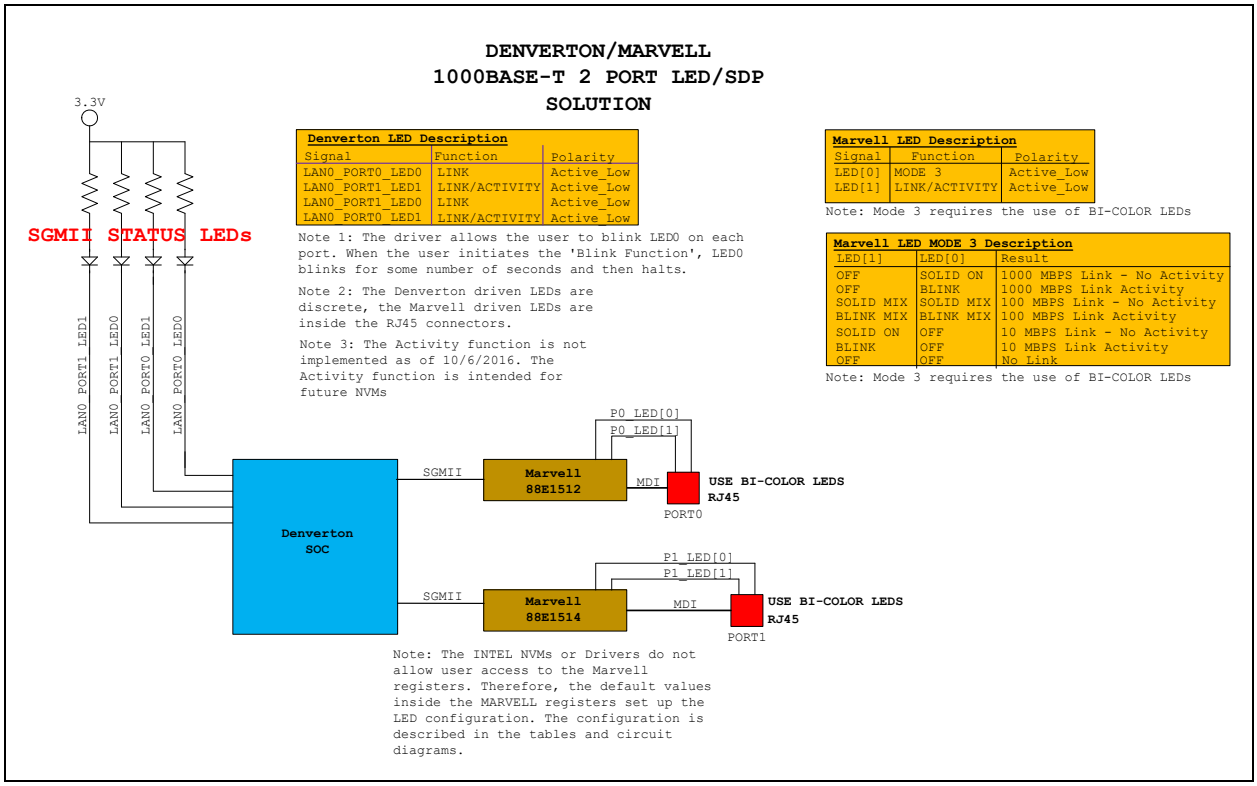


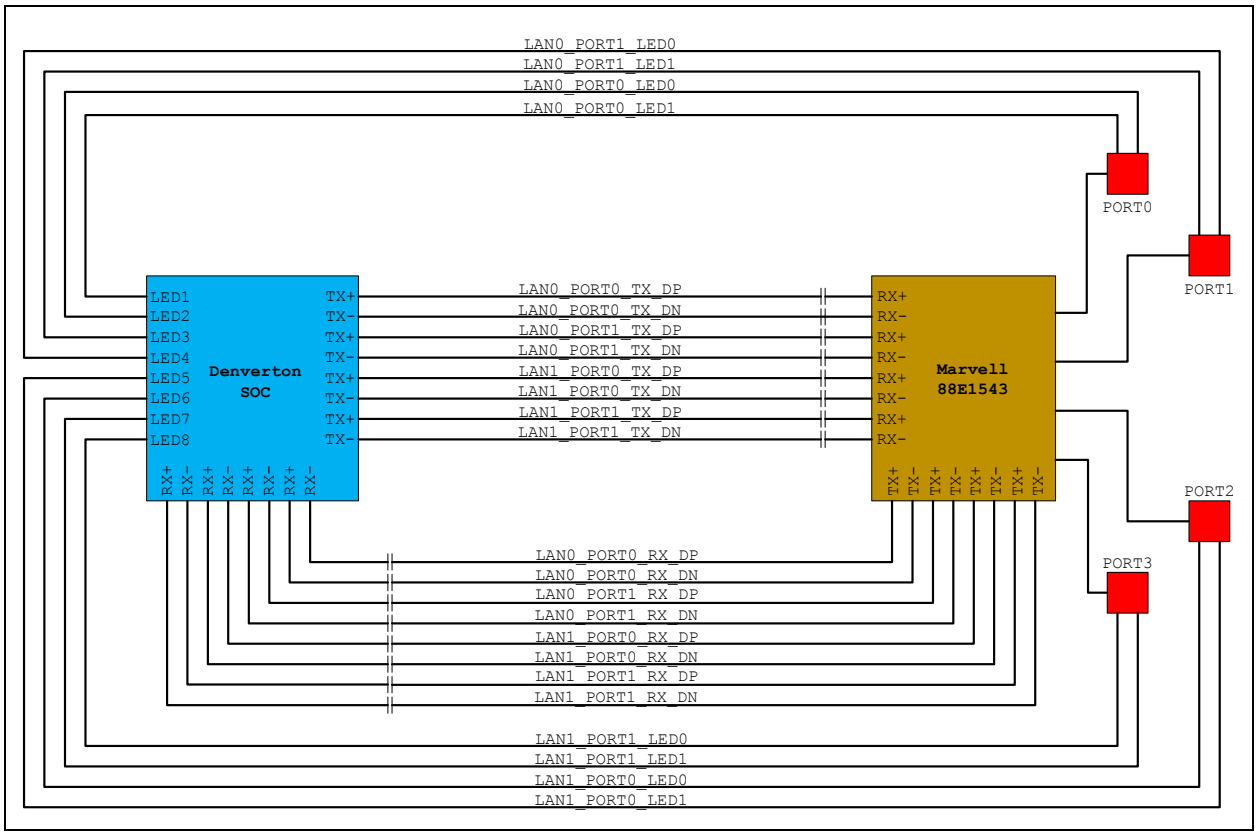
Figure C-7. Alternate LED Solution for Marvell 1512/1514 Configuration



C.4 SoC to 88E1543

SoC to 88E1543 uses the *Marvell 88E1543. It is a 4 channel PHY which provides up to 4 ports of 1GBASE-T connectivity.

Figure C-8. 1GBASE-T Block Diagram



Notes:

1. The signal names in the schematic are the same as those in the Denverton EDS. (The only exception are the signal names in parentheses.) For example if a search is done on 'LAN0_PORT1_RX_DP' in the EDS, the corresponding pin number and description can be found.
2. PORT0, PORT1, PORT2, PORT3: RJ45 Connectors
3. The Marvell has several strapping options. Refer to the data sheet as to how to select these.
4. 0.1uF series capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. It is not recommended to use Y5V capacitors but X7R quality or better.

Figure C-9. SGMII to 1GBASE-T

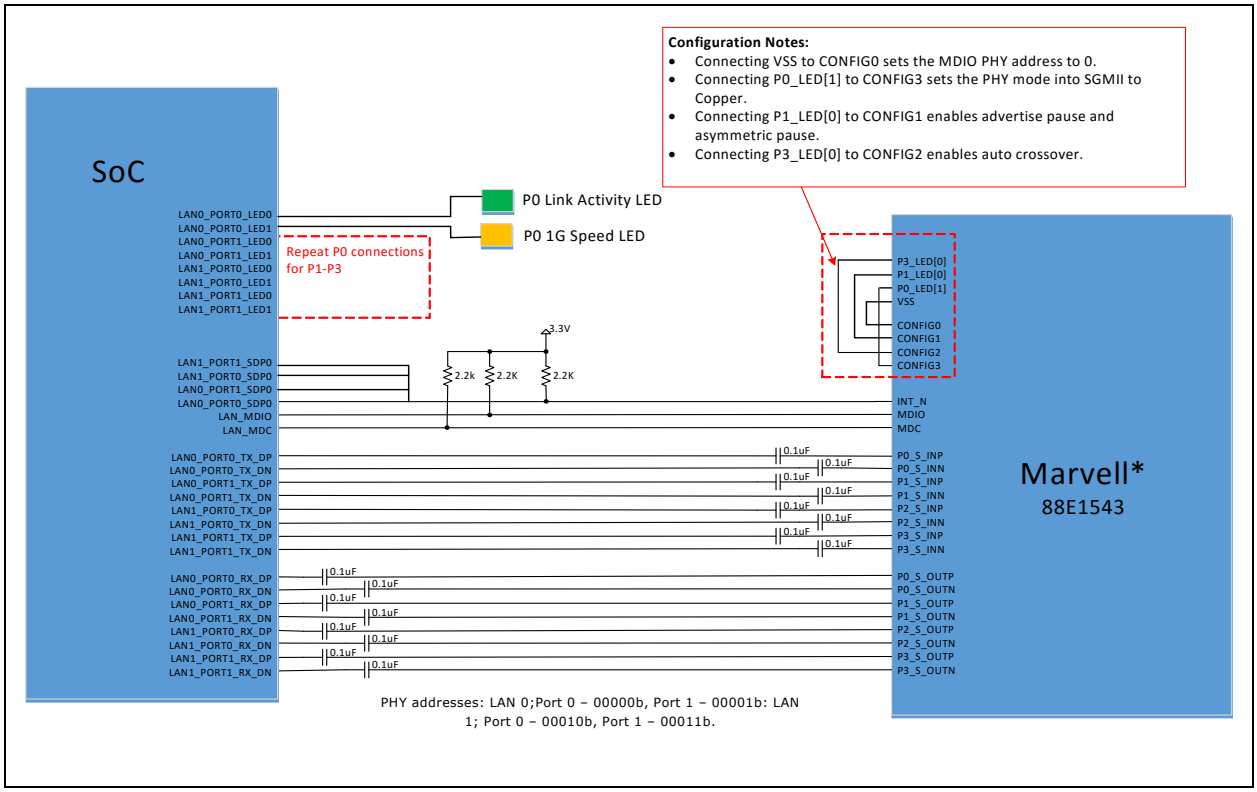
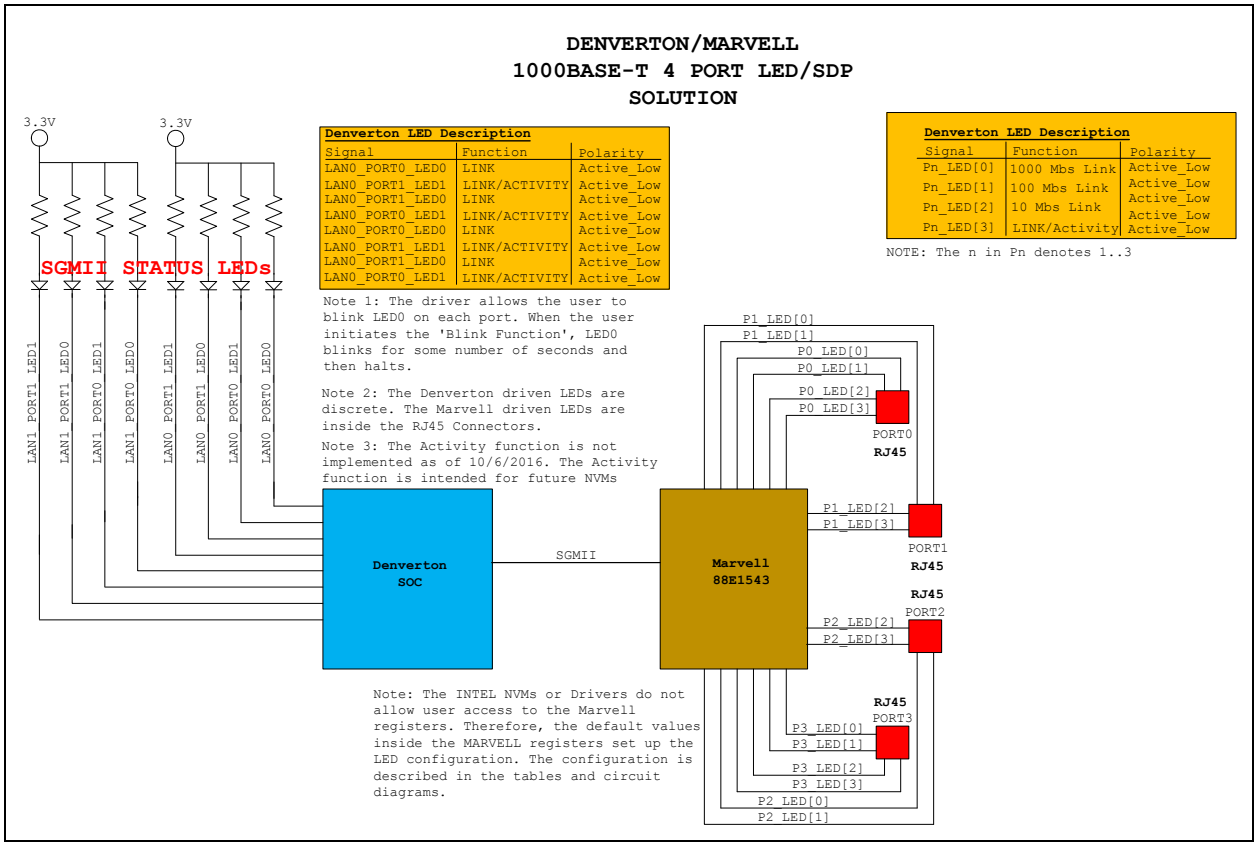


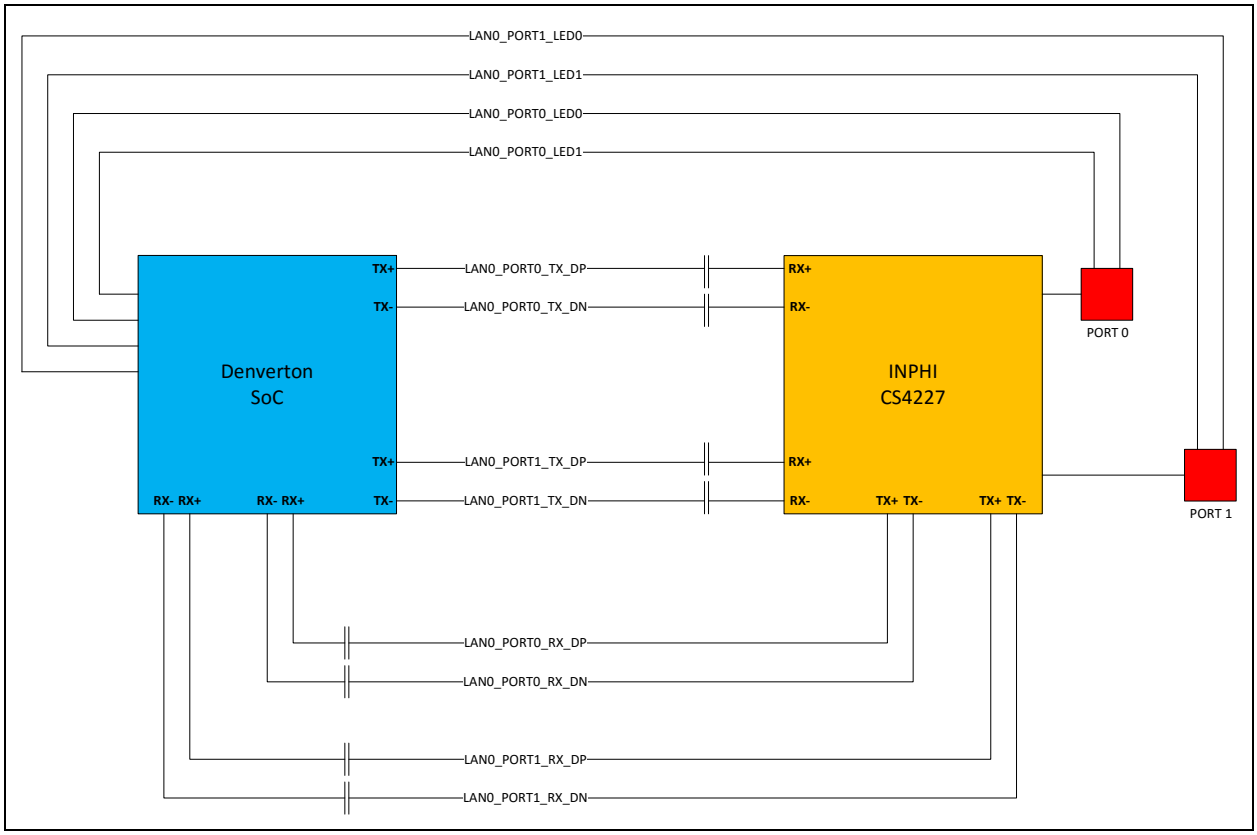
Figure C-10. Alternate LED Solution for Marvell 1543 Configuration



C.5 SoC to SFP+

The SoC to SFP+ design reference is for SFP+ cages through the SFI interface. The channel length on the SFI channels are limited, refer to Section 6.4.8, "LAN Controller SFI Channel Design Guidelines" for SFI channel guidelines. We recommend using the SoC to *Inphi design for most SFP+ applications.

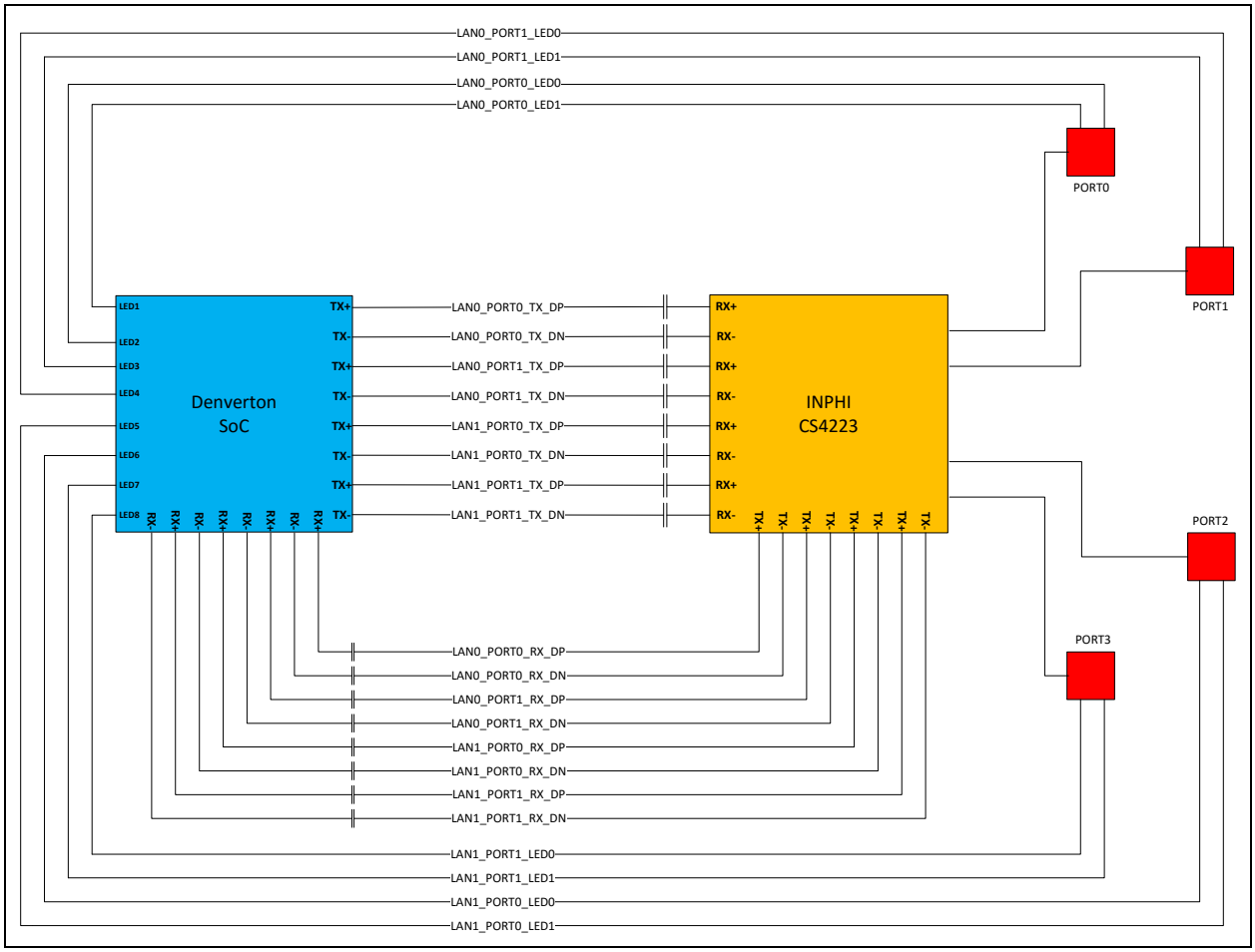
Figure C-11. SoC to *INPHI SFP+ 2 Port Schematic



Notes:

1. The signal names in the schematic match those in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*. If a search is done, for example, on "LAN0_PORT1_RX_DP" in the EDS, the corresponding pin number and signal description will be found.
2. A series of 0.1µF capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. Use X7R quality or better.
3. PORT0 and PORT1 use SFP+ Connectors.

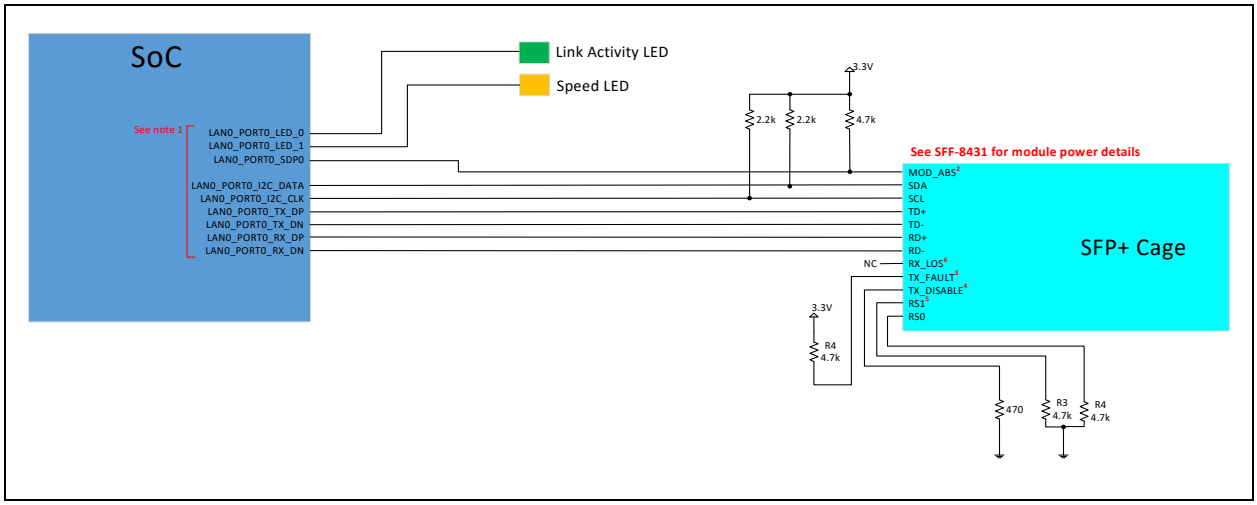
Figure C-12. SoC to *INPHI SFP+ 4 Port Schematic



Notes:

1. The signal names in the schematic match those in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*. If a search is done, for example, on "LAN0_PORT1_RX_DP" in the EDS, the corresponding pin number and signal description will be found.
2. A series of 0.1µF capacitors are recommended as close as possible to the RX differential pair pins for Denverton and Marvell. Use X7R quality or better.
3. PORT0, PORT1, PORT2, and PORT3 use SFP+ Connectors.

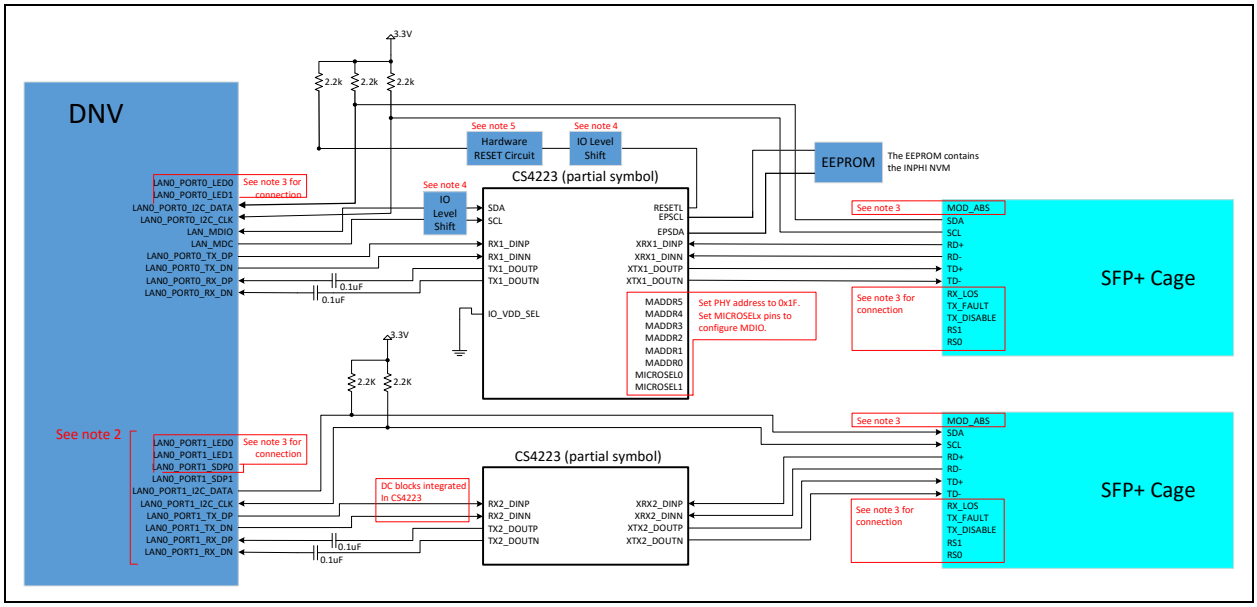
Figure C-13. SoC SFI Connections for SFP+ Cages



Notes:

1. Repeat connections of Port0 for Port1, Port2 and Port3.
2. MOD_ABS is pulled low in the module. Pull high on the host.
3. TX_FAULT is an open drain output and should be pulled high by the host.
4. TX_DISABLE is asserted in the module. Must be pulled low to enable the module.
5. RS1 and RS0 are logically OR'ed with an I2C accessible register to configure module rate. Software must write this register to put the module in a desired state.
6. Leave RX_LOS disconnected.
7. I2C addresses:
   LAN 0; Port 0 – 1010000b, Port 1 – 1010001b
   LAN 1; Port 0 – 1010010b, Port 1 – 1010011b.

Figure C-14. SoC KR Connections to *Inphi Quad Port SFP+ PHY (CS4223)



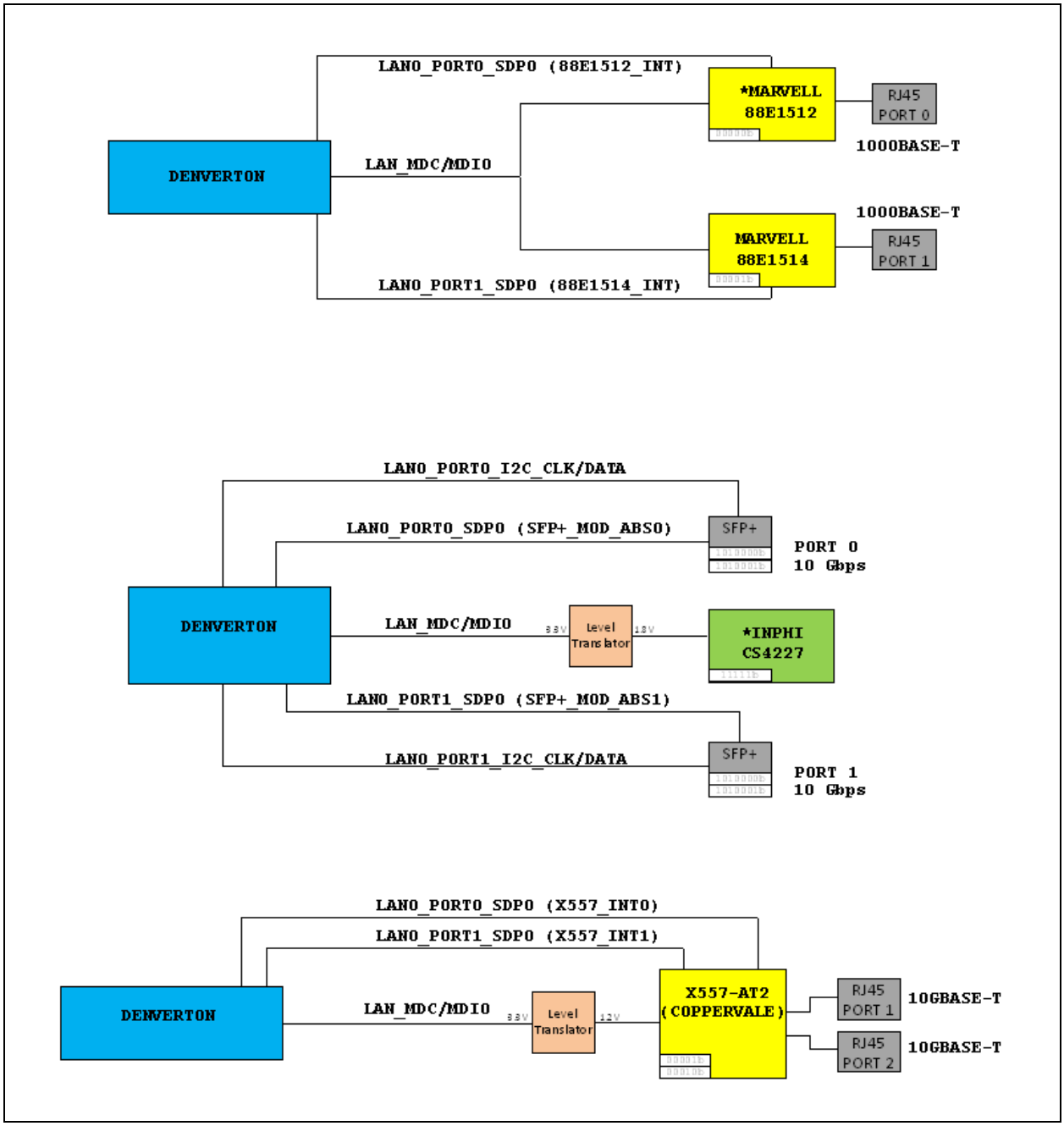
Notes:

1. This is only a partial schematic showing relevant connections to and from the SoC and the Inphi CS4223. Refer to the CS4223 datasheet for other needed connections related to the CS4223.
2. Copy this schematic segment for additional ports.
3. Refer to "SoC_to_SFP+" schematic for these connections.
4. Bi-directional level shift from DNV 3.3V IO levels to 1.8V CS4223 IO levels.
5. Refer to the Inphi CS4223 datasheet for reset requirements.
6. Note that the CS4223 line side connections are facing the host and the host side is facing line side. Note that KR link training is only supported on the line side of the CS4223.
7. I2C addresses:
   LAN 0; Port 0 - 1010000b, Port 1 - 1010001b
   LAN 1; Port 0 - 1010010b, Port 1 - 1010011b.
   Inphi MDIO address 111111b
   Other supporting circuits are needed for the Inphi CS4223.
   These include a 156.25 MHz reference clock, an EEPROM, a 0.9V supply, a 1.8V supply, and a reset circuit.

C.6 SoC to NCSI/MDIO/SMBus

SoC to NCSI/SMBus design reference can apply to any of the previous LAN topologies and provides connectivity to an on-board BMC device. SoC to NCSI multi-drop also applies to an of the previous LAN topologies.

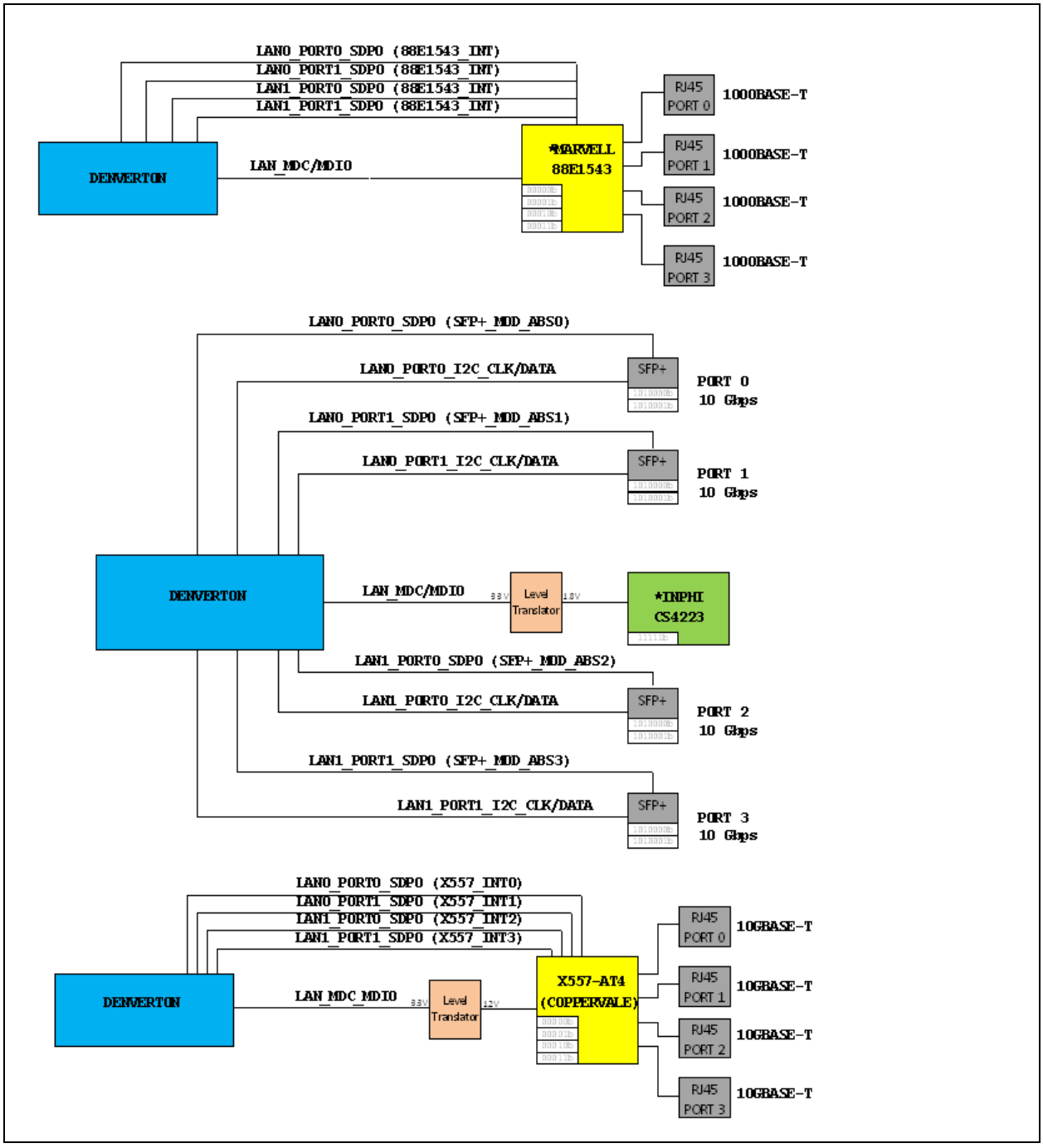
Figure C-15. MDIO/I2C Block Diagram (1 of 2 Figures)



Notes:

1. The signal names in the schematic match those in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*. The only exception are the signal names in parentheses.
2. All 7-bit binary values refer to I2C addresses. All 5-bit binary values refer to MDIO addresses.

Figure C-16. MDIO/I2C Block Diagram (2 of 2 Figures)



Notes:

1. The signal names in the schematic match those in the *Intel® Atom™ Processor C3000 Product Family External Design Specification [EDS], Volumes 1, 2, 3, and 4*. The only exception are the signal names in parentheses.
2. All 7-bit binary values refer to I2C addresses. All 5-bit binary values refer to MDIO addresses.The Marvell has several strapping options. Refer to the data sheet as to how to select these.

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