PRINTED WIRING BOARD

DESIGN FOR

MANUFACTURABILITY

GUIDELINES

Created by the HADCO Product Engineering and Field Application Engineering Teams.

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INTRODUCTION

Welcome to the HADCO PWB Design for Manufacturability Guidelines. The primary focus of HADCO's mission statement is customer satisfaction. It is our belief that there can be no better way to continually improve customer satisfaction than to offer a more reliable, higher quality, more cost effective circuit board. Some industry analysts believe that 20-25% of a PWB's cost could be avoided if proper consideration were given the manufacturing process. We have seen savings of this magnitude and believe that this may be within your realm of possibility. This document presents volume PWB fabrication design guidelines.

At a basic level, a Printed Wiring board is essentially a solution to an interconnection problem. It is not a commodity product. As such, its value to our customers must be continually enhanced. HADCO believes that a major component in the pursuit of this value enhancement is designing for manufacturability.

There are four factors, which influence the cost of circuit board fabrication more than anything else: material utilization, layer quantity, PWB size and yield. This guide focuses on material utilization, and on factors which affect yield throughout the board fabrication process. The information will help you to design your board as cost effective as possible, without compromising quality or reliability.

HADCO is involved in building leading edge and low to high volume product, both in our Tech Centers and in volume facilities. Technologies include: buried and blind vias, PC cards, thick backplane fabrication and assembly, exotic materials, fine lines, high layer count, tight controlled impedance, and more. We will gladly work with you at length about any challenges that you may have before you.

Product that is designed to these criteria will result in high quality boards with the lowest possible manufacturing costs. The design parameters are applicable for all HADCO volume and Tech Center manufacturing facilities. Additional capabilities are available that are not described in this document. Contact HADCO for more specific information.

The design criteria are provided in two classifications; **Preferred** and **Available**.

> **Preferred** criteria will allow the PWB to be manufactured in any volume or Tech Center manufacturing facility.
>
> **Available** criteria may limit the volume capability to specific manufacturing facilities.

Each section opens with a **tutorial subsection**, which will provide a basic understanding for the subject matter. It will then be followed by **detailed design criteria subsection**, which will provide in-depth specifications and guidelines.

Each HADCO manufacturing facility has unique capabilities. These can be discussed with your Sales or Field Application Engineer representative.

HADCO SALES AND TECHNICAL SUPPORT LOCATIONS

Location	Address
Corporate Offices	12A Manor Parkway Salem, NH 03079 603-898-8000
Northeast & International	8C Industrial Way Salem, NH 03079 603-898-8000
Mid-Atlantic	4000 Vine Street Middletown, PA 17057 717-944-9560
Southeast	110 Eagle Springs Drive, Suite C Stockbridge, GA 30281 770-474-6645
Latin America	4673 NW 97th Court Miami, FL 33178 305-436-5434
South Central	525 International Parkway, Suite 495 Richardson, TX 75081 972-235-1112
South West	5020 S. 36th St. Phoenix, AZ 85040 602-268-3461
North Central	5001 W. 80th Street, Suite 495 Bloomington, MN 55437 612-893-1370
Western	425 El Camino Real Santa Clara, CA 95050 408-241-9900
Canada	5401 Eglinton Ave. W., Suite 204 Toronto, Ontario, Canada M9C 5K6 416-626-2020
Asia	Pica Centre 20 Kallang Ave. Singapore 339411 (65) 297-0150

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HADCO MANUFACTURING AND DESIGN FACILITIES

High Volume PWB Manufacturing	Derry	7 Manchester Road Derry, NH 03038 603-432-2004
	Malaysia	Sama-Jaya Free Industrial Zone 93450 Kuching, Sarawak Malaysia 011-60-82363000
	Owego	1200 Taylor Road Owego, NY 13827 607-687-3425
	Phoenix	5020 South 36th Phoenix, AZ 85040 602-268-3461
	Santa Clara	435 El Camino Real Santa Clara, CA 95050 408-241-9900
Technology Development Centers	Tech Center Austin	15508 Bratton Lane Austin, TX 78728 512-246-5600
	Tech Center East	46 Rogers Road Ward Hill, MA 01835 978-372-0200
	Tech Center West	78 Hangar Way Watsonville, CA 95076 408-728-0333
Flex and Rigid Flex	HADCO/Dynaflex	1758 Junction Ave., Suite E San Jose, CA 95112 408-441-8717
Value Added Manufacturing (VAM)	VAM East	10 Manor Way Salem, NH 03079 603-896-2300
	VAM West	425 El Camino Real Santa Clara, CA 408-241-9900
Design Centers Email: hadco_design@hadco.com	Colorado	2004 West 15Th Street, Unit 1 Loveland, CO 80538 970-622-8933
	New Hampshire	8C Industrial Way Salem, NH 03079 603-896-2470
	Texas	1915 North Austin Avenue Georgetown, TX 78626 512-930-2233
	California	1821 Saratoga Avenue, Suite 280 Saratoga, CA 95070 408-366-9030

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PANEL UTILIZATION

PANEL UTILIZATION TUTORIAL

Panelization is the process of positioning one or more Printed Wiring boards (PWB's) on a manufacturing panel and incorporating features to facilitate manufacturing (such as tooling holes, fiducials, coupons, resin vents, panel theiving, etc.). This is one of the highest cost impact factors.

The panel area is divided between these functions:

- Keep-out zones that are required for manufacturing
- Circuit boards (single and arrays)
- Test coupons (such as impedance coupons)
- Circuit board spacing for routing or scoring (depanelization)
- Traces (buss bar traces) added for electroplated edge connectors

The panel area that is available for circuit boards and coupons is called the useable area. The useable area is measured as a percentage (total area for PWB's divided by the total panel area). PWB's are laid out in the useable area, and any area outside the useable area is designated for tooling to optimize manufacturing. A target panel utilization of greater than 70% is considered cost effective material utilization (i.e., lower cost). In order to reduce cost and minimize the amount of unused base material, HADCO offers several manufacturing panel sizes.

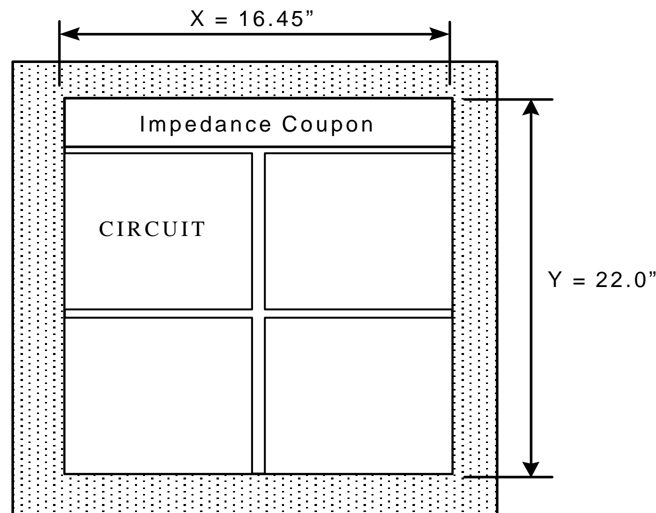

Figure 1 18” x 24” panel example

The following pages will outline the provisions and requirements necessary to best utilize the useable area.

Four general panel modifications reduce the available useable area. These modifications are:

(1) Step-and-repeat requirements
(2) Assembly rails
(3) Provisions for electroplating edge connectors
(4) Coupon requirements

Step-and-repeat

The term 'step-and-repeat' describes the process of reproducing successive images onto a panel. For printed wiring boards without gold-plated edge contacts, the standard step-and-repeat spacing between parts is normally 0.100" to 0.200". A typical lay-up is shown in the following figure.

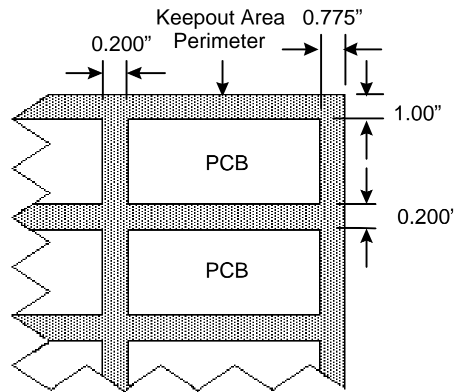

Figure 2 Step-and-repeat without Edge Connectors

Gold-Electroplated Edge Connectors

For Printed Wiring boards with gold-plated edge connectors (a.k.a. tips, fingers, tabs), parts are usually arranged such that the edge connectors are either facing each other or opposite each other when plated on a tip plating line. When the edge connectors are facing each other, the spacing between the part outlines needs to be at least 0.400" minimum. This allows space for tie bars to connect to the connectors for electroplating and to allow room for a shearing operation to separate the pieces. When the edges opposite the edge connectors are facing each other, the space between the parts can be 0.200" since there is no gold plating required in this area.

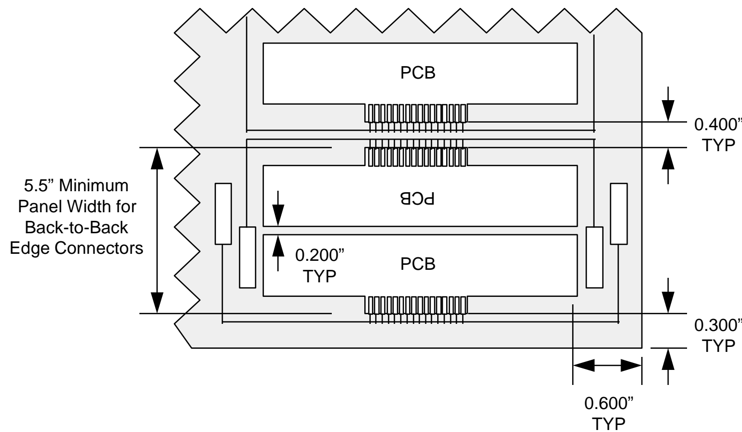

Figure 3 Step-and-repeat with edge connectors

For Printed Wiring boards with recessed gold-plated edge connectors, the same rules apply as those without recessed edge connectors. Panels, which contain edge connectors that can not be plated on the tip plating line, can be plated in the deep gold plating lines that are available at several HADCO facilities.

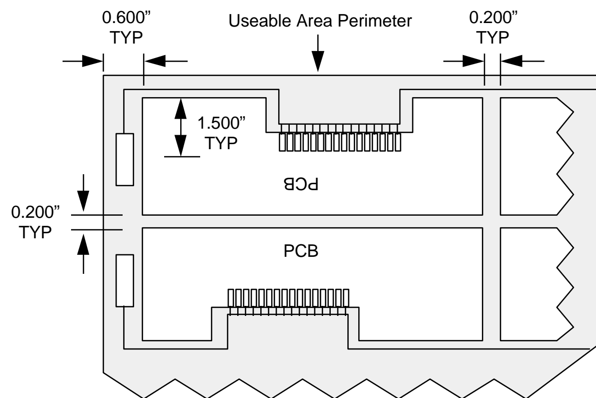

Figure 4 lay-up with recessed edge connectors

Controlled Impedance Coupons

Printed Wiring boards with controlled impedance technology are processed with test coupons as part of the lay-up. When a +/- 10% of nominal impedance tolerance is specified, we recommend using controlled geometry versus controlled impedance (see Controlled Impedance section). This will free area on the panel for parts since the coupons will not be required. It also may allow a smaller panel size to be used. The coupons are typically one-inch wide and are placed along the short end of the panel. A typical arrangement is shown in the following figure.

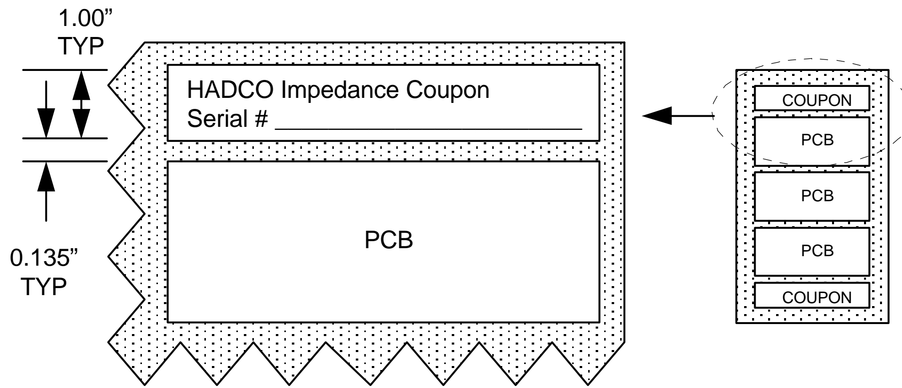

Figure 5 Controlled impedance coupon placement

Assembly Rails

To maximize the number up on a panel when assembly rails are required, the following should be considered. A minimum of a 1.0” border must be maintained around the perimeter of the panel to allow for HADCO’s pinning, coupons, plating clamps, and other assorted targets that are required to tool a panel. It is a common practice for the assembly rail (breakaway) to enter the 0.5” border of the panel, keeping the PWB away from the border. When the rail enters the 0.5” border of the panel, some HADCO tooling features may remain on the rail after processing. This can include, tooling holes, targets, inner layer gates and theiving. These additional features do not generally affect any assembly operations.

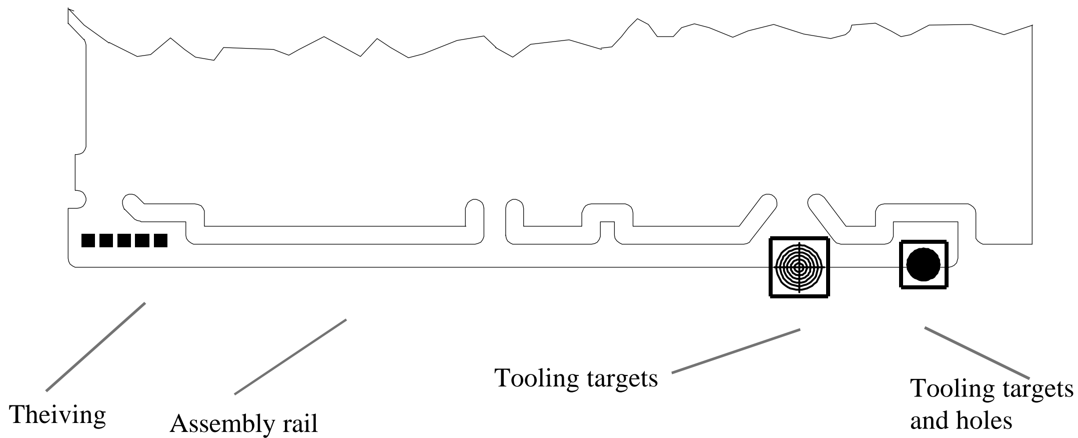

Figure 6 Assembly rail design

Assembly arrays or sub-panels

PWB’s are often required to be step-and-repeated onto an array for assembly. The assembly array database should be provided to HADCO to ensure that the correct array is provided to the assembler.

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PANEL UTILIZATION DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
General:		
Panel sizes: (inches)	18 x 24	12 x 18, 12 x 21, 12 x 24, 12 x 27, 14 x 16, 14 x 18, 14 x 21, 14 x 24, 14 x 27, 16 x 18, 16 x 21, 16 x 24, 16 x 27, 18 x 21, 18 x 26, 18 x 27, 19 x 25 20 x 21, 21x24, 21 x 25, 21x27, 22 x 24

STANDARD PANEL SIZES

Use the following table to determine the maximum, single 1-up PWB's that can fit into a panel. The 18"x24" panel is preferred because it is the most common panel size in the industry. The PWB dimensions should be optimized to maximize the panel utilization. This will provide the most real estate for circuitry and component mounting.

Panel Sizes (mm)	Useable Area (mm)	Panel Sizes (in)	Useable Area (in)
305 X 457	265 X 406	12 X 18	10.45 X 16
305 X 533	265 X 482	12 X 21	10.45 X 19
305 X 610	265 X 305	12 X 24	10.45 X 22
355 X 406	316 X 355	14 X 16	12.45 X 14
355 X 457	316 X 406	14 X 18	12.45 X 16
355 X 533	316 X 482	14 X 21	12.45 X 19
355 X 610	316 X 559	14 X 24	12.45 X 22
355 X 686	316 X 635	14 X 27	12.45 X 25
406 X 457	367 X 406	16 X 18	14.45 X 16
406 X 533	367 X 482	16 X 21	14.45 X 19
406 X 610	367 X 559	16 X 24	14.45 X 22
406 X 686	367 X 635	16 X 27	14.45 X 25
457 X 533	417 X 482	18 X 21	16.45 X 19
457 X 610	417 X 559	18 X 24	16.45 X 22
457 X 660	417 X 610	18 X 26	16.45 X 24
457 X 686	417 X 635	18 X 27	16.45 X 25
482 X 635	423 X 594	19 X 25	17.025 X 23.4
508 X 533	468 X 482	20 X 21	18.45 X 19
533 X 610	494 X 559	21 X 24	19.45 X 22
533 X 635	494 X 584	21 X 25	19.45 X 23
533 X 686	496 X 640	21 X 27	19.55 X 25.2
610 X 711	570 X 610	24 X 28	22.45 X 26

Table 1 Panel sizes & useable area

MATERIALS AND LAYER STACKUP

MATERIALS & LAYER STACKUP TUTORIAL

Materials

HADCO generally manufactures PWB's using Epoxy-glass (FR-4) dielectrics and copper foil. PWB's are constructed from three basic material types; Copper foil, prepreg and cores.

- **Copper foil**: Sheets of copper foil are incorporated into the outer layer of the PWB placing it on the prepreg to create the outer layers. Outer layers are generally constructed using 0.5 oz. copper. Internal layers are constructed with copper that is specified on the fabrication print. 1 oz. foil is generally preferred. 0.5 oz. is commonly used for signal layers with fine lines. 2 oz. copper is used for power planes where there is a high DC current.
- **Prepreg**: This is commonly called B-stage. This is semi-cured glass-epoxy material. There is no copper attached to this material.
- **Core**: This is commonly called C-stage. This is fully-cured glass-epoxy material with copper laminated to both sides. This is used for internal layers. It is occasionally used for outer layers, but is not preferred. A core is constructed of one (single-ply) or two (or more plies of two-ply) prepreg layer and two layers of copper foil. Single ply is considered the preferred core construction and has better dimensional stability.

More exotic board materials are available and are discussed in the Advanced Technologies section. Combinations of glass-epoxy and exotic materials can provide cost effective, high performance PWB's.

Layer Stackup

Layer stackups are determined by mechanical and electrical requirements. This information is detailed on the PWB Fabrication drawing. Only the key mechanical attributes should be specified. These are generally:

- Overall PWB thickness and tolerance
- Measurement reference locations (copper to copper, glass to glass, etc.)
- Impedance
- Critical layer-to-layer spacing (and tolerance)

HADCO prefers to use Foil versus all Core constructions. This is the most cost-effective approach because both sides of the adjacent internal layers are imaged and etched together. This improves productivity and yield. The outer layer circuitry is not created until after drilling.

The following guidelines should be used when determining multilayer constructions:

- To promote even etch distribution and minimize warp & twist, design balanced constructions that are symmetrical from the lay-up's center outward.
- Whenever possible, only one core thickness should be used.
- Actual layer-to-layer spacing will vary based on whether each side has signal or power planes and the copper weight used for those layers.

- The overall board thickness should not be specified less than +/- 10%.
- Boards that are thicker than 0.100" and have more than eight layers should utilize high Tg material when utilized in high operating temperature environments or in high availability or reliability application. This will lower the PWB Z-exis thermal expansion rate and create a more reliable PTH's.
- Specify how the overall board thickness should be measured. For example specify that it should be measured over copper or over laminate. Edge connector boards should be measured over copper to ensure that the correct insertion thickness is obtained.
- Single ply construction should be allowed.
- Cores should have the same copper weight on both sides to ensure good trace etching tolerance.

MATERIAL DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Materials:		
Laminate types available:	FR-4 (Tg = 135°C minimum)	FR-4 (Tg = 170°C minimum)
Foil weight: (inner layer)	1/2, 1 ounce	2,3 ounce
Foil weight: (outer layer)	1/2 ounce	1 ounce
Dielectric & PWB thickness :		
Minimum overall board thickness: (As measured over metal)	0.031"	0.016"
Maximum overall board thickness: (As measured over metal)	0.150"	0.250"
Thickness tolerance:	+/- 10%	+/- 8%
Warp and Twist	1%	0.7%, 0.5%
Minimum dielectric spacing:	Cores: 0.005" Prepregs: 0.004"	Cores: 0.002" Prepregs: 0.004"
Minimum PC Card dielectric spacing:	Cores: 0.002" Prepregs: 0.002"	

FR4 Material Tolerances

THICKNESS RANGE (inches)	TOLERANCE (inches)
0.0020 to 0.0069	+/- 0.0005
0.0070 to 0.0099	+/- 0.0007
0.0100 to 0.0139	+/- 0.0010
0.0140 to 0.0209	+/- 0.0020
0.0210 to 0.0339	+/- 0.0025
0.0340 to 0.0560	+/- 0.0040

Table 2 FR4 laminate (core) tolerances

THICKNESS RANGE (inches)	TOLERANCE (inches)
0.0010 to 0.0029	+/- 0.0003
0.0030 to 0.0074	+/- 0.0005
0.0075 to 0.0109	+/- 0.0010
0.0110 to 0.0139	+/- 0.0015
0.0140 to 0.0199	+/- 0.0020
0.0200 to 0.0299	+/- 0.0025

Table 3 FR4 laminate prepreg tolerances

MULTI-PLY GLASS STYLES	SINGLE PLY STYLES
1060 1080 2113 2116 7628	6000 8000

Table 4 FR4 glass styles

COPPER WEIGHT (ounce)	THICKNESS (inches)	THICKNESS (microns)
0.5	0.00050	20
1	0.00120	48
2	0.00260	104

Table 5 Copper foil thickness (after processing)

Material Type	Transition Temperature
Standard FR4	≥ 130° C
High Tg FR4	≥ 160° C

Table 6 FR4 Material glass transition temperatures

MULTILAYER CONSTRUCTION DESIGN GUIDELINES

The following guidelines should be used when designing multilayer constructions:

- Design balanced constructions that are symmetrical from the lay-up's center outward to promote even etch distribution and minimize warp & twist.
- Use only one core thickness whenever possible.
- The maximum B-Stage opening between C-Stages is 0.021".
- High Tg materials should be used in high temperature or high reliability applications.
- Each outer layer is typically a signal layer built using 0.5 ounce copper.
- The overall board thickness should not be specified less than +/- 10%.
- Warp and twist should be specified to be ≥ 1%.

Standard PWB Constructions

The following examples are the most cost-effective constructions for common 0.062” and 0.093” thick PWB’s. These should be used for PWB’s where specific layer to layer spacing is not required. Other cost effective PWB thickness’ can be calculated for you by HADCO. All measurements are taken over copper. The impedance values for each of these constructions are provided in the Impedance section.

Note: - Constructions are not drawn to scale.
-All dimensions are in inches/

KEY	
P	Power
G	Ground
S	Signal

Table 7 Construction key

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0590”		0.062 +/- .006”
2	S	--------------------------------	0.5	

Figure 7 Two Layers (Double-sided)

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0154”		
2	G	--------------------------------	1	
		0.0230”		0.062 +/- .006”
3	P	--------------------------------	1	
		0.0154”		
4	S	--------------------------------	0.5	

Figure 8 Four Layers

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0063”		
2	G	--------------------------------	1	
		0.0140”		
3	S	--------------------------------	1	
		0.0110”		0.062 +/- .006”
4	S	--------------------------------	1	
		0.0140”		
5	P	--------------------------------	1	
		0.0063”		
6	S	--------------------------------	0.5	

Figure 9 Six Layers

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0055”		
2	S	--------------------------------	1	
		0.0081”		
3	G	--------------------------------	1	
		0.0072”		
4	S	--------------------------------	1	
		0.0081”		0.062 +/- .006”
5	S	--------------------------------	1	
		0.0072”		
6	P	--------------------------------	1	
		0.0081”		
7	S	--------------------------------	1	
		0.0055”		
8	S	--------------------------------	0.5	

Figure 10 Eight Layer

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0046”		
2	G	--------------------------------	1	
		0.0055”		
3	S	--------------------------------	1	
		0.0045”		
4	S	--------------------------------	1	
		0.0055”		
5	P	--------------------------------	1	
		0.0060”		0.062 +/- .006”
6	G	--------------------------------	1	
		0.0055”		
7	S	--------------------------------	1	
		0.0045”		
8	S	--------------------------------	1	
		0.0055”		
9	P	--------------------------------	1	
		0.0046”		
10	S	--------------------------------	0.5	

Figure 11 Ten Layers

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0063”		
2	G	--------------------------------	1	
		0.0071”		
3	S	--------------------------------	1	
		0.0065”		
4	S	--------------------------------	1	
		0.0071”		
5	P	--------------------------------	1	
		0.0072”		
6	S	--------------------------------	1	
		0.0071”		0.093 +/- .009”
7	S	--------------------------------	1	
		0.0072”		
8	G	--------------------------------	1	
		0.0071”		
9	S	--------------------------------	1	
		0.0065”		
10	S	--------------------------------	1	
		0.0071”		
11	P	--------------------------------	1	
		0.0063”		
12	S	--------------------------------	0.5	

Figure 12 Twelve Layers

LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0055”		
2	S	--------------------------------	1	
		0.0059”		
3	G	--------------------------------	1	
		0.0053”		
4	S	--------------------------------	1	
		0.0059”		
5	S	--------------------------------	1	
		0.0053”		
6	P	--------------------------------	1	
		0.0059”		
7	S	--------------------------------	1	
		0.0045”		0.093 +/- .009”
8	S	--------------------------------	1	
		0.0059”		
9	G	--------------------------------	1	
		0.0053”		
10	S	--------------------------------	1	
		0.0059”		
11	S	--------------------------------	1	
		0.0053”		
12	P	--------------------------------	1	
		0.0059”		
13	S	--------------------------------	1	
		0.0055”		
14	S	--------------------------------	0.5	

Figure 13 Fourteen Layers

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LAYER	TYPE	CONSTRUCTION	CU WEIGHT	OVERALL THICKNESS
1	S	--------------------------------	0.5	
		0.0049”		
2	G	--------------------------------	1	
		0.0045”		
3	S	--------------------------------	1	
		0.0045”		
4	S	--------------------------------	1	
		0.0045”		
5	P	--------------------------------	1	
		0.0053”		
6	S	--------------------------------	1	
		0.0045”		
7	S	--------------------------------	1	
		0.0053”		
8	G	--------------------------------	1	
		0.0045”		0.093 +/- .009”
9	P	--------------------------------	1	
		0.0053”		
10	S	--------------------------------	1	
		0.0045”		
11	S	--------------------------------	1	
		0.0053”		
12	G	--------------------------------	1	
		0.0045”		
13	S	--------------------------------	1	
		0.0045”		
14	S	--------------------------------	1	
		0.0045”		
15	P	--------------------------------	1	
		0.0049”		
16	S	--------------------------------	0.5	

Figure 14 Sixteen Layers

BURIED CAPACITANCE™ DESIGN GUIDELINES

Capacitance without Capacitors

Printed Wiring board design is a tug-of-war between maximizing performance and minimizing cost. Conventional wisdom says when you achieve one you sacrifice the other. But a new technology takes a big step towards refuting this notion by enabling engineers to improve high frequency EMI performance and system quality while reducing the impact on system cost.

Patented and licensed worldwide, Buried Capacitance™ (BC), utilizes ZBC-2000™ laminate. It is an advanced board manufacturing technique in which distributed decoupling capacitance is achieved by embedding thin dielectric layers within the board between adjacent power planes. This technique makes virtually all discrete decoupling capacitors unnecessary, thereby clearing the board space and enabling designers to design boards that can have greater functionality or a reduced size. More detailed design information can be obtained from the "Buried Capacitance Design Guide".

Preferred Buried Capacitance Constructions

The following figures present common Buried Capacitance constructions. Please consult the Buried Capacitance Design Guide for specifics on power and ground plane orientation. The most common sequences are shown in the following figures.

-All dimensions are in inches

KEY	
P	Power
G	Ground
S	Signal
LYR	Layer Number

LYR	Type	Layer / Dielectric	Cu	Overall
1	S	--------------------------------	0.5	0.062 +/- .006"
		0.0063"		
2	G	--------------------------------	1	
		0.002"		
3	P	--------------------------------	1	
		0.0072"		
4	S	--------------------------------	1	
		0.0018"		
5	S	--------------------------------	1	
		0.0072"		
6	G	--------------------------------	1	
		0.002"		
7	P	--------------------------------	1	
		0.0063"		
8	S	--------------------------------	0.5	

Figure 15 Eight Layers (Buried Capacitance)

Layer	Type	Dielectric	Copper	
1	S		0.5	
		0.0063”		
2	G		1	
		0.0020”		
3	P		1	
		0.0053”		
4	S		1	
		0.0071”		
5	S		1	
		0.0045”		0.062 +/- .006”
6	S		1	
		0.0071”		
7	S		1	
		0.0053”		
8	G		1	
		0.0020”		
9	P		1	
		0.0063”		
10	S		0.5	

Figure 16 Ten Layers (Buried Capacitance)

Layer	Type	Dielectric	Copper	
1	S		0.5	
		0.0049”		
2	G		1	
		0.0020”		
3	P		1	
		0.0039”		
4	S		1	
		0.0049”		
5	S		1	
		0.0039”		
6	G		1	
		0.0049”		0.062 +/- .006”
7	P		1	
		0.0039”		
8	S		1	
		0.0049”		
9	S		1	
		0.0039”		
10	G		1	
		0.0020”		
11	P		1	
		0.0049”		
12	S		0.5	

Figure 17 Twelve Layers (Buried Capacitance)

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TRACES, PADS & CONDUCTIVE FEATURES

TRACES, PADS & CONDUCTIVE FEATURES TUTORIAL

Line width and space

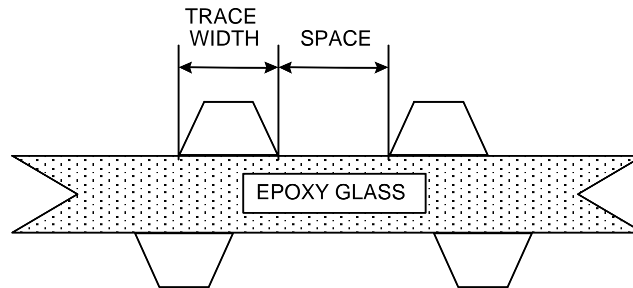

Figure 18 Line width & spacing measurement

The required line width and space is established in the provided CAD database. The line width should be measured at the base of the trace. This is much easier to measure and is provides a more repeatable measurement. The CAM database will be modified to compensate the trace width of the production artwork for the manufacturing processes.

Inner layer features are easier to reproduce, than outer layer features. Inner layer features are exposed to less processing steps than outer layer features.

Thieving

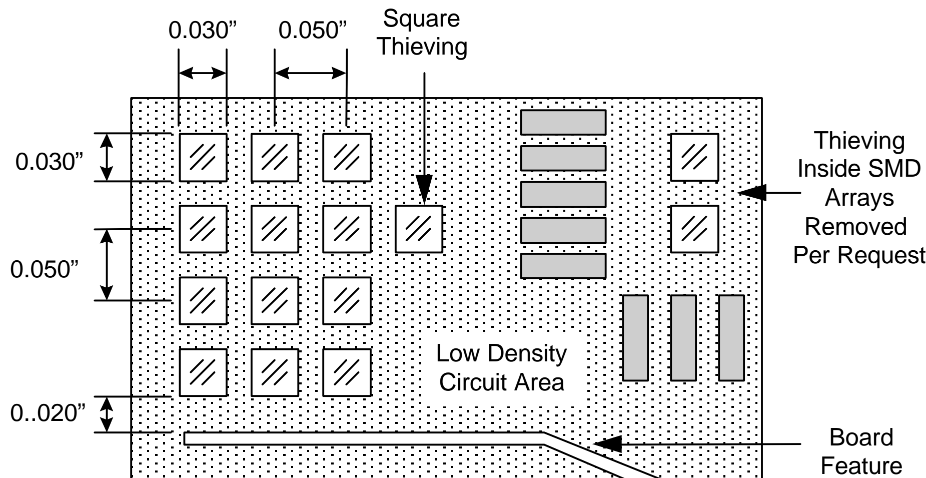

Figure 19 Square Thieving

Outer layer copper features are created by imaging a base pattern and plating copper to a specified thickness. The pattern plating process is very dependent on the uniformity of the copper features on the outer layers. Areas that have a very small amount of copper (like isolated single traces) will plate a very thick amount of copper on those features. Other areas that have uniform density will have a plating thickness that will be within the specified thickness. Non-functional thieving pads can be added to low-density areas to even out the copper distribution. This is called thieving. Thieving should be incorporated

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during the PWB layout to ensure that you will receive identical coverage from all suppliers. HADCO can also automatically thieve the inner and outer layers with our CAM system.

Pads, drilled holes and power plane clearance

The drilled hole to power plane distance is critical to ensure that the plating in the hole will not short to adjacent traces or planes.

A plated thru hole connects to traces through a pad. Pads may connect to one or more traces. The target pad and drilled hole have manufacturing tolerances associated with them. The following equation is used to calculate the required pad size based on a drilled hole size:

Pad diameter = Drilled hole diameter + 2 x (annular ring) + manufacturing tolerance

Drilled hole diameter	= This will be discussed in the next section
	= Finished nominal hole size + plating manufacturing compensation
Annular ring	= The distance between the drilled hole and edge of pad
Manufacturing tolerance	= Pad etching and drilled hole locational tolerance

EXAMPLE:

The design requires a 0.038” +/- .003” finished plated through hole with a 0.001” annular ring.
What pad diameter should be used for the inner and outer layers?

Outer layer pad diameter	= (0.038” + 0.005”) + 2 x (0.001”) + 0.010”
	= 0.055”
Inner layer pad diameter	= (0.038” + 0.005”) + 2 x (0.001”) + 0.012”
	= 0.057”

The clearance between the hole and the power plane is essential to ensure that the plating in the through hole does not wick along fiberglass bundles and short to the plane. The power plane clearance is determined from the following equation.

Plane Clearance = Drilled hole diameter + 2x (annular ring) + 2 x (power plane clearance)

EXAMPLE:

The design requires a 0.038” +/- .003” finished plated through hole with a 0.001” annular ring. The specification requires a 0.010” pad to plane clearance and is using an OSP surface finish.
What power plane clearance anti-pad should be used?

Power plane clearance	= (0.038” + .005”) + 2 x (0.001”) + 2 x (0.010”)
	= 0.065”

Annular Ring

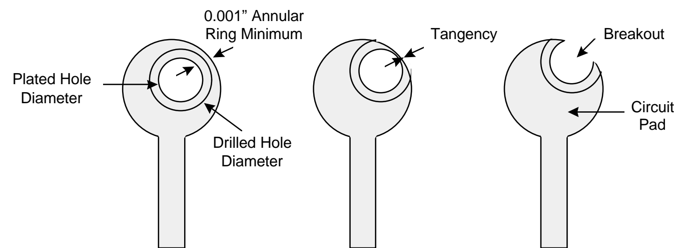

Figure 20 Annular Ring / Tangency / Breakout

Annular ring specifies the distance between the worst case drilled hole to pad distance. This can be specified with a finite distance. It can also be specified as tangent to, or the hole may breakout of the pad. Non-critical hole to trace areas should allow the holes to have a 25% breakout. Critical hole to trace distances should be specified to be tangent.

The manufacturing tolerance will be smaller for outer layers than for inner layers. This is because the outer layer image is registered to the actual drilled holes.

Non-functional pad removal

Pads that do not connect to traces are not required on inner layers. They should be removed to increase drill life (reduce drill cost). This is called non-functional pad removal. Removal of the unused pads will not affect the board reliability. Non-functional pad removal should be specified on the fabrication drawing or specification.

Teardropping

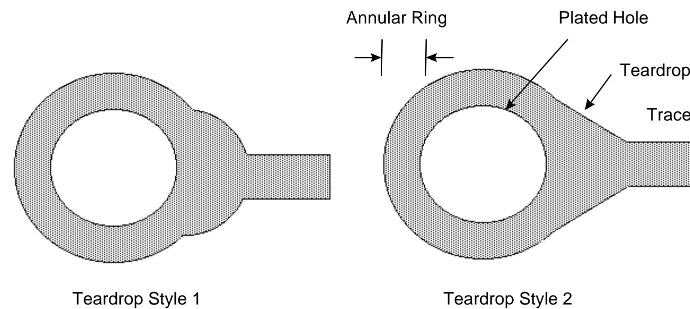

Figure 21 Pad-to-trace teardrop

The drilled hole may finish tangent to the side of the pad where the trace connects to the pad. An extension to the pad should be added at the trace to pad intersection to ensure that the hole will not create a possible open at this point. This is called teardropping. The teardrop addition should extend 0.005" onto the trace.

Circuit to pad connections

The preferred method of connecting a circuit to a pad is to have the vector enter the pad terminating at the center of the pad without any bends or turns while it is in the pad. If the pad is square it is preferred that the circuit does not run along the side of the pad, 0.001" or 0.002" mils from the pad, and then enter at the center of the pad.

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It is also possible to have the circuit run up the side of a square pad and enter at the center, but the distance between the circuit and the side of the pad should be equal to the nominal spacing of the layer.

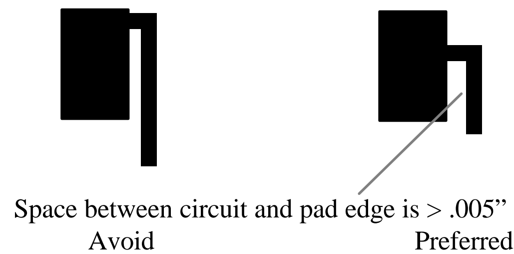


Figure 22 Same pad to trace spacing

If the same net spacing is less then 4 mils along the edge of a surface mount pad, it can cause excessive amounts of design rule violations and processing problems like, flaking resist that will re-deposit causing pin holes, damaged SMD pads or cut circuits.

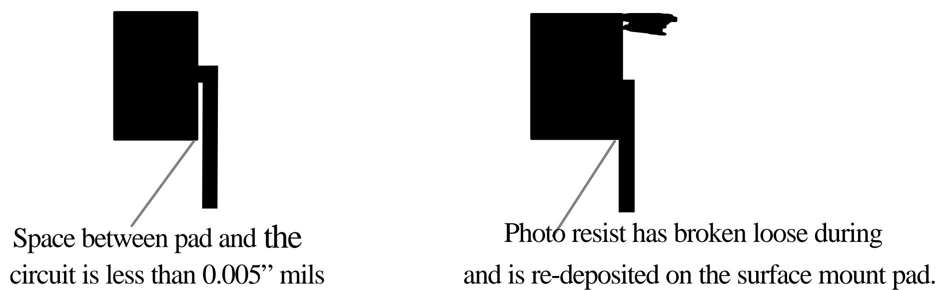


Figure 23 Photo resist re-deposit example

It is not a good design practice when the circuits do not enter on the center axis of a round pad, but this can cause flares to be off center and cause false errors in the design rule checks, spacing problems, and possibly shorts.

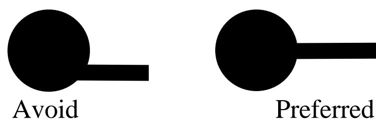


Figure 24 Off-center trace connections to a round pad

Dangling Traces

Trace segments that stub from a pad or trace that do not connect to another pad are called dangling traces. These cause problems during the manufacturing process because they look like a broken trace. These cause false errors during manufacturing. These should be removed during the post rout clean up. We will ask to remove these during the CAM process.

Spacing

Feature to feature spacing should be considered between all copper features. This includes:

- Hole to pad
- Pad to pad
- Pad to trace
- Trace to trace (same net and different nets)

- Hole to hole
- PWB edge to copper

In some designs same net spacing violations can cause functional problems.

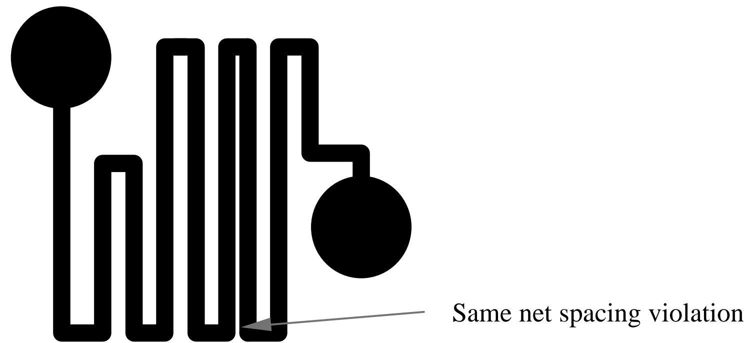


Figure 25 Same net spacing

Spacing design rule checks should not allow same net spacing violations to pass.

Line widths

Circuits should be drawn with one vector that terminates at another vector or at a pad. Circuits drawn with more than one vector, which do not terminate together, can result in reduced line widths. These types of line width reductions can not be caught with our design rule checks.

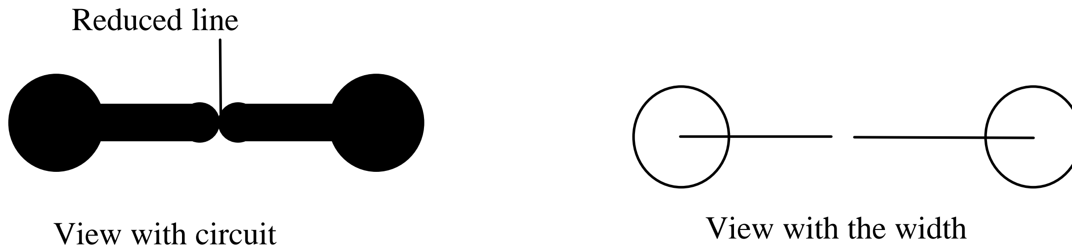


Figure 26 Wrong vector terminations

The width of circuits should be defined by 1 vector and not drawn with 2 or more. This will prevent false errors while running the design rule checks.

Figure 27 Correct vector terminations

Power plane clearance and thermal pads

Sufficient clearance (anti-pad) must be provided between a pad and the internal power planes to ensure that copper plating from the via won't provide a conduit which can create a short circuit.

 © HADCO Corporation

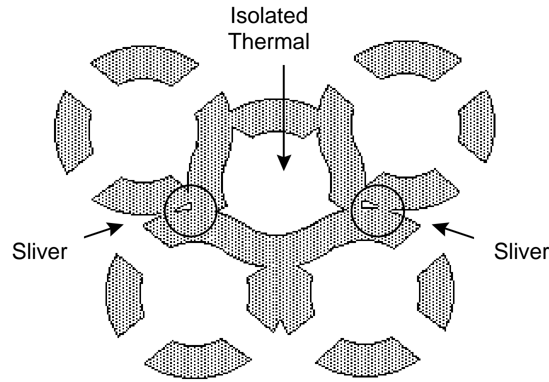


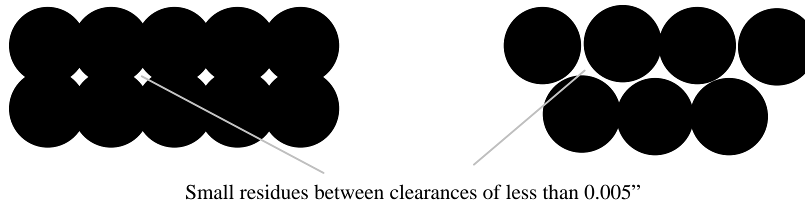
Figure 28 Avoid thermal isolation & slivers of copper

Thermal relief pads patterns should provide a long and wide enough spoke to ensure that all spokes are connected. Care should be taken to ensure that power planes areas do not become isolated after the thermal relief pads are placed and etched. Small slivers of copper should be removed. These may flake during fabrication and create shorts in another location when they re-deposit on a layer. The designer should be sure to check these in the CAD system prior to releasing the final design.

Clearance Pads

Clearance pads (anti-pads) keep the plane away from the plated through hole to ensure that the copper plating does not wick along glass fibers between the hole and plane. This wicking can create a short circuit between the hole and plane after many hours of operation due to CAF. This function is called electro-migration.

Clearance sizes that are too large can cause areas between clearances to have webs, or residues of less than 0.005”. Small webs can break loose, dangle or redeposit and enter a clearance during the inner layer process and cause shorts.



Small residues between clearances of less than 0.005”

Figure 29 Clearance pad spacing

Clearance pads that may surround a thermal must maintain a minimum web between them to maintain a connection, after etch, between the surrounded thermal and the rest of the plane.

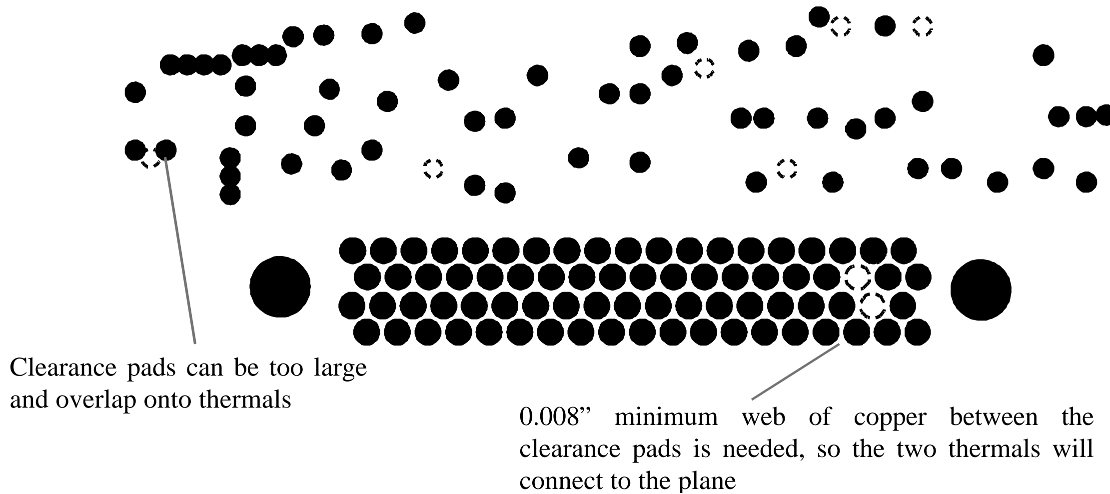


Figure 30 Clearance pad placement

Direct connect vias (No thermal pad)

Direct connection of holes to a plane should include a clearance anti-pad half of the diameter of the hole placed at these locations. This will reduce the amount of copper that needs to be drilled, and will result in less drill breakage of smaller drills.

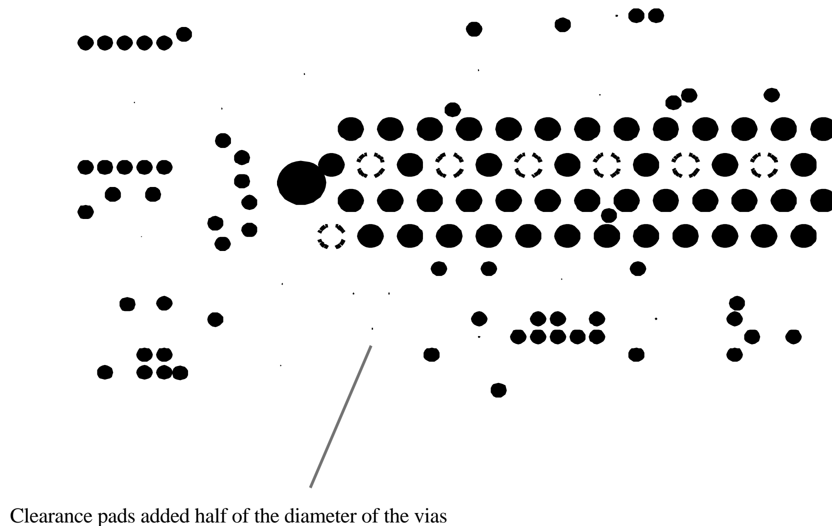


Figure 31 Direct connect vias

Voltage plane separation

Voltage plane separation on the same plane (split planes) should be sufficient to ensure that electrical properties are maintained. The spacing should be no closer than 0.010".

Thermals or plated holes should not enter, or touch the separators. Plane separators will draw on top of the thermals and cause poor or no connection of the thermal to the plane.

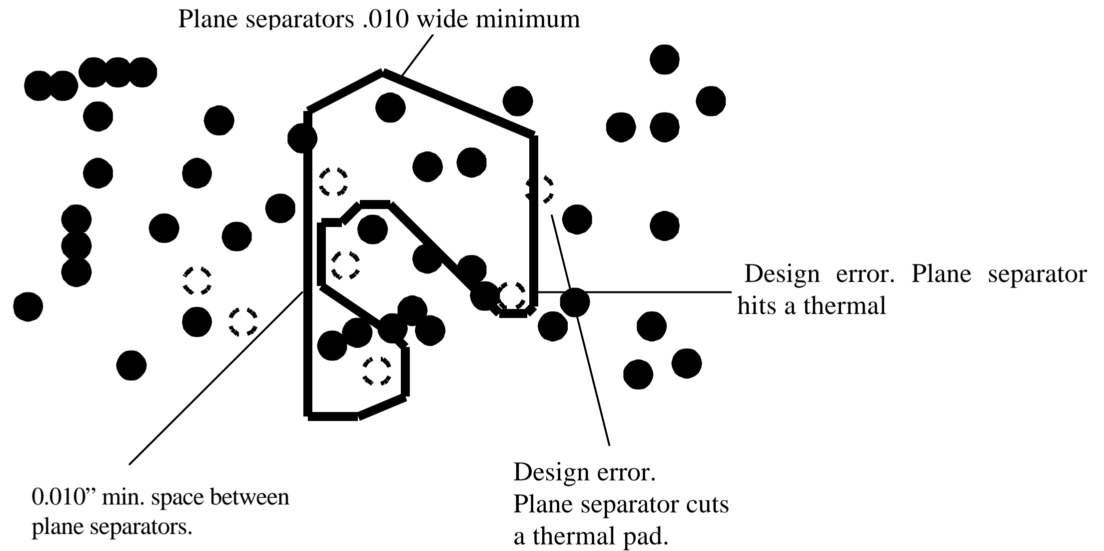


Figure 32 Adjacent plane separation

Crosshatch

Crosshatch of plane layers is not recommended in most cases. Some designs may need some sort of cross hatch of the planes to attempt to reduce warpage. If needed, the crosshatch should be done with spacing between features of no less than .010" square. Feature spacing of less than .010", may cause the dry film to flake off, or not be totally resolved during processing. Preferred minimum spacing between vectors to create a crosshatch is .025. All vectors used to cross hatch should terminate at another vector. If they do not terminate, it will result in a lot of false errors when running the design rule checks.

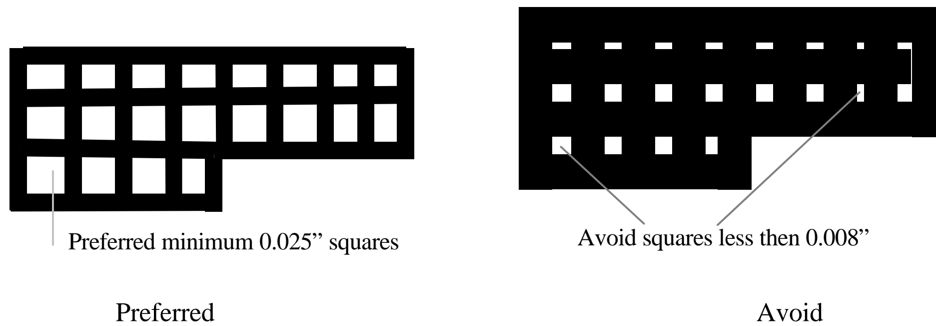
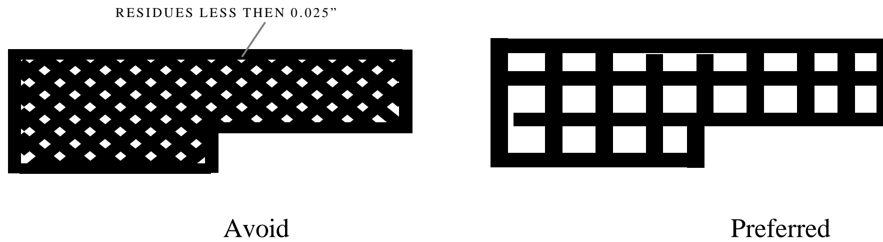


Figure 33 Plane crosshatching

Keep cross hatched drawn areas as vertical and horizontal lines. Do not run them at 45 degrees. These may flake off during processing, and may cause scrap, rework and false design rule violations in CAM.



Avoid Preferred

Figure 34 Plane crosshatching

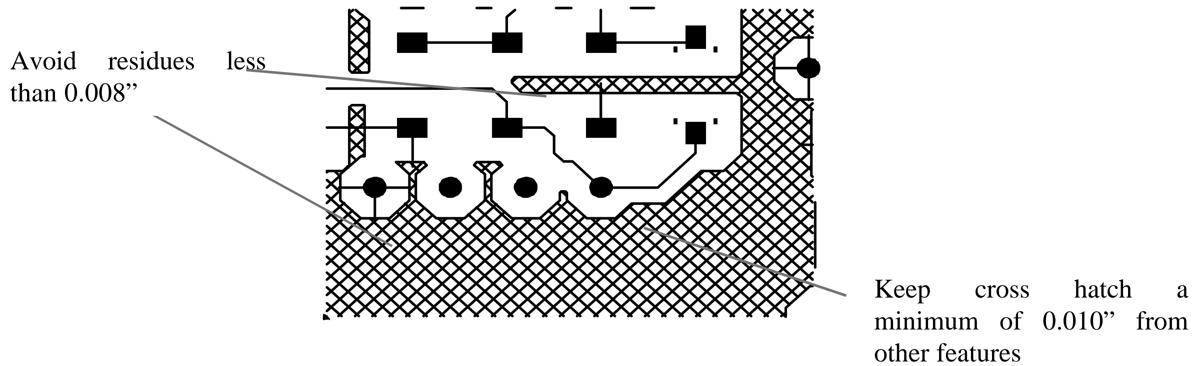


Figure 35 crosshatching example

Copper in cutouts and low pressure areas

Areas on a ground plane that have large open areas, in some cases, cannot be completely filled in during the multilayer press process. PWB's that contain higher layer counts of plane layers, with the open areas in the same location on each plane, are the most likely to not fill with resin.

For example, a PWB contains 6 plane layers. Each of these planes has a large area that does not have copper. This area in the same location on the entire plane layers. Using 1 oz. copper on the planes will result in the thickness before press in the low-pressure areas, to be 0.008" less then the copper filled area that surrounds this open area. This type of design relies on the resin flow to fill these areas. The larger the low pressure area, the more possible it is that the prepreg will not completely fill these areas. After lamination, these low-pressure areas appear to be delaminated, when in fact, there was not enough prepreg to fill this area in the first place.

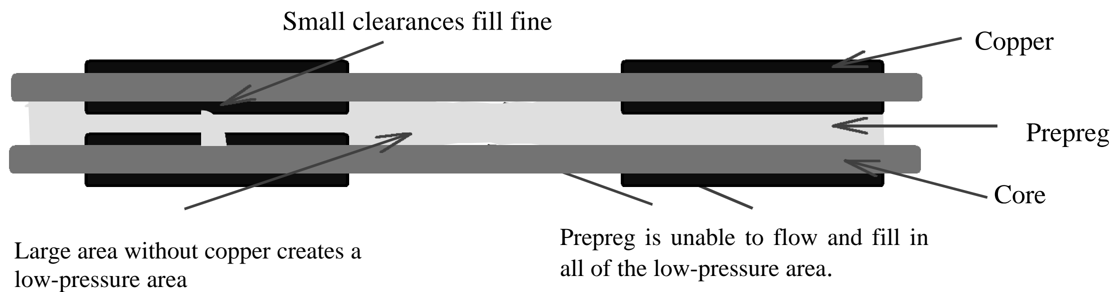


Figure 36 Low-pressure fill example

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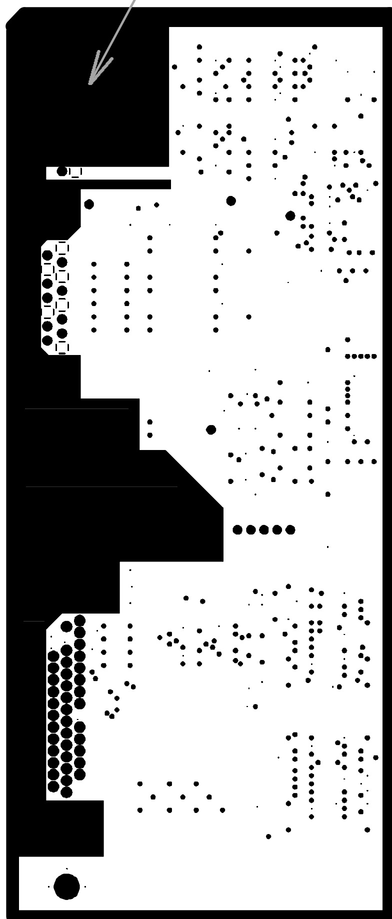
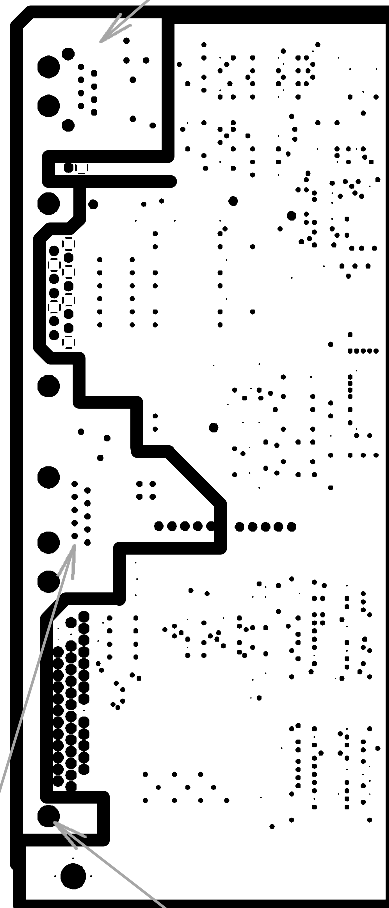
This problem is greatly compounded when the copper weight is 2 or 3 oz, and may require more expensive prepreg to be used, or the use of patches of prepreg placed in these low-pressure areas to make up the difference in thickness. High layer counts, and impedance control may limit or eliminate the available options that HADCO has when dealing with this problem.

This problem can easily be avoided, by placing unused copper inside of these cutouts or open spaces on the plane layers. This added copper would then allow the prepreg to properly fill and will result in a much more reliable cost effective PWB design. In some designs adding copper is the only practical option for preventing delamination in these low-pressure areas, because of the PWB type and build-up.

Large area void of copper creates a low-pressure area during lamination

Non functional copper added to fill low-pressure area





Clearance antipads keep holes from touching unused copper

Avoid

Preferred

Figure 37 Void fill examples

TRACES, PADS & CONDUCTIVE FEATURE DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Inner layers:		
1 oz. Minimum line width / spacing:	0.004" / 0.005"	
1/2 oz. Minimum line width / spacing:	0.004" / 0.005"	0.003" / .004"
Pad diameters:		
0.008" cores or less:		
Tangency:	Add 0.012" to drilled hole diameter	
Annular ring requirements:	Drilled hole + 0.012" + 2 x min A/R	
Inner layers (above 0.008" core):		
Tangency:	Add 0.010" to drilled hole diameter	
Annular ring requirements:	Drilled hole + 0.010" + 2 x min A/R	
Power plane clearance	Drilled hole + 0.024"	
Outer layers:		
½ oz. Minimum line width / spacing:	0.005" / 0.005"	0.003" / 0.003"
Pad Diameters:		
Tangency:	Add 0.010" to drilled hole diameter	
Annular ring requirements:	Drilled hole + 0.010" + 2 x min A/R	
NPTH-to-Copper for primary drill:	0.015"	
Copper feature to hole spacing	0.005"	

GENERAL

- To increase interconnect reliability on the signal layers, HADCO recommends that all pad-to-trace intersections be teardropped whenever the pad diameter minus the plated hole diameter is less than 0.020".

INTERNAL POWER / GROUND LAYER DESIGN GUIDELINES

- Power and ground layers in the Gerber data must have a negative polarity.
- Provide a layer number and description on the artwork.
- Clearance antipads must be a minimum diameter 0.024" larger than the nominal drilled hole size.
- When placing thermal pads:

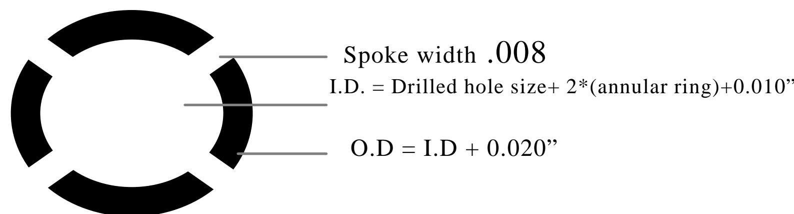


Figure 38 Thermal pad design

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- Size the outside diameter using this formula: OD = ID + 0.020”.
- Rotate each thermal 45° to the plane and add spokes that are 90° apart.
- Spoke width: 0.015” (preferred) or 0.008” (minimum).
- To prevent exposed copper at board edge, keep copper 0.025” away from the PWB perimeter.
- Provide square thieving inside all inner-layer breakaway areas

INTERNAL SIGNAL LAYER DESIGN GUIDELINES

- Standard trace / space: 0.004” / 0.005”.
- Minimum trace-to-trace spacing: 0.004”
- Gerber data for the inner signal layers must have a positive polarity.
- Clearly label layer number and description.
- Minimum barrel of hole-to-copper spacing: 0.010” (see the following figure)
- No feature smaller than a 0.005” square is allowed.
- Relieve all internal copper from route paths by at least 0.05”.
- Provide thieving inside all open and breakaway areas.
- Whenever possible, remove all non-functional pads that have no connected traces on inner layers.
- Use internal signal layers for fine-line and dense circuitry.
- Keep cross-hatching grids greater than 0.010” x 0.010”.
- Provide teardropping for all trace to pad connections.
- Allow trace repairs per IPC-R-700 guidelines.
- Keep same net spacing greater than 0.004”.

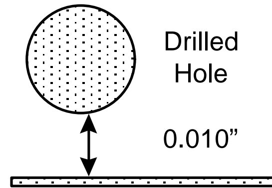

Figure 39 Hole-to-copper spacing

OUTER SIGNAL LAYER DESIGN GUIDELINES

- Standard trace / space: 0.005” / 0.005”.
- Minimum trace / space: 0.003” / 0.003”.
- Outer layer Gerber data must have a positive polarity.
- Clearly label layer number and description on Gerber data.
- Relieve all internal copper from route paths by at least 0.025”.
- Minimum NPTH-to-copper spacing: 0.015” (for tenting at primary drill).
- Minimum distance from tooling hole edge-to-feature edge should be at least one half of the board thickness.
- Minimum space between gold edge connector and breakaway tab: 0.250”.
- Traces should be ≥ 0.040” away from the score line center on all outer layers.
- Use a different size pad for every hole size and test point.
- Keep all pad edges at least 0.050” above edge fingers.
- Keep the most complex circuitry off the outer layers.
- Rout critical lines on the inner layers.
- On the solder-side, leave a 0.200” x 0.400” area for HADCO to add a date code box, ID, and UL logo.

- Isolated fiducials with a diameter ≤ 0.050” should have a 0.015” copper diameter ring of copper around the fiducial, covered by soldermask. This protects the pad during HASL application.
- Layout of circuitry on the board has a major influence on the way the panel actually plates. Try to avoid unbalanced designs on the outer layers. Solitary traces will over plate. Isolated holes will over plate and may yield finished hole sizes that are under specifications.
- To maximize plating distribution, allow HADCO to add square thieving to low density areas on the outer layers (such as breakaways or substantial unused spaces within the PWB). Square thieving consists of 0.030” copper squares centered on a 0.050” grid and spaced 0.020” from all board features. Per request, thieving will be removed from the inside of SMD arrays.
- Allow trace repairs per IPC guidelines.
- Gold edge fingers should be greater than 0.009” wide to minimize lifting during PWB edge routing.
- Recessed edge fingers should be connected for plating using internal bussing.
- For boards with edge connectors, there must be at least 0.035” of soldermask between the soldermask clearance of the nearest via hole and the top of the edge connector area. If this spacing is violated, mask will be extended onto the edge connector until 0.035” is achieved. The board designer should extend the soldermask over the finger.

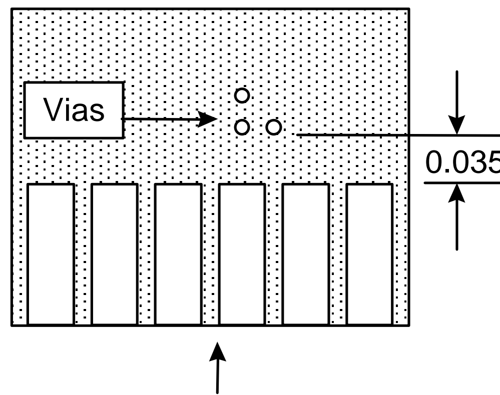

Figure 40 Via-to-gold edge connector spacing

DRILLED HOLES & SLOTS

DRILLED HOLES & SLOTS TUTORIAL

This section discusses mechanical drilled holes. Other hole creation technologies are discussed in the Technology section. There are three finished hole configurations; non-plated (NPTH), plated (PTH) and optionally plated (OPTH).

Non-plated Through Holes

Non-plated through holes are drilled through the board and do not have any plating on the hole walls. The drilled hole diameter and tolerance is the same as the finished hole specifications.

Drilled hole diameter = Nominal finished hole diameter

EXAMPLE:

The design requires an unbalanced tolerance hole which is 0.038" +0.005"/-0.001" finished non-plated through hole.
What will the drilled hole size be?

Drilled hole diameter = 0.038" + (+0.005" – 0.001")/2
= 0.040"

Plated Through Holes

Plated through holes are drilled through the board and will have copper plating covering the internal hole surfaces. There may also be an additional surface finish coating the copper surface, such as solder (HASL). The finished hole diameter will be drilled larger than the finished hole diameter. The larger diameter will include the copper and surface finish thickness included. The finished hole tolerance will be utilized to select the drilled hole size diameter to ensure that the final tolerance is met. Only PTH's that will have a component inserted into them should have a finished tolerance. Via holes, or holes that are utilized to connect signals on multiple layers should be allowed to be completely closed shut if they are less than 20 mils in diameter.

Drilled hole diameter = Nominal finished hole diameter + manufacturing tolerance + surface finish tolerance

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EXAMPLE:

The design requires a 0.038” +0.003/-0.003” finished plated through hole with a HASL finish.
What will the drilled hole size be?

Drilled hole diameter = 0.038” + 0.005” + 0.002”
= 0.045”

EXAMPLE:

The design requires a 0.038” +0.003/-0.003” finished plated through hole with an OSP finish.
What will the drilled hole size be?

Drilled hole diameter = 0.038” + 0.005” + 0.000”
= 0.043”

Optionally Plated Through Holes

Optionally plated holes should be specified when a non-plated or plated hole can be used. This allows the fabricator to drill the hole in the least expensive manner.

General Guidelines

Drilled holes are a substantial percentage of the fabrication cost. The cost can be kept low by removing all unnecessary holes and removing all internal pads that do not connect to a trace (non-functional pads). One of the predominate factors that reduce the quantity of holes drilled per drill bit is the amount of copper that it must drill through. There is a significant amount of reliability data that has been performed over the last 30 years that demonstrate the removal of non-functional pads will not detrimentally affect the plated through hole reliability.

Aspect Ratio

The second major factor that affects cost is the number of boards that are drilled at the same time. HADCO tries to simultaneously drill at least three boards with every bit. This lowers the hole drilling cost. The holes should be made as large as possible to allow the highest possible stack height. Try to keep a low board thickness: hole diameter ratio (aspect ratio) as possible. 5:1 to 7:1 aspect ratios are cost effective. Greater than a 7:1 ratio will impact the drilled hole cost.

Hole to Hole Spacing

Drilled holes must be spaced with sufficient distance so they won’t break out into the side of a previously drilled hole.

Routed Versus Drilled Holes

Holes that are greater than 0.250” will be routed versus drilled. These holes will require a larger finished diameter tolerance. The center-to-center hole distance should be kept at least (finished hole diameter + 0.030”) apart from each other to minimize the propensity to break-out into each other.

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DRILLED HOLES & SLOTS DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Holes:		
Minimum drilled hole diameter:	0.012”	0.010”
Maximum drilled hole diameter:	0.250”	
Maximum Aspect ratio:	8:1	10:1
Plated hole diameter tolerance:	+/- 0.003”	+/- 0.002” (after OSP/ NiAu)
Drilled hole diameter tolerance (NPT):	+/- 0.0015”	+/- 0.001”
Hole-to-hole location accuracy:	+/- 0.003” (0.00849” DTP)	

GENERAL

- Whenever possible, combine hole diameters that are within 0.002” of each other.
- Clearly, indicate on the blueprint if any holes or slots can be optionally plated.
- Vias that have more than 4 interconnections of one-ounce copper should have a separate drill code. Different drill bits may be utilized due to higher drill breakage that is due to the additional copper.
- Maximum drilled hole aspect ratio (board thickness/drilled hole diameter): 8:1

NON-PLATED THROUGH HOLES

- Minimum drilled hole diameter tolerance: +/- 0.0015”. This assumes that the nominal hole size matches a standard drill diameter.
- Tooling holes should be ≤ 0.250”. The preferred size is 0.125”.
- Non-plated holes with a diameter greater than 0.250” may be produced during the profile routing sequence (Size tolerance = +/- 0.005” and Position tolerance = +/- 0.005”).
- Holes with a diameter > 0.250” that require a size tolerance less than +/- 0.005” will be drilled at +/- 0.003” using a circle option (drill pecking).
- Non-plated holes and slots will be second drilled whenever the required 0.010” minimum feature clearance cannot be maintained.

PLATED THROUGH HOLES

- Standard diameter tolerance: +/- 0.003”.
- Minimum diameter tolerance: + 0.003” / -0.002”.
- Minimum backplane hole diameter tolerance (after copper plating): +/- 0.002”.
- Minimum hole edge-to-hole edge spacing: 0.015”.
- Minimum hole-to-copper spacing: 0.010” (inner & outer layers).
- The tolerance for any via ≤ 0.018” in diameter will be + 0.003” / - nominal hole size.
- Minimum drill diameter for vias passing through EMI shielding (copper all layers): 0.018”.
- Small via holes which are specified at less than 0.018” in diameter should have a tolerance of +.003/-.diameter. (e.g., 0.013” +.003/-.013”)
- Holes will be drilled at least 0.005” larger than the nominal finished hole diameter (before adjusting for the surface finish).
- Holes which are drilled directly into plane layers (i.e. EMI shields) without thermal relief pads should provide a center clearance which is half of the drilled hole size diameter to improve the drill quality.
- Padless holes should have a pad on the outer layers to reduce outer layer imaging problems.
- The minimum average plated thickness for a plated through hole should be specified as 0.001”.

- The absolute minimum plating thickness for a drilled plated through hole should be specified as 0.0008”.

NON-PLATED THROUGH SLOTS

- Non-plated slots with a tolerance < 0.0049” and ≥ 0.002” will be drilled.
- Tolerances ≥ 0.005” will be routed. Length, width, and position tolerances maintain 0.005”.
- The slot length should be a minimum of twice the slot width + 0.001”.

PLATED SLOTS

- Minimum size tolerance (length & width): +/- 0.005”.
- Minimum position tolerance: +/- 0.005”.
- The slot length should be a minimum of twice the slot width + 0.001”.

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STANDARD DRILL SIZES

Size	Equivalent (mm)	Equivalent (in)	Size	Equivalent (mm)	Equivalent (in)	Size	Equivalent (mm)	Equivalent (in)
#91		.0083	1.80mm	1.80	.0709	#21		.1590
#87		.0100	#49		.0730	#20		.1610
#83		.0120	1.90mm	1.90	.0748	4.15mm	4.15	.1634
#82		.0125	#48		.0760	4.20mm	4.20	.1654
#80		.0135	1.95mm	1.95	.0768	#19		.1660
#79		.0145	5/64”		.0781	4.25mm	4.25	.1673
1/64”		.0156	#47		.0785	#18		.1695
#78		.0160	#46		.0810	11/64”		.1719
#77		.0180	#45		.0820	#17		.1730
#76		.0200	2.15mm	2.15	.0846	4.45mm	4.45	.1752
#75		.0210	#44		.0860	#16		.1770
#74		.0225	2.20mm	2.20	.0866	#15		.1800
#73		.0240	#43		.0890	#14		.1820
#72		.0250	2.30mm	2.30	.0906	#13		.1850
#71		.0260	2.35mm	2.35	.0925	4.75mm	4.75	.1870
0.70mm	0.70	.0276	#42		.0935	3/16”		.1875
#70		.0280	2.40mm	2.40	.0945	#12		.1890
#69		.0292	#41		.0960	#11		.1910
0.75mm	0.75	.0295	#40		.0980	#10		.1935
#68		.0310	#39		.0995	#9		.1960
0.80mm	0.80	.0315	2.55mm	2.55	.1004	5.0mm	5.00	.1969
#67		.0320	#38		.1015	#8		.1990
#66		.0330	#37		.1040	5.10mm	5.10	.2008
0.85mm	0.85	.0335	#36		.1065	#7		.2010
#65		.0350	2.75mm	2.75	.1083	13/64”		.2031
#64		.0360	7/64”		.1094	#6		.2040
#63		.0370	#35		.1100	#5		.2055
#62		.0380	#34		.1110	#4		.2090
#61		.0.390	#33		.1130	#3		.2130
#60		.0400	2.90mm	2.90	.1142	5.45mm	5.45	.2146
#59		.0410	#32		.1160	5.50mm	5.50	.2165
#58		.0420	3.00mm	3.00	.1181	5.55mm	5.55	.2185
#57		.0430	#31		.1200	5.60mm	5.60	.2205
1.12mm	1.12	.0440	3.10mm	3.10	.1220	#2		.2210
1.15mm	1.15	.0453	3.15mm	3.15	.1240	5.70mm	5.70	.2244
#56		.0465	1/8”		.1250	#1		.2280
3/64”		.0469	3.20mm	3.20	.1260	A		.2340
1.20mm	1.20	.0472	3.25mm	3.25	.1280	6.00mm	6.00	.2362
1.25mm	1.25	.0492	#30		.1285	B		.2380
1.27mm	1.27	.0500	3.30mm	3.3.0	.1299	6.10mm	6.10	.2402
1.30mm	1.30	.0512	3.35mm	3.35	.1319	6.20mm	6.20	.2441
#55		.0520	3.40mm	3.40	.1339	6.25mm	6.25	.2461
1.35mm	1.35	.0531	#29		.1360	6.30mm	6.30	.2480
#54		.0550	3.50mm	3.50	.1378	0.25”		.2500
1.45mm	1.45	.0571	#28		.1405	6.40mm	6.40	.2520
1.50mm	1.50	.0591	3.60mm	3.60	.1417	F		.2570
#53		.0595	#27		.1440	6.80mm	6.80	.2677
1.55mm	1.55	.0610	3.70mm	3.70	.1457			
1/16”		.0625	#26		.1470			
1.60mm	1.60	.0630	#25		.1495			
#52		.0635	#24		.1520			
1.65mm	1.65	.0650	#23		.1540			
#51		.0670	5/32”		.1562			
1.75mm	1.75	.0689	#22		.1570			
#50		.0700	4.00mm	4.00	.1575			

Table 8 Standard drill size

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SOLDERMASK

SOLDERMASK TUTORIAL

Soldermask is a protective coating that shields selected areas of a PWB from oxidation, handling, and unwanted solder during assembly. Soldermask is applied in two separate operations called primary and via plug. Primary soldermask (LPI) is applied to cover traces and planes so adjacent features won't short during assembly. Via holes are not covered during this operation.

Via plug is a secondary screen print operation which coats soldermask material into one side of the via. This is generally required when a vacuum assisted In-circuit test is utilized after assembly.

- The master drawing should only specify that a LPI soldermask is required with a compatible via plug option. Do not specify the actual supplier material. This may limit the available manufacturing sites.
- Finish: It is available with a matte or semi-gloss finish.
- Color: It is available in green or clear.
- The soldermask opening should be created in the CAD design at least 0.006" larger than the pad size. The soldermask clearance should be one half of the pad to trace spacing for clearances less than 0.006". The minimum soldermask to pad clearance should be two mils on each side (0.004" overall).

Webbing

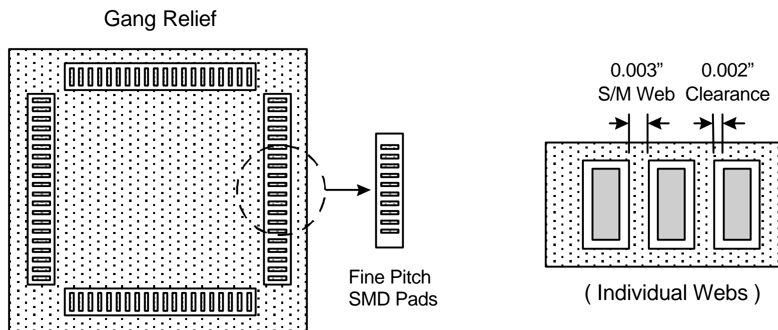

Figure 41 Soldermask SMD clearances

Soldermask is commonly placed between surface mount pads to reduce solder bridging during assembly. These small lines of mask between the pads are called webs. Soldermask webs have a minimum width that can be reliably exposed such that they will remain on the board during assembly. The space between the pads must allow for registration tolerances for imaging the soldermask. This leaves a small "finger" of soldermask web between the SMT pads. The web must be removed when the web width falls below the manufacturing capability. This is called gang relief. Please specify if gang relief is allowed, or not allowed, on the fabrication print.

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Soldermask on the top of gold edge fingers

It is preferred to have the solder mask brought down to the top of the fingers, and not to have it stop above the fingers. Stopping above the tops of the fingers will result in circuits exposed from the edge of the solder mask to the fingers. Damage to the exposed circuits may result during gold tipping.

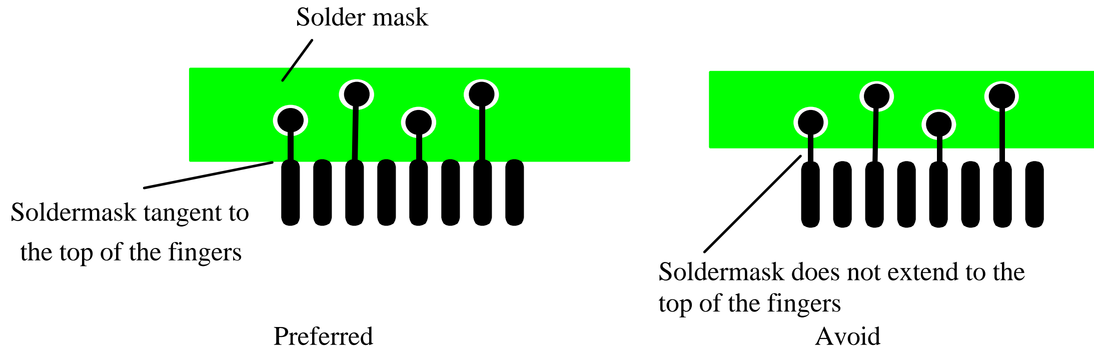

Figure 42 Soldermask coverage on gold fingers

Soldermask at the bottom of gold edge fingers

Solder mask clearances at the fingers should extend past the bevel and the board edge. This will prevent having soldermask between the end of the bevel and the fingers. This will flake off during manufacturing.

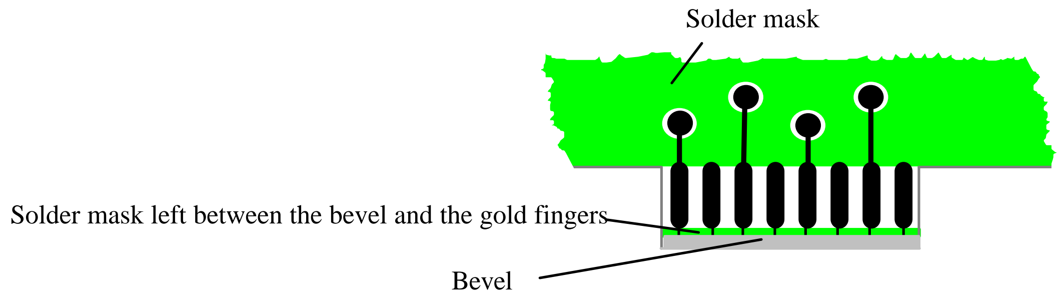

Figure 43 Soldermask coverage on gold fingers

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Via Plugging

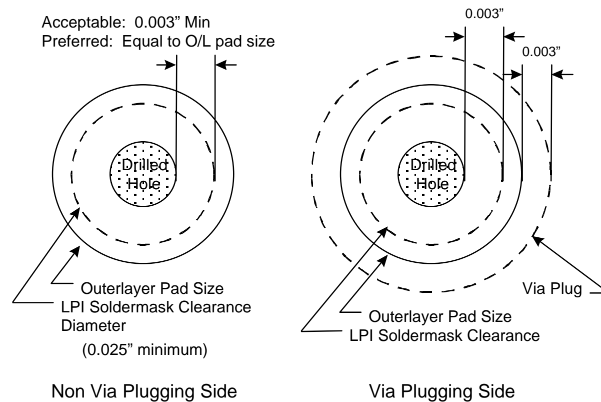

Figure 44 Via plugging

The standard LPI soldermask process cannot tent or fill vias. A secondary screen print operation deposits UV curable or epoxy soldermask into the holes to plug them. This is called via plugging. Via plugging is used to fill (plug) open holes with a soldermask to block air leakage during In Circuit Test (ICT). Only one side of the via can be plugged. There is a high probability that one side of the plug will be blown off during assembly if both sides of the same via are plugged. HADCO prefer to plug the solder side of the board. The soldermask opening must be made larger than the hole to allow for reliable via plug deposition into the hole.

SOLDERMASK DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
LPI Soldermask:		
Average thickness over trace:	0.0005”	
Registration tolerance:	+/- 0.003”	+/- 0.002”
Spacing (for mask between pads):	0.009”	0.007”
Available colors:	Green	

- Green is the preferred soldermask color.
- Green soldermask allows a 0.004” web to be placed between pads in an SMD array, provided the minimum spacing between these pads is 0.009” (by design).
- To assure no soldermask on any pad in an SMD array, the minimum soldermask clearance for a surface mount pad is 0.003” per side. As space permits, a clearance of 0.0025” per side is available.
- Mask features below 0.004” are not allowed (as measured on the CAD data).
- Allow 0.010” per-side soldermask clearance from the edge of the score line.
- To prevent soldermask from going into and/or plugging a hole, soldermask clearance should be 0.006” (0.003” per side) larger than the pad size on both sides of the board.
- Plugging vias with LPI soldermask is not an option.
- The maximum height for the via plug mask should be 0.0025”.
- Soldermask should not be left between edge plated fingers.
- Via plug holes should be less than 0.015” finished diameter.

LEGEND

LEGEND TUTORIAL

Legend (silkscreen) provides graphical component outlines or alphanumeric characters to designate component locations. It is applied using a standard screen-print process.

Legend should not be used on high-density designs. Generally, a non-readable character remains when minimum character sizes are used and then modified to remove legend from all conductive surfaces. Components are located by using assembly drawings or trouble-shooting documentation.

LEGEND DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Legend:		
Colors:	White, Yellow	Orange, black
Smallest line width:	0.008”	
Location accuracy:	+/- 0.008”	
Minimum character height:	0.050”	0.040”

- To ensure all letters, numbers, and figures are legible on the finished board, character line widths should be greater than 0.008” and at least 0.050” high.
- Space letters at least 0.008” apart so they don’t bleed together.
- No legend nomenclature should overlap a copper pad or plane area. This is especially important for surface mount pads and fiducials.
- White and yellow are standard legend ink colors.
- Use the fabrication print notes to specify special features to be screened onto the board.

MECHANICAL FEATURES

MECHANICAL FEATURES TUTORIAL

Routing

The routing operation removes the PWB from the production panel. Routing is also used to create cut-outs and slots in the PWB interior. The key design consideration is providing sufficient clearance between the edge of the rout and PWB traces and holes. The largest router bit should be used to minimize the routing cost by allowing multiple panels to be simultaneously routed.

Breakaway rails

Assembly breakaway rails should be included with the board design. This will ensure that all fabricators will provide the same size. HADCO should be allowed to incorporate production targets, holes and thieving in the breakaway area. This will allow us to maximize the panel utilization by letting the breakaway fall into the panel unusable area.

Beveling

Beveling is performed to add a smoother sliding surface for edges of the PWB that are required to slide into a mating connector. Bevels can be provided for inset surfaces with some restrictions. The angle and depths are generally established by the connector pin style.

Scoring

Scoring cuts a small vee notch into the bottom and top surfaces of the board. This allows the board to be “snapped” apart from other boards after assembly. This is an alternative to using breakaway rails. It provides the minimum board-to-board spacing of all these options. The assembler can provide component and trace to score edge distances that are required for their processes.

Edge milling

Edge milling is performed for boards that are too thick to slide into the card guides. For example, a PWB is required to increase the thickness from 0.062” to 0.093” to provide sufficient routing layers or to create the required impedance. The two sides of the board can be edge milled to allow the 0.093” board to slide into the 0.062” card guide.

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MECHANICAL FEATURES DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Routing:		
Edge-to-edge tolerance:	+/- 0.010"	+/- 0.003"
Edge-to-datum hole tolerance:	+/- 0.005"	+/- 0.003"
Minimum internal radius:	0.047"	0.031"
Minimum external radius:	None	None
Max. routed hole diameter and tol.:	1.250" +/- 0.010"	1.250" +/- 0.005"
Min. routed hole diameter and tol.:	0.250" +/- 0.005"	0.250" +/- 0.003"
Preferred router bits:	0.093"	0.047",0.062"
Scoring:		
Minimum web thickness:	0.012"	
Available scoring angles:	30°	45°, 60°
Web thickness tolerance:	+/- 0.003"	+/- 0.002"
Location tolerance:	+/- 0.005"	
Jump score capability:	Yes	
Edge beveling:		
Available angles:	30°	20° & 45°
Angle tolerance:	+/- 5°	
Available depths:	0.015" to 0.075"	
Depth tolerance:	+/- 0.010"	

ROUTING

- Minimum drilled datum-to-routed edge tolerance: +/- 0.005".
- Minimum routed edge-to-routed edge tolerance: +/- 0.010".
- NC Routed slots:
    - Minimum length & width tolerance: +/- 0.005".
    - Minimum position tolerance: +/- 0.005".
- Slots must show a radius at the top and the bottom.
- The preferred router bit diameter is 0.093".
- Breakaway tab attachments should be spaced apart between 1.00" and 2.50".
- Minimum tolerance of internally routed features: +/- 0.005".
- Provide at least 2 non-plated, diagonally placed tooling holes for pinning during profile routing. Three holes are prefered.
- Minimum distance from tooling hole edge-to-feature edge: 0.015".
- Relieve all internal copper from the route path by ≥ 0.025".

BREAKAWAY RAILS

- Breakaway rails should be included in the PWB design.
- Tab spacing should provide sufficient strength so it won't break off during normal handling. The following figure presents a typical design.
- Breakaway holes should be designed so they won't break during PWB fabrication and will easily break after assembly. The following figure presents a typical design.

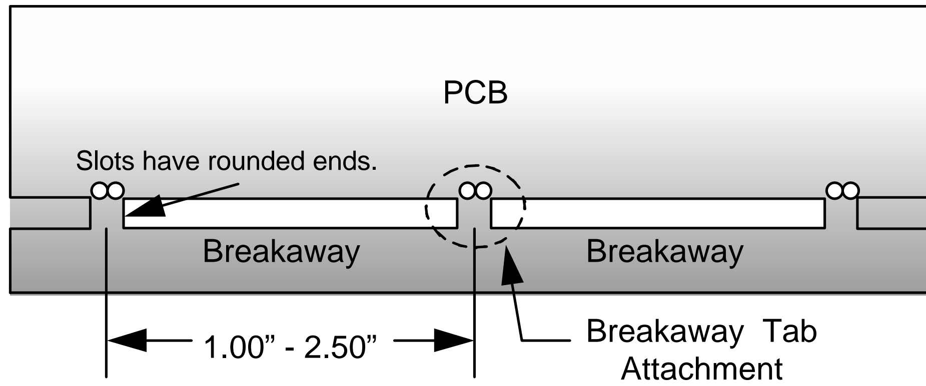

Figure 45 Breakaway tab spacing

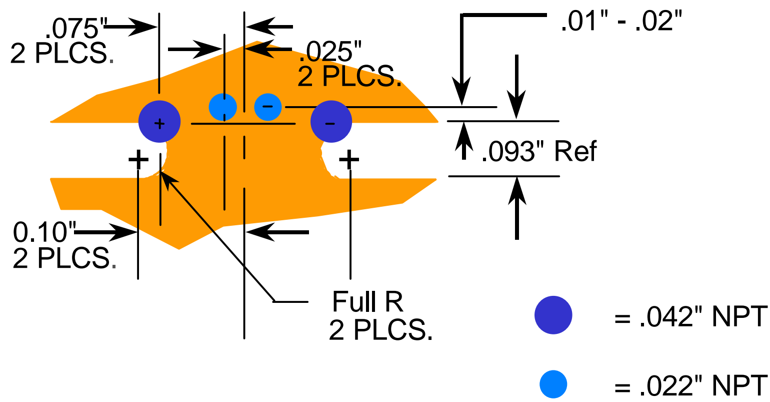

Figure 46 Breakaway tab detail

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BEVELING

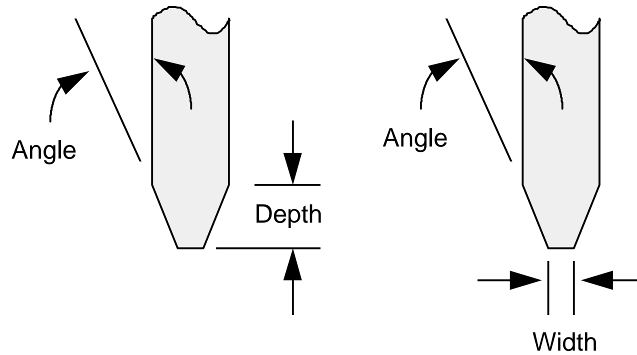

Figure 47 Bevel diagram

- Maximum length of a beveled edge: 18”.
- Minimum beveled edge-to-opposite edge of the PWB dimension: 2.5”.
- Minimum / maximum bevel depth: 0.015” / 0.075”.
- Bevel angles available: 20, 30, & 45 degrees +/- 5 degrees.
- Maximum recessed bevel: 1.25”.
- Minimum space between gold edge connector and breakaway tab: 0.250”.
- Do not partially edge chamfer the finger side of the board when the fingers are flush with the edge of the board.

SCORING

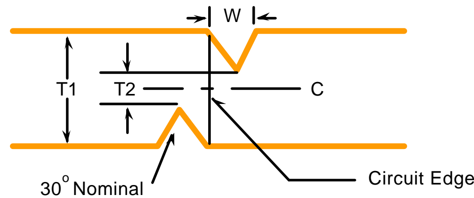

Figure 48 Scoring diagram

- Minimum / maximum panel thickness (T1): 0.020” / 0.125”.
- Maximum score distance: 25”.
- Minimum web thickness tolerance: +/- 0.005”.
- Score angle: 30 +/- 2 degrees.
- Minimum web thickness (T2 in the above figure): 0.012”.
- Traces should be ≥ 0.050” away from the score line center on all outer and inner layers.
- Score line width should be 1.15 times the depth.
- Minimum scoring should be orthogonal.
- One score test coupon per score line should be included (see the following figure). In the netlist, these score coupons will be designed as opens.
- No board to board spacing is required.

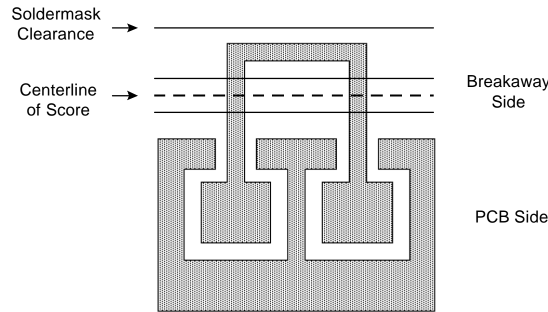

Figure 49 Score coupon

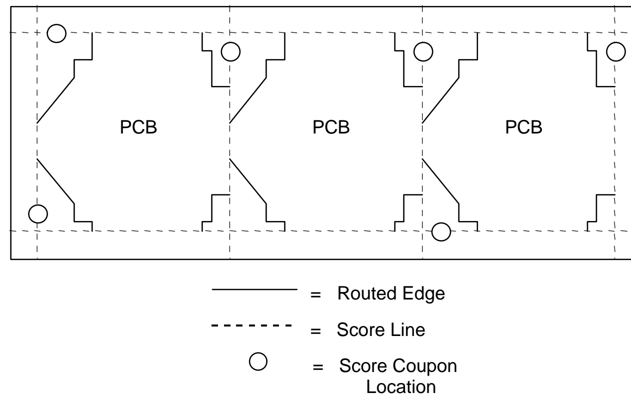

Figure 50 Score coupon locations

EDGE MILLING

- Edge milling is used to reduce the thickness on the edge of a PWB that is too thick to slide into a card guide.
- A finished board thickness tolerance of +/- 0.006" minimum can be achieved.
- The fabrication drawing must specify which side of the board that the material must be removed from.
- Only edge mill one side of the board on the same edge.
- All metal must be removed from the area that is to be milled.

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SURFACE FINISHES

SURFACE FINISHES TUTORIAL

A surface finish provides a coating over the outer layer copper that prevents oxidation and provides an electrically conductive surface. This surface has two generic functional requirements. The first is to provide a solderable surface for connecting components with solder. The second function is to attach a component without soldering, such as a wire bond or press-fit connector.

Solderable Finishes

HASL (Hot Air Solder Leveling): A thin solder coating is deposited onto all exposed copper pads. It is the most prevalent and most solderable coating. It increases fabrication rework for boards that have fine pitch SMT devices with lead centers below 0.020”. Boards that have been HASL leveled will have bright silvery pad coloration. This is also termed HAL (Hot Air Leveled)

Solder thickness and uniformity on SMD pads is a function of pad size, pad orientation during processing, and HASL equipment. As pad size increases, thickness and uniformity decrease. This is caused by the high surface tension of solder and the airflow over pads that removes excess solder. Small pads (0.025” pitch SMD) will have more uniform solder coating than large pads (0.050” x 0.050”). Large pads may be partially covered with a mound of solder while the rest is thin eutectic solder. Small pads may have the same condition depending on pad orientation during processing.

Pad orientation also contributes to solder thickness and uniformity. Fine pitch SMD pads perpendicular to the direction of processing will have a more uniform solder coating covering the entire pad. Fine pitch SMD pads that are parallel to the direction of processing will have the leading half reduced down to the thin eutectic solder with a mound of solder on the trailing half. Angled processing exposes both pad directions to similar air blasts resulting in more consistent pad thickness for similar pad sizes. 45-degree angle processing minimizes the pad orientation difference.

OSP (commonly called ENTEK®): This process coats a very thin coating of an organic material that inhibits copper oxidation. It is so thin that it is nearly impossible to see and measure. The organic material is removed by the assembly flux. Boards that have been OSP coated will have bright copper pad coloration.

Immersion Gold*:* This process plates a thin coat of nickel covered by a thin layer of pure gold. The gold provides a very good solderable surface. When components are soldered onto these pads the gold diffuses into the solder joint. This process is generally not utilized for high reliability, long lifetime, or high vibration applications.

Mechanical Mounting Surfaces

HASL (Hot Air Solder Leveling): This is the most common surface finish. It is also used for connections which have a gas tight compression fit contact which is prevalent in press-fit backplane applications.

Edge Plated Fingers (commonly called Tips): A nickel coating is deposited on bare copper with a hard gold surface finish electrolytically deposited on it. This is applied in a horizontal line and can only be used

near the edge of a board. This is a relatively in-expensive fabrication process. This is the preferred method for creating edge card fingers.

Selective Electroplated Gold: This process applies a nickel coating onto the bare copper and coats it with a electroplated gold surface. It differs because the entire board must have additional fabrication steps which remove the primary surface finish, such as HASL, in order to apply the gold only to the required locations. This is a relatively expensive process.

Selective non bussed areas can be plated with nickel and gold before etching, by the use of a gold mask. These gold masks should be supplied in the data package. Simple gold masks can be created at HADCO if detailed information is supplied as to what features will be plated.

- Non gold plated circuits and pads should not be within 0.020" of the features that require selective gold plate.
- The gold mask should be designed so that the mask is a 0.010" larger than the features that will be gold plated.
- If via holes, or other plated holes fall into the area that is to be gold plated, then both sides of the gold mask should have these included in the gold mask. Tenting a hole on one side, and gold plating the pad and hole on the other will not work with the process. The results will be voided holes that should be plated.

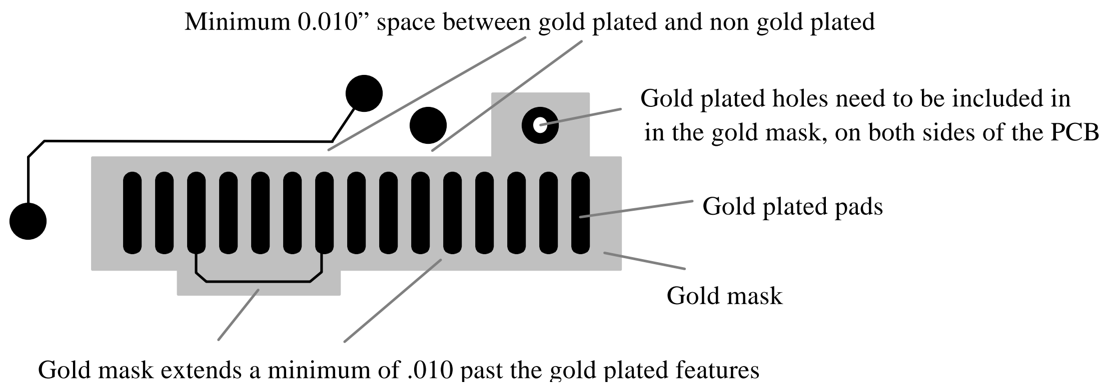

Figure 51 Selective gold design rules

Selective Solder Strip: This process is typically used when the surface mount pitch is less than 0.015", and the use of the standard solder paste deposition process at assembly is not an option. Tin lead is electroplated onto the board features. It is then selectively removed (typically from traces) by using multiple imaging operations. This process is much more expressive than HASL due to the additional processing steps. Current solder thickness capabilities using the selective solder strip process are, maximum of 0.0015" and minimum of 0.0003".

Via in pads

Vias should not be drilled through any surface mount pads. Plated holes in surface mount pads tend to wick up the extra solder from the surface mount pads, causing poor solder joints at assembly. If vias are near surface mount pads and both pads are free of solder mask maintain a 0.025" space between via pads and the surface mount pads. This will prevent the solder from wicking into the via hole at during solder reflow.
HADCO can not ensure that surface mount pads that have via pads within 0.020" of the surface mount pads will have the required solder thickness.

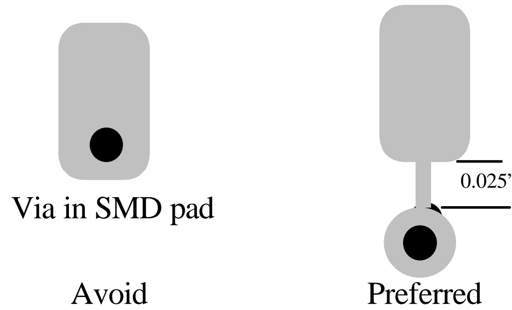

Figure 52 Via to pad spacing

Wire Bondable Surfaces

Selective Electroplated Gold (commonly called soft gold): This process applies a nickel coating onto the bare copper and coats it with a electroplated soft gold surface. It differs because the entire board must have additional fabrication steps that remove the primary surface finish in order to apply the gold only to the required locations. This is a relatively expensive process.

SURFACE FINISHES DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Hot Air Solder Level thickness:	50 - 1500 µ in	
OSP	Solderable	
Electroless Ni / Immersion Au	100 µ in Ni / 2-8 µ in Au	
Edge plated fingers	100 – 150 µ in Ni / 20 - 50 µ in Au	100 – 300 µ in Ni / 20 - 50 µ in Au
Fused Tin Lead		0.0003” min (as plated)

ORGANIC SOLDERABILITY PRESERVATIVE (OSP)

- OSP is a replacement for other solderable surfaces including Hot Air Solder Leveling (HASL), reflowed SnPb, and Ni/Au.
- HADCO prefers this surface finish over HASL.
- PWB thickness range: 0.020” through 0.250”.
- HADCO offers two basic types of OSP finishes:

Benzotriazole:	~50 Angstroms thick. It is a self limiting process. Can detect its presence (not thickness). This offers only 1 thermal cycle of protection at assembly
Benzimidizole:	0.2 to 0.5 microns thick. Can measure thickness by processing a standard thickness coupon. This offers multiple thermal cycles of protection at assembly.

ELECTROLESS NICKEL / IMMERSION GOLD

- Minimum nickel thickness: 100 µ in
- Gold thickness range: 2 µ in - 8 µ in.

HOT AIR SOLDER LEVELING (HASL)

- Solder thickness range: 50 - 1500 µ in.
- Special option solder thickness tolerance: 100 - 1000 µ in (measured at the center of the pad).
- Solder thickness at the knee of a plated through hole is approximately 10 - 25 µ in.
- Thickness measurements are taken at the pad's centroid.
- As pad size decreases, solder thickness per unit area increases.
- The solder thickness distribution of the PWB is determined by the solder thickness requirements of the smallest features.

ELECTROPLATE "TIP PLATING EDGE CONNECTORS"

- Minimum / nickel thickness: 100 µ in.
- Minimum / Maximum gold thickness: 20 µ in.
- Maximum nickel-gold finger length / connector span: 0.750" / 23.25"
- Minimum part processing height: 5.5"

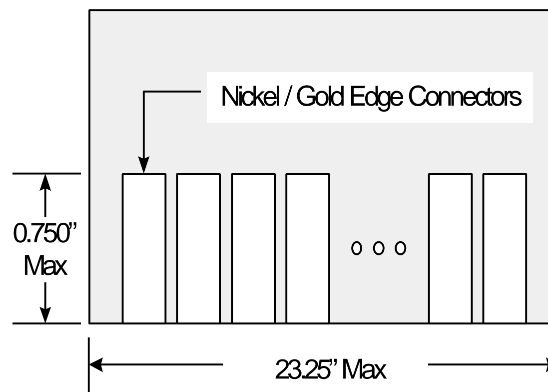

Figure 53 Gold edge connectors - Height & width dimensions

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CONTROLLED IMPEDANCE

CONTROLLED IMPEDANCE TUTORIAL

Controlled impedance PWB's require specific constructions and tighter manufacturing controls. HADCO has tailored standard impedance equations to precisely calculate PWB constructions. This equation is available on the HADCO web site (www.hadco.com). A +/- 10% impedance tolerance can be manufactured without requiring 100% product testing. AQL tests or controlled geometry techniques should be specified or allowed.

A 10% or greater impedance tolerance can be manufactured without any additional conformance tests or coupons. Nominal impedance values below 50 ohms may require higher tolerances.

The fabrication drawing should not specify the exact layer-to-layer spacing for impedance layers. It should specify the required nominal impedance and tolerance. HADCO can create the PWB construction and send it to you for your approval.

Primary Impedance Factors

PWB fabrication processes affect the trace nominal impedance and tolerance. The key factors are:

- Trace width
- Trace thickness (affected by base copper and copper plating thickness')
- Dielectric thickness
- Overall PWB thickness
- Relative permittivity (Dielectric constant)

HADCO uses proprietary impedance modeling software, to determine the specific PWB construction required to produce the specified impedance. It is important to not specify the material glass styles, thickness and tolerance. The PWB drawing should only specify the nominal impedance, tolerance and nominal line width. This will allow HADCO to create the most cost effective PWB material construction.

Multiple Impedance's

Some boards require multiple impedance values on the same signal layer. HADCO is able to modify impedance coupons to accommodate such a request. The coupon will either be wider than normal (one trace for each impedance) or have one trace of varying widths. However, testing multiple impedance values on a given signal layer is not recommended. Whenever possible, designate one target impedance value per layer. This will validate manufacturing tolerances.

Two types of impedance classifications are generally specified; Single-ended and Differential.

Single-ended Impedance

Single-ended impedance is the impedance established by the interaction of a single trace and it's reference plane(s). There are three basic impedance classifications:

- **Microstrip**: This is a trace on an outer layer with a single reference plane below it.
- **Embedded Microstrip**: This is a microstrip line that has a dielectric over the top of it. Soldermask will change a microstrip into an embedded microstrip line.
- **Stripline**: This is a trace on an internal layer that has a reference plane on above and below it.

- **Dual Stripline or Offset Stripline**: This is a stripline, which is offset between the two reference planes. It generally is used when two adjacent signal layers are routed orthogonally and have reference planes outside of them.

Differential Impedance:

Differential impedance is the impedance established by the interaction of a two traces and their reference plane(s), if required. There are three basic impedance classifications:

- **Edge Coupled Microstrip**: This is two adjacent traces on an outer layer with a single reference plane below it.
- **Edge Coupled Embedded Microstrip**: This is an edge coupled microstrip line that has a dielectric over the top of it. Soldermask will change a microstrip into an embedded microstrip line.
- **Edge Coupled Stripline**: This is two adjacent traces on an internal layer, which is centered between a reference plane above and below it.
- **Edge Coupled Dual Stripline or Offset Stripline**: This is an edge-coupled stripline, which is offset between the two reference planes. It is generally used when two adjacent signal layers are routed orthogonally and have reference planes outside of them.
- **Broadside Coupled Stripline**: This configuration has the two differential lines on adjacent layers directly one above the other. These are offset striplines centered between their two reference planes.

The following guidelines should be used for designing and specifying differential striplines:

- No special fabrication requirements are required for differential transmission lines.
- A higher tolerance will be required when the differential lines are on adjacent layers that are separated by prepreg.
- Broadside coupled striplines should only be used on a core. They should not have prepreg between them. This is required to control the z-axis alignment between the two signal layers.
- Specify the design trace to trace spacing for correct impedance modeling.
- HADCO should be involved in the pre-layout phase to assist with the line width and spacing calculations.
- Give the differential pairs a different aperture than non-differential traces. This will make it easier for HADCO to adjust line widths during the tooling process.

Minimizing Impedance Costs:

Using the following guidelines will reduce the cost impact when specifying controlled impedance PWB’s:

- Only specify the impedance on the layers where it is actually required.
- Route all of the controlled impedance traces onto the same layers.
- Specify a +/- 15% tolerance when possible.
- Do not specify all of the physical dimensions for the trace. Just specify the required impedance and allow HADCO determine the physical parameters. Try to just specify the trace width and tolerance based on the PWB routing.
- Do not require impedance test coupons. This may reduce the panel utilization and will require each PWB to be manually tested.
- Allow panel level testing, without individual PWB serialization, to verify the PWB impedance. Panel testing has been shown to provide sufficient results comparable to individual PWB testing.

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CONTROLLED IMPEDANCE DESIGN GUIDELINES

KEY REQUIREMENTS

- When the tolerance is ≥ 10%, controlled geometry is recommended to assure product conformance.

CONTROLLED IMPEDANCE MATRIX

The following tables present impedance values for various trace widths using the cost-effective constructions that are provided in figures 8 through 14. Other impedance nominal values can be provided using custom layer constructions. Please contact HADCO for PWB construction assistance.

STANDARD CONSTRUCTIONS		LAYERS	NOMINAL TRACE WIDTH (inches)						
LYRS	LOCATION		0.005	0.0055	0.006	0.0065	0.007	0.0075	0.008
4	Figure 8	1, 4	96.3	94.0	91.8	89.8	87.9	86.0	84.3
6	Figure 9	1, 6	70.7	68.3	66.1	64.0	62.1	60.3	58.6
8	Figure 10	1, 8	98.5	96.0	93.8	91.7	89.7	87.8	86.0
8 w/BC	Figure 15	1, 8	70.7	68.3	66.1	64.0	62.1	60.3	58.6
10	Figure 11	1, 10	59.1	56.9	54.8	52.9	51.1	49.5	48.0
10 w/BC	Figure 16	1, 10	70.7	68.3	66.1	64.0	62.1	60.3	58.6
12	Figure 12	1, 12	70.7	68.3	66.1	64.0	62.1	60.3	58.6
12 w/BC	Figure 17	1, 12	54.9	52.7	50.7	48.8	47.1	45.5	44.0
14	Figure 13	1, 14	92.9	90.5	88.2	86.1	84.1	82.2	80.5
14	Figure 13	2, 13	64.8	62.8	61.0	59.2	57.6	56.1	54.6
16	Figure 14	1, 16	61.4	59.1	57.0	55.1	53.3	51.6	50.0

Table 9 Single-ended Microstrip Impedance Matrix (Ohms)

STANDARD CONSTRUCTIONS		LAYERS	NOMINAL TRACE WIDTH (inches)						
LYRS	LOCATION		0.005	0.0055	0.006	0.0065	0.007	0.0075	0.008
6	Figure 9	3, 4	75.0	73.4	71.8	70.4	69.0	67.6	66.3
8	Figure 10	4, 5	65.2	63.2	61.3	59.6	57.9	56.4	54.9
8 w/BC	Figure 15	4, 5	65.2	63.3	61.5	59.8	58.1	56.6	55.1
10	Figure 11	3, 4, 7, 8	54.7	52.7	50.8	49.1	47.4	45.9	44.5
10 w/BC	Figure 16	4, 7	62.9	60.7	58.7	56.8	55.1	53.4	51.8
10 w/BC	Figure 16	5, 6	76.5	74.7	73.0	71.3	69.8	68.3	66.8
12	Figure 12	3, 4, 9, 10	62.7	60.6	58.7	56.9	55.2	53.5	52.0
12	Figure 12	6, 7	61.6	59.6	57.8	56.0	54.4	52.8	51.3
12 w/BC	Figure 17	4, 5, 8, 9	56.3	54.1	52.1	50.2	48.2	46.9	45.3
14	Figure 13	4, 5, 10, 11	57.5	55.4	53.4	51.5	49.8	48.1	46.6
14	Figure 13	7, 8	56.5	54.5	52.6	50.9	49.2	47.7	46.2
16	Figure 14	3, 4, 13, 14	51.0	48.9	47.1	45.3	43.7	42.2	40.8
16	Figure 14	6, 7, 10, 11	56.7	54.5	52.5	50.6	48.9	47.3	45.8

Table 10 Single-ended Stripline & Dual Stripline Impedance Matrix (Ohms)

CONFORMANCE TESTS

Controlled Geometry

Controlled geometry boards have specified thickness between certain layers and require no impedance coupons. These constructions do not give much flexibility regarding the materials used, and typically do not have many alternative constructions. HADCO will select the appropriate prepregs and cores that satisfy the dielectric spacing, tolerance, and overall thickness requirements. This is the least expensive impedance specification method.

AQL Testing

If testing is required, HADCO prefers to perform a [c=o] impedance test. This is the second least expensive impedance specification method.

100% Testing

All impedance coupons are 100% electrically tested when specified by the customer. After comparison against specified values, the measurements are electronically stored. This is the most expensive impedance test method.

Serialization

Serialization is a traceability process for controlled impedance jobs. HADCO will add test coupons to the panel to measure impedance with a TDR. When the impedance has been tested, the coupon and PWB have a serial number engraved on them. However, this procedure is not preferred by HADCO and will only be performed when specified by the customer. Serialization adds additional steps to the manufacturing process.

ELECTRICAL TEST

TESTING TUTORIAL

Electrical Test encompasses two types of tests: Continuity and Hi-pot. This testing is performed just prior to final inspection and shipping. OSP coated boards will be tested just prior to OSP coating.

Continuity Test

Continuity testing ensures that all endpoints of a net are connected and that they are not shorted to other nets. HADCO will also verify that all other points that will have an external connection or contact to them will be verified. In-Circuit-Test (ICT) points will be verified when the netlist and PWB data identify them. ICT points should have a pad that is a different size than the vias and should be included in the IPC-D-356 or IPC-D-356A netlist. This will ensure that they are tested properly. Data preparation is very important to ensure that a 100% test is performed. The most important points are:

- All testable points should have a pad that is flashed (such as .020 x .080), not drawn with vectors.
- Non-plated holes should not be included in the netlist.
- All test points should be included in the netlist.
- Vias that are also test points should have a different pad size than non-test vias. This will ensure that test points will included in the test fixture.

A netlist, which is derived from the CAD system, should be provided with the PWB data. This allows us to extract a netlist from the PWB data file and compare it against one generated from the CAD system. This will ensure that the board has been properly loaded into the CAM system.

Hi-pot Test

Hi-pot testing is performed to ensure that there is good isolation between all adjacent power planes. A high voltage DC potential, typically greater than 500VDC, is maintained between the layers for a short period. The leakage current is measured and an isolation resistance is then calculated.

TESTING DESIGN GUIDELINES

KEY REQUIREMENTS

Specification	Preferred	Available / Special Options:
Electrical test capabilities:		
Pitch:	0.020"	0.016", 0.010"
Fixture types:	Universal grid, dedicated	
Test voltages available:	100 volts	10 - 250 volts
Resistivity testing:		
Open resistance:	20 Ω	
Short resistance:	10 MΩ minimum	2 - 100 MΩ
Netlist capability:	Yes (IPC D 356 or IPC-D-356A)	Yes (Gerber netlist extraction)
Hi-pot testing:	250 to 1000 volts	

Continuity Test

Preferred Continuity Test Specifications:	Continuity:	20 Ω.
	Isolation:	10 MΩ.
	Voltage:	100 V.
Available Continuity Test Specifications:	Continuity:	>10 Ω.
	Isolation:	2 to 100 MΩ.
	Voltage:	10 to 250 V.

Netlist Programs

- For electrical testing, supply a correct IPC-D-356A or IPC-D-356 netlist file from which the required test program will be derived.
- If a netlist isn't supplied, one will be generated from the supplied PWB data. This is not considered a CAD referenced netlist test.
- To ensure boards receive 100% netlist testing, PWB data files should have the following characteristics:
  - (1) All test points and solderable features should be flashed, not drawn
  - (2) Non-plated through holes should not be included in the netlist.
  - All test points should be in the netlist.

Hi-Pot Test

Available Hi-Pot Test Specifications:	Voltage:	500 to 4000 VDC.
	Duration:	2 to 30 sec.
Preferred Hi-Pot Test Specifications:	Voltage:	500 V.
	Duration:	2 sec.

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PWB DATA REQUIREMENTS

PWB DATA REQUIREMENTS TUTORIAL

DATA FORMAT

The preferred choice of CAD data is, Valor ODB++, Orbotech Backup, CSI Auto plot, or RS-274-X Gerber. This type of data allows anyone using these formats to restore the complete job onto the CAM system, with out the use of an aperture wheel. These formats also eliminate any operator or software input mistakes during the read-in process, because all the aperture information is contained in the file along with any special aperture information. The need to merge files can also be eliminated by using one of the preferred data formats.

ODB++

Valor's ODB++ is the most preferred data format. It can, if set up from the start, contain intelligent information on features in the data. Features such as SMD pads, test points, plated holes, vias or none plated holes, to name only a few. These attributes help speed up design rule checks and pre-production engineering and test fixture generation. This approach permits an intelligent, error free transfer of the entire design. If analyzed correctly, this can also eliminate fabrication and pre-production editing and will significantly reduce cycle time.

The ODB++ file should be output using the "EXPORT" function in Enterprise. The file that is sent to HADCO should contain the Genesis file and the fabrication print (in HPGL format) along with the README file.

Valor ODB++, & Orbotech backup can also contain step and repeat information for sub panel arrays, with out making large complex data files.

Gerber

The standard RS-274-D Gerber format (not 274X) is also usable, but requires operator verification of the aperture wheel. Some aperture wheels can contain hundreds of apertures increasing the opportunity for error. The standard Gerber format should be avoided if any of the preferred data format options are available during output.

The preferred unit of measure is English, but Metric is usable. Never mix the units of measure within a job, like having the Gerber layers in English and the drill in Metric.

Aperture wheels and README files

To eliminate the manual input of each position of the wheel, it is preferred that standard wheels be used whenever possible. Standard wheels allow someone to read in several part numbers, using the same wheel, and not having to manually input the apertures into the computer each time. If standard wheels are not possible, keeping the wheels in a standard format is preferred. Standard formats allow scripts to be written that will allow the HADCO to automate the input process. If the format of the wheel changes, then each position on the wheel has to be inputted manually during each read in.

Regardless of the type of wheel used, it is important that any and all special apertures be clearly defined. Include drawings that define ID, OD, spoke size and degree of rotation for the thermal. It is also preferred that one wheel be supplied with a job. Try to avoid a wheel for each layer.

It is critical that the aperture wheel describes thermals as clearly as possible. Descriptions that include the word "thermal" are best. This description should include the inner diameter, outer diameter, break widths and angles.

Avoid special apertures and contour apertures when ever possible. Break or decompose these features into standard apertures before data output. Use one of the preferred formats Valor ODB++, Orbotech and RS-274-X if any special apertures or contours exist. This will eliminate the need for some one to build the aperture, and it will eliminate the possibility of errors.

Impedance controlled circuits should use an aperture or DCODE that is not used for any other features in the PWB.

Read me files need to contain all information that is not clearly defined in the aperture wheel. These types of things would include,

- information on merging layers
- descriptions of special aperture and contour names
- thermal descriptions
- complete list of files and prints sent
- Gerber, print and drill data format information
- a contact name and phone number for questions

Avoid notes in the README files, such as, "DELETE THERMAL USED ON .043 HOLES" or "GROW ALL 8 MIL LINES TO 10" or any special shipping or packaging instructions. The preferred method for CAM changes is to update the supplied data. The second preference is to place the notes on the fabrication print. Shipping or packaging instructions should be supplied in the purchase order, or specification.

Layer naming

All layers including the drill, solder masks, legends, via plug, and any layers that are merged, should be named and labeled within the layer as clearly as possible to prevent confusion. It is preferred that file numbering and sequences follow layer identification for copper layers.

Example: Compside = layer 1 and therefore file 1, Solder side = layer 6 therefore file 6. Soldermasks, legends, pastes etc. can follow all circuit level files.

Actual names might look like this, L1.GBR, SM1.GBR, SS1.GBR, PLUG6.GBR etc. Any instructions for merging etc. should be contained within the "read me" file, and the layers should be named to reflect the fact that they are to be merged. The layer name should be within the layer its self, outside of the crop lines.

APERTURE WHEEL AND README FILE EXAMPLE

MUNSTER HARD DRIVE INC.
READ ME, APERTURE LIST FOR PRINTED WIRING BOARD FABRICATION

PART NUMBER : 1313 REV: E BOARD DESCRIPTION: MOCKINGBIRD LN

==

L1.gbr layer 1
L2s.gbr layer 2 signal
L3p.gbr layer 3 plane
L4p.gbr layer 4 plane
L5s.gbr layer 5 signal
L6.gbr layer 6
sm1.gbr layer 1 soldermask
sm6.gbr layer 6 soldermask
ss1.gbr layer 1 silkscreen
ss6.gbr layer 6 silkscreen
mrg4.gbr merge with layer 4
print.gbr blue prints
drl.exl drill (Excellon format)
npt.gbr non plated holes
rout.gbr profile

Note: merg4.gbr must be merged with layer 4 before plot

character format: ASCII
coordinates: absolute
number format: 2.4
zeros omitted: leading

APERTURE LIST

D_Code	Shape	Type	Power OD	Power ID	Power BRAKE	Height(Y)/Diameter	Width(X)
10	circle	trace				0.050000	0.000000
11	circle	trace				0.008000	0.000000
12	thermal	flash	.046	.031	.015	0.000000	0.000000
13	thermal	flash	.065	.050	.015	0.000000	0.000000
15	thermal	flash	.105	.085	.020	0.000000	0.000000
16	rectangle	flash				0.040000	0.070000
17	rectangle	flash				0.050000	0.040000
18	circle	trace				0.025000	0.000000
19	circle	trace				0.024000	0.000000

Define Power Aperture 28 Thermal Relief .046 OD x .031 ID .015 *see below
Define Power Aperture 30 Thermal Relief .065 OD x .050 ID .015 *see below
Define Power Aperture 32 Thermal Relief .105 OD x .085 ID .020 *see below

* NOTE: ALL THERMAL BRAKES ARE AT 45 DEGREES

M.H.D. Inc. Contact: Herman Munster - days 714-555-5555 24 hr Pager number – 714-555-5555

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ARRAYS (SUBPANELS)

It is preferred that the data supplied contain all of the array information. The array data should contain fiducials, tooling holes, fiducial clearances, along with anything else that is required in the array. In most cases this is only practical if the array contains only one PWB. If the array contains more than one PWB, the array data may be too complex, and it may not be practical to modem and archive. There are two ways around the huge data problem, and still supply all the benefits of array data.

- Valor ODB++ or Orbotech backup is the ideal format to use when sending stepped array data. These formats contain 1 set of 1-up data, but it also contains the step and repeat information for the array. This greatly reduces the file size on multiple up arrays with all of the benefits of sending complete array data.

- Another alternative is to build the complete array data, rails, fiducials, tooling, holes, etc., but only step one PWB into that array, even if the array has 6 PWB's in it. Then allow the board shop to step the PWB data into the customer supplied array data.

When complete array data is sent with multiple sets of PWB data, and the PWB's do not match each outer in the same array, adding a note on the print explaining the intent will eliminate any confusion.

PWB DATA REQUIREMENTS DESIGN GUIDELINES

KEY REQUIREMENTS	
Data Must Include:	README.TXT file , Legible fabrication drawing file , Drill (NC) file , Aperture list , All PWB Files , CAD netlist test data
Compression:	.ZIP. .Z, .TAR, .ARC, LHA (.LZH), ARJ
Data Format:	ODB++, RS-274-X, RS-274-D, Orbotech Backup, CSI autoplot
Drill and Rout File:	EXCELLON (Tool format D-xx, units: inches or mm)
Fabrication Drawing:	HPGL 1 or 2, Postscript, Gerber, AUTOCAD (.DXF), .CGM
Netlist:	IPC-D-356A, IPC-D-356
Floppy Disk	3 ½ IBM or UNIX format, 5 ¼ IBM format

TRANSMITTING DATA TO HADCO

The preferred method of receiving data is by Internet or by modem transmission, with all the files contained inside of one ZIP or TAR file. In order for HADCO to better serve you, we have several different modem settings and two types of modems

Internet Transfer

The preferred method of receiving data is via FTP over the Internet. Transmitting FTP data files to HADCO is simple and very reliable. If FTP is inaccessible, file transmission may be made by modem, or attached to an e-mail. For ease of transmission, please contain all the files inside of a ZIP or TAR file.

FTP TRANSFER VIA THE INTERNET

FTP accounts *must* be set up for all new users before attempting to send files via FTP. Please contact the HADCO Central Data Administrator at 603-896-2626 to establish an account and to receive a password. FTP procedures in both Word 97 and ASCII (plain text) format and a confirmation containing account and password information will be emailed to you immediately.

A typical FTP login procedure:

- From the DOS or Unix command line, enter: ftp ftp.hadco.com
- NOTE: If you receive the error message "unknown host" or "can not resolve remote host", use the IP address 148.164.6.1 as the site name (i.e., ftp 148.164.6.1)
- When prompted for a login, enter your assigned login ID
- When prompted for a password, enter your assigned password
- There is no need to create a subdirectory. You are automatically dropped into the next sequential directory up from the last time you logged in (if this is your first time, you will be logged into sequence directory "1", the next time you login it will be "2", the time after that it will be "3", etc.)
- At the ftp> prompt, change to binary mode by typing "binary"
- To get a visual representation of the progress of your transfer, at the ftp> prompt type "hash"
- Type "put datafile", where "datafile" is the actual name for *your* data file
- When the transfer is complete, type "bye" to logout from the HADCO FTP site

When the FTP transfer is completed, upon disconnection, an email message is automatically generated and posted to our Customer Service Bulletin Board letting your Customer Service Representative know that the file has been received at HADCO. Contact the HADCO Central Data Administrator at 603-896-2626 if you are experiencing any difficulty using the FTP site.

Modem login

Modem accounts *must* be set up for all new users before attempting to send files via modem. Please contact the HADCO Central Data Administrator at 603-896-2626 to establish an account and to receive a password.

- Modem phone number   603-896-2282
- Protocol   ZMODEM
- Data Bits   8 bits
- Parity   None
- Stop Bits   1
- Duplex   Full

Host software is HyperACCESS

When the modem transfer is completed, upon disconnection, an email message is automatically generated and posted to our Customer Service Bulletin Board letting your Customer Service Representative know that the file has been received at HADCO. Contact the HADCO Central Data Administrator at 603-896-2626 if you are experiencing any difficulty transmitting via modem.

E-mail attachment

Files may be sent to HADCO as an e-mail attachment. This is not encouraged because there is significant file corruption for files sent using this method. Sending files using the FTP or modem methods is preferred.

DATA PACKAGE CONTENT

It is important to send the complete tooling package at one time. Missing files or prints can cause unnecessary delays and confusion. It is also important to have the data be error free. This includes ensuring that the data conforms to your design rules and HADCO DFM rules. This will ensure a quick transition into manufacturing.

The following is a checklist of the major items that should be included in a complete tooling package.

Specifications

- PWB fabrication specification. IPC-6012 will be utilized if no specification is provided.

Layer Data

- All inner and outer layer data. Preferred format is Valor's ODB++, or 274X
- Solder mask layers
- Legend layers
- Drill layers
- Via plug layers
- All layers passed the design rule and producability checks
- Read me file that contains the wheel and any special instructions, all long with a contact name and phone number for design questions or problems.
- IPC-D-356A or IPC-D-356 netlist.

Fabrication Print

- Include a drawing for the PWB and sub-panel (assembly panel).
- All dimensions tolerances have been reviewed for producability
- Hole charts with all hole sizes and tolerances
- Multilayer build ups, copper weights and materials
- Any special notes on the build up such as buried capacitance
- Any special notes for impedance control, tolerance, what line widths etc.
- Solder mask type
- Legend ink color
- Surface finish (solder, immersion gold, OSP)
- Gold and nickel thickness
- Rout dimensions for cut outs, arrays, and the PWB
- Dimensions for score, bevel and slots
- Locations for any dimensioned holes, fiducials or IRMs
- Descriptions for IRMs, fiducials, and fiducial clearances
- Special notes on adding thieving to the outer layers, keep out areas etc.
- Special notes on non functional pad removal from inner layers
- Fabrication specification reference

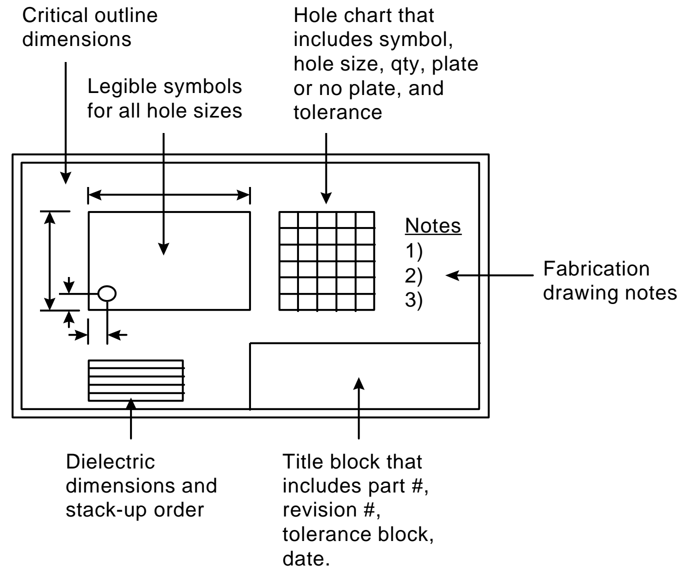

Figure 54 Fabricaion print requirements

NOTE: Accurate PWB data is essential to manufacture a perfect PWB. It is important that the blueprint revision, film revision, and drill tape revisions all agree. All of the documentation part numbers should also be identical. In addition, any special instructions should be instructed in the README.TXT file.

File Name:	README.TXT
Format:	ASCII, or MS/Word
Contents:	Company name Division name (and / or location) List of files in the package Board Part Number and Revision Purpose of the submittal: QUOTATION and/or PRODUCTION? Technical Contact (name and best times to call) Phone number Fax number EMAIL address (If available) Special Instructions

Table 11 README.TXT Content

COMMON DATA ISSUES

Two types of data issues are frequently encountered: critical and non-critical. Critical data issues can be substantial enough to stop the tooling process, while non-critical data issues simply result in additional edits that need to be performed. The following lists present the most common errors. Minimization of these issues will decrease tool generation time.

Critical Problems

- Bad Compression (cannot unzip)
- Formats not recognized
- No README.TXT file
- Missing Gerber files
- Missing Drill Files
- Missing Aperture List
- Unclear aperture list
- Missing FAB prints of files
- FAB prints are not legible
- Information does not match
- Outside HADCO's manufacturing capabilities
- Does not meet HADCO PWB reliability criteria
- Missing "D" codes
- Revisions do not match

Non-Critical Problems

- Netlist not supplied.
- No README.TXT file (when aperture wheel reads).
- Design, as supplied, violates the OEM provided specifications / documentation?
- Design, as supplied, violates the Contract Assemblers provided specifications?
- Violations on rules that improve yield.

Manual Edits

- Rename layers
- Realign Gerber layers
- Convert draws to flashes (O/L's)
- Convert draws to flashes (S/M)
- Type in aperture list
- Type in thermals
- Copy soldermask layer

PRICE CONSIDERATIONS

The board price is dependent on many variables. The following tables present the cost factors.

TURN-AROUND TIME

High price	Prototype	The fastest turn-around time and quality is most important. Manufacturing will start more boards than may be required to ensure that the schedule is met. There is less automated processes due to the small lot sizes.
Mid price	Quick Turn (QT)	A shorter time than available in volume runs and quality are very important. Manufacturing will start lot sizes which are not optimized for volume.
Low price	Volume	Lot sizes are released which are optimized for the automated volume equipment.

TECHNICAL ATTRIBUTES

High Cost Factors

Advanced technologies
Buried vias
Layer count
Material utilization
Selective plating
Line width and space

Medium Cost Factors

Mechanical drill hole quantity
Drilled hole size
Embedded resistors
Non FR-4 materials
Buried Capacitance
Non-single ply materials
Edge plating
High Tg versus low Tg material
Drilled holes between 0.010” & 0.012”

Low Cost Factors

Complex routing, scoring or beveling
Edge routing
> 0.093 thick PWB’s
< 0.030 thick PWB’s
Via plug
Legend

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COST TRADE-OFFS

The following list presents some general rule-of-thumb trade-offs that will provide the most cost effective higher interconnect density.

- Use a smaller line width/space before adding layers
- Investigate how boards will fit into a production panel to ensure that maximum material utilization occurs.
- Laser, plasma or photo-imaged blind vias before buried vias.
- Smaller holes before adding layers.

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ADVANCED TECHNOLOGIES

Component packaging is requiring denser and less expensive interconnect solutions. The traditional approach is to increase the PWB layer count while reducing the signal line width and space. This approach has fundamental limitations because the relatively large signal vias start to block a significant amount of routing channels. New techniques are required which can provide higher interconnect density at existing cost structures.

HADCO is both providing and researching advanced interconnect solutions that encompass the packaging from a system perspective. This following table provides a quick summary of the available technologies.

Vias	Blind	Laser, Photoimageable, Mechanical
	Buried	Laser & Mechanical
	Blind & Buried	Laser & Mechanical
Embedded Components	Capacitance	Buried Capacitance™ EmCap™
	Resistors	Ohmegaply®
	Inductors	Planar Magnetics
Connection Solutions	Flexible	
	HVRFlex	
	Rigid-Flex	
Value Added Manufacturing	Backplanes	
	Box Build	
	Functional Test	
Materials	High frequency or low loss	

APPENDIX 1: TERMS AND DEFINITIONS

ANNULAR RING: That portion of conductive material completely surrounding a hole.

ASPECT RATIO: A ratio of length or depth of a hole to its pre-plated diameter.

B-STAGE: An intermediate stage in the reaction of a thermosetting resin in which the material softens when heated and swells in contact with certain liquids, but does not entirely fuse or dissolve.

B-STAGED RESIN: A resin in an intermediate state of cure. The cure is normally completed during the laminating cycle.

BASE MATERIAL THICKNESS: The thickness of the base material excluding metal foil or material deposited on the surfaces.

BOARD THICKNESS: The overall thickness of the base material and all conductive materials deposited thereon.

BOW: The deviation from flatness of a board characterized by a roughly cylindrical or spherical curvature such that, if the board is rectangular, its four corners are in the same plane.

C-STAGED RESIN: A resin in a final state of cure.

CLEARANCE HOLE: A hole in the conductive pattern larger than, but coaxial with, a hole in the printed board base material.

CONDUCTOR BASE WIDTH: The conductor width at the plane of the surface of the base material.

CONDUCTOR LAYER: The total conductive pattern formed on one side of a single layer of base material. (This may include all or portion of ground and voltage planes.)

CONDUCTOR LAYER NO. 1: The first layer of a printed board having a conductive pattern on or adjacent to the primary side.

CONDUCTOR THICKNESS: The thickness of the conductor including all metallic coating. (It excludes nonconductive protective coating.)

CONDUCTOR WIDTH: The observable width of a conductor at any point chosen at random on the printed board normally viewed from directly above unless otherwise specified.

CONTROLLED IMPEDANCE: Controlling or modifying the characteristic impedance of the Printed Wiring board to match source and load impedance's.

CONTROLLED IMPEDANCE COUPON: A test coupon on the panel which is used to measure the characteristic impedance of the board(s) on that panel.

DIELECTRIC: An insulating material, such as rubber, glass or waxed paper. When a dielectric is placed between power and ground plates, the capacitance increases.

EXTERNAL LAYER: A conductive pattern on the surface of a printed board.

GLASS TRANSITION TEMPERATURE: The temperature at which an amorphous polymer (or the amorphous regions in a partially crystalline polymer) changes from a hard and relatively brittle condition to a viscous or rubbery condition. (This transition occurs with increasing temperature and generally over a relatively narrow temperature range; it is not a phase transition. In this temperature region, many physical properties undergo significant rapid changes. Some of those properties are hardness, brittleness, thermal expansion, specific heat, etc.)

GROUND PLANE CLEARANCE: Ground-plane clearance is the etched portion of a ground plane around a hole that isolates the plane from the hole.

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HOLE BREAKOUT: A condition in which a hole is not completely surrounded by the land.

IMPEDANCE: The ratio of voltage to current in a propagating wave, i.e., the impedance which is offered to this wave at any point of the line. (In printed boards its value depends on the width of the conductor, the distance from the conductor to ground planes, and the dielectric constant of the media between them.)

INTERNAL LAYER: A conductive pattern that is contained entirely within a multilayer printed board.

KEY SLOT: A slot in a printed board which permits the printed board to be plugged into its mating receptacle but prevents it from being plugged into any other receptacle.

LAMINATE THICKNESS: Thickness of the metal-clad base material, single or double-sided, prior to any subsequent processing.

LAMINATE: A product made by bonding together two or more layers of material.

LAND: A portion of a conductive pattern usually used for electrical connection, component attachment, or both.

LANDLESS HOLE: A plated-through hole without a land.

LAYER-TO-LAYER REGISTRATION: The degree of conformity of a conductive pattern, or portion thereof, with that of any other conductor layer of a printed board.

LAYER-TO-LAYER SPACING: The thickness of dielectric material between adjacent layers of conductive patterns in a multilayer printed board.

LEGEND: A format of letters, numbers, symbols and patterns on the printed board primarily used to identify component locations and orientation, for convenience in assembly and replacement operations.

MICROSECTIONING: The preparation of a specimen for the metallographic examination of the material to be examined (usually by cutting out a cross-section, followed by encapsulation, polishing, etching, staining, etc.).

MICROSTRIP: A type of transmission line configuration that consists of conductor over a parallel ground plane, and separated by a dielectric.

MINIMUM ANNULAR RING: The minimum width of metal, at the narrowest point, between the edge of the hole and the outer edge of the land. This measurement is made to the drilled hole on internal layers of multilayer printed boards and to the edge of the plating on outside layers of multilayer boards and double sided boards.

MULTILAYER PRINTED WIRING BOARD: A part manufactured from rigid base material upon which a completely processed Printed Wiring has been formed on more than two layers each separated by insulating materials and bonded together.

NONFUNCTIONAL LAND: A land on internal or external layers, not connected to the conductive pattern on its layer.

OVERALL PANEL DIMENSIONS: The actual physical outside dimensions of the panel.

PANEL: A rectangular or square sheet of base material or metal-clad base material of predetermined size used for the processing of one or more printed boards and, when required, one or more test coupons.

PANELIZATION: The process of positioning circuit patterns on a manufacturing panel and incorporating features such as tooling holes, fiducials, etc., to facilitate manufacturing.

PLATED-THROUGH HOLE: A hole in which electrical connection is made between internal or external conductive patterns, or both, by the plating of metal on the wall of the hole.

POSITIVE ARTWORK: An artwork, artwork master or production master in which the intended conductive pattern is opaque to light, and the areas intended to be free from conductive material are transparent.

PREPREG: Sheet material impregnated with a resin and cured to an intermediate stage.

PRINTED BOARD: The general term for completely processed Printed Wiring and Printed Wiring configurations. (It includes single-sided, double-sided, and multilayer boards with rigid, flexible, and rigid-flex base materials.)

PRINTED WIRING: A conductive pattern composed of printed components, Printed Wiring, or a combination thereof, all formed in a predetermined design and intended to be attached to a common base. (In addition, this is a generic term used to describe a printed board produced by any of a number of techniques.)

REFERENCE DIMENSION: A dimension without tolerance used only for informational purposes that does not govern production or inspection operations.

SIGNAL PLANE: A conductor layer intended to carry signals, rather than serve as a ground or other fixed voltage function.

SOLDER LEVELING: A solder coating process where heated gas or other media levels and removes excess solder.

SOLDER PLUG: A core of solder in a plated-through hole.

SOLDER-SIDE: The secondary side of a single-sided assembly.

STEP-AND-REPEAT: A method by which successive exposures of a single image are made to produce a Multiple Image Production Master. (A term used in the CAM environment for describing the process of reproducing successive circuit images electronically.)

TENTING: A printed board fabrication method of covering holes and the surrounding conductive pattern with a resist that is usually dry film.

TEST COUPON: A portion of the quality conformance test circuitry used for a specific acceptance test or group of related tests.

THERMAL RELIEF: Crosshatching a ground or voltage plane to minimize blistering or warpage during soldering operations.

THIEVING: A racking device or non-functional pattern area on the panel used in the electroplating process to provide a more uniform current density on plated parts. ("Thieving" absorbs the unevenly distributed current on irregularly shaped parts, thereby assuring that the parts will receive an electroplated coating of uniform thickness.)

TRANSMISSION LINE: A signal-carrying circuit composed of conductors and dielectric material with controlled electrical characteristics used for the transmission of high-frequency or narrow-pulse type signals.

TWIST: The deformation parallel to a diagonal of a rectangular sheet such that one of the corners is not in the plane containing the other three corners.

USEABLE AREA: The area on a manufacturing panel largely available for Printed wiring board imaging.

USEABLE PANEL AREA: The largest area available for imaging manufacturing features and Printed wiring boards.

VIA: A plated-through hole used as an inter-layer connection, but in which there is no intention to insert a component lead or other reinforcing material.